

R2A20112A

R03AN0009JJ0100

Application Note

Rev.1.00

Feb 22, 2012

1. Introduction

The R2A20112A is an active power factor correction controller that operates in the critical conduction mode. And the R2A20112A has the interleaved operation function that controls two boost converters of the master and the slave with 180 degree phase shift.

This document is described outline of PFC operation, device functions and design for SMPS.

Refer to the data sheet for the device electrical characteristics, maximum ratings and so on.

2. Constant ON Time Control

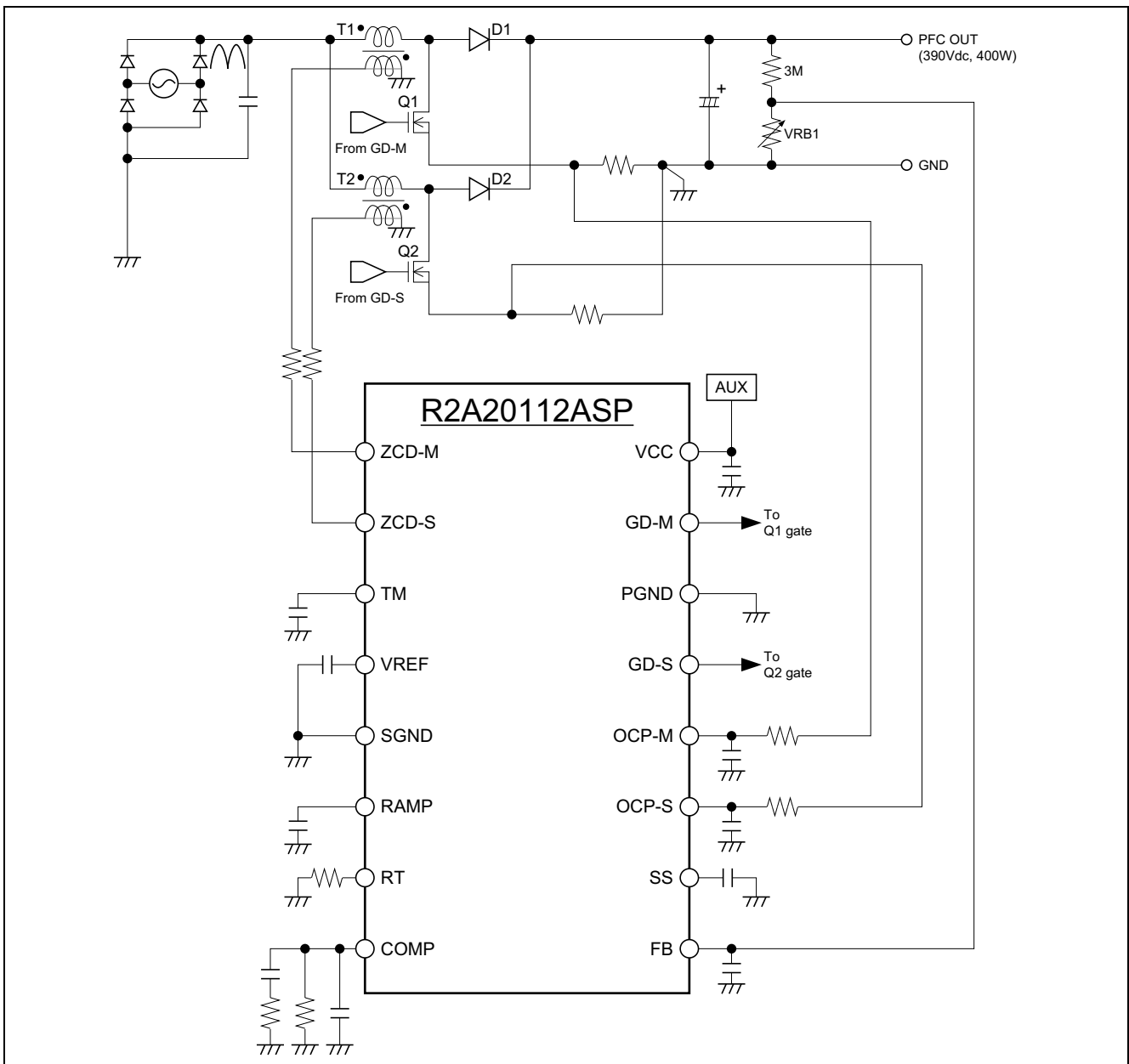


Figure 1 System Diagram

The R2A20112A is a power factor correction boost converter controller with critical conduction mode (CRM). The CRM is the operation mode between continuous conduction mode (CCM) and discontinuous conduction mode (DCM), and it is controlled by detecting zero current of boost inductor and changing switching frequency one by one. R2A20112A's CRM operation is adopted "Constant ON Time" control method by which gate ON time becomes constant according to a relation of input and output conditions.

Gate ON time is generated from error amp and saw tooth wave (RAMP waveform), and it becomes constant because error amp voltage if the conditions of input and output don't change. As a result, inductor current is changed peak values according to input voltage.

At this time, inductor current becomes continuous triangle wave, and its peak current turns into a proportional value to AC voltage. Moreover, the average value of this triangle wave ( $I_{ac}$ ) becomes 1/2 of the inductor peak current. Therefore, the input waveform according to input voltage can be obtained by smoothing of the inductor current.

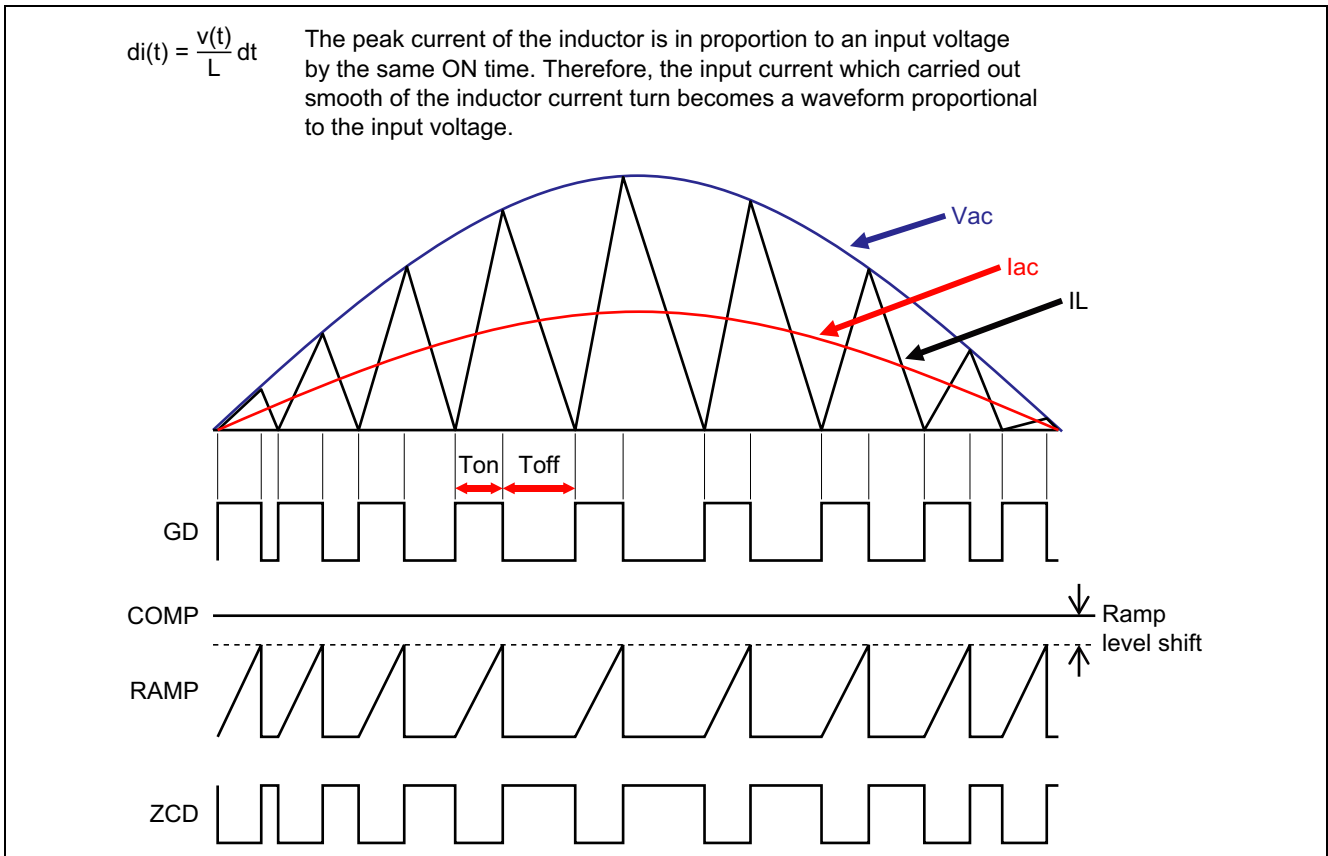


Figure 2

3. Block Diagram

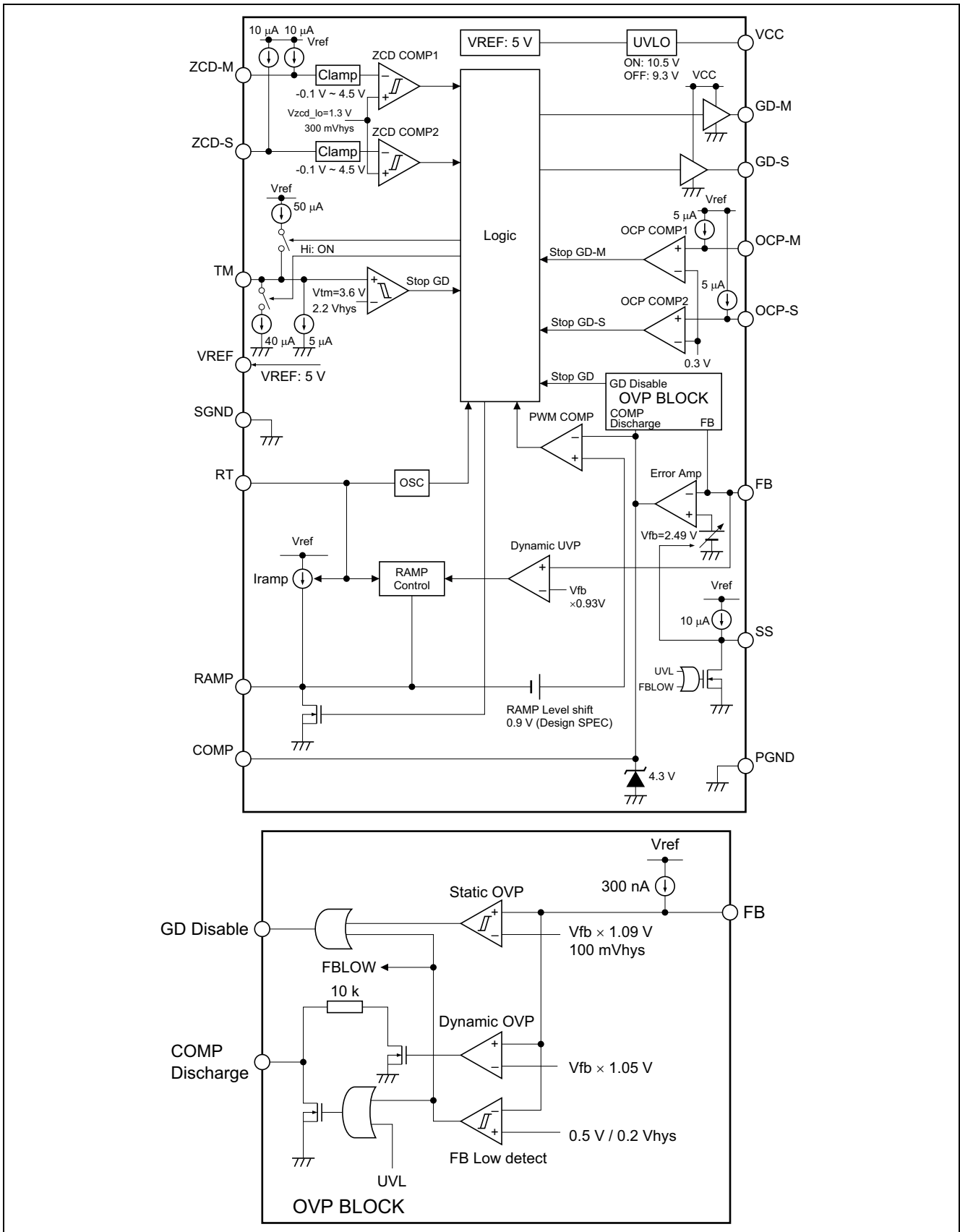


Figure 3 Block Diagram

### 3.1 UVLO and Reference Voltage Block

UVLO (Under voltage lock out) is a function for not operating IC when supply voltage is low. This function will be canceled when the supply voltage becomes 10.5 V typ. or more. UVLO has 1.2 V typ. hysteresis voltage. Reference voltage VREF (5 V typ.) is used for the power supply of each internal block, and internal reference voltage Vfb (2.49 V typ.) for non inverting input to Error Amp is also generated from VREF.

### 3.2 Error Amp

The Error Amp keeps PFC output voltage constant. It is a transconductance amplifier, and non inverting input terminal is connected to internal reference voltage Vfb (2.49 V typ.). Inverting input terminal is connected to FB pin which detects PFC output voltage. COMP pin of Error Amp output is connected to PWM comparator and controls PFC output voltage.

When AC input is supplied and VCC is not supplied, a current flows from PFC output to VCC through the divider resistor and internal ESD protection diode which is between FB pin and VCC pin.

Though this current changes by the divider resistor value and AC input voltage, it should not exceed 300  $\mu$ ADC.

### 3.3 Zero Current Detection

The zero current detection (ZCD) signal is necessary for CRM operation. It detects zero current in boost inductor and turns-on MOSFET.

ZCD signal is made from the auxiliary winding of the boost inductor, the auxiliary winding is connected to ZCD pin through a current limit resistor RZCD. ZCD pin voltage is clamped by RZCD and the internal clamp circuit. The clamp voltage is hi-side 4.5 V/low-side -0.1 V and the maximum source and sink current are 3 mA.

Also 10  $\mu$ A constant current flows into outside. In case the AC input voltage is high and an amplitude of the auxiliary winding goes low, however it is easy to exceed the ZCD high threshold voltage 1.6 V by this source current.

When the auxiliary winding open, ZCD pin is pulled up to 4.5 V by this constant current.

In case VCC of IC is not supplied, and if the secondary winding has some voltage, a current flows from ZCD pin to VCC pin. However this current should not exceed 3 mA which is same as the maximum ratings of ZCD pin.

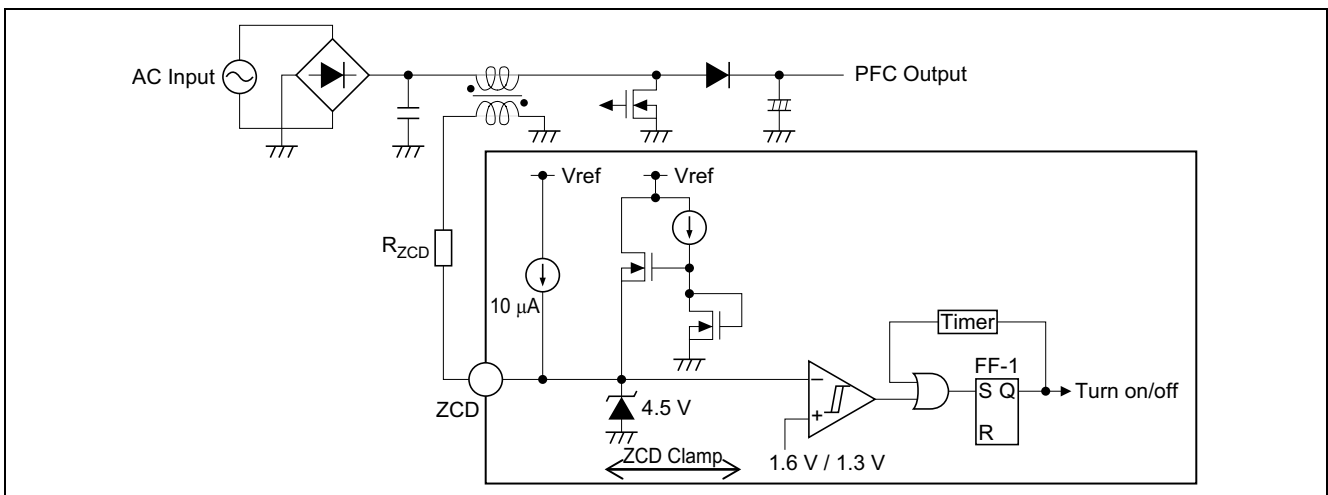


Figure 4

### 3.4 RAMP Generator

RAMP generator outputs saw tooth wave to PWM comparator in order to determine the ON time.

The RAMP slope decode a maximum ON time which can be outputted, and it is determined by external capacitor and resistor.

The resistor is connected between RT pin and GND, and the capacitor is connected between RAMP pin and GND. RT pin resistor decides the internal oscillation frequency. So that this resistor value should be fixed 33 kΩ. In this case, RAMP pin source current is 50 μA typ.

The ramp generator starts RAMP pin charge when ZCD detects the inductor zero current and RAMP pin voltage is under 0.2 V. The ramp generator starts to discharge RAMP pin when the ramp slope added internal level shift voltage 0.9 V reaches COMP voltage. Therefore, On time becomes maximum at COMP clamp voltage 4.3 V. In addition, the ON time becomes zero when COMP voltage is under 0.9 V which is internal level shift voltage because RAMP slope is always over the COMP voltage and discharged.

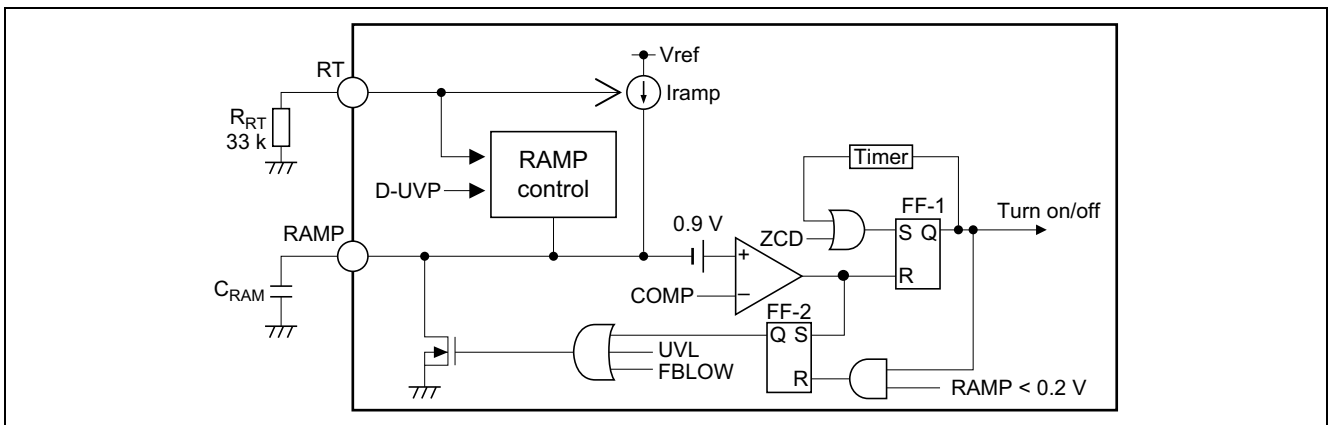


Figure 5

### 3.5 Drive Stage

GD pin outputs drive pulse for POWER MOSFET. The R2A20112A contains two totem-pole output stages for master and slave. The source drive ability is 300 mA peak and the sink drivability is 1.2 A peak.

Please adjust a driver circuit according to the characteristics of using Power MOSFET.

Zero current switching influences the loss by Turn-off speed, and doesn't have the so much influence by Turn-on speed in the loss. The example of driving circuit is shown in the following.

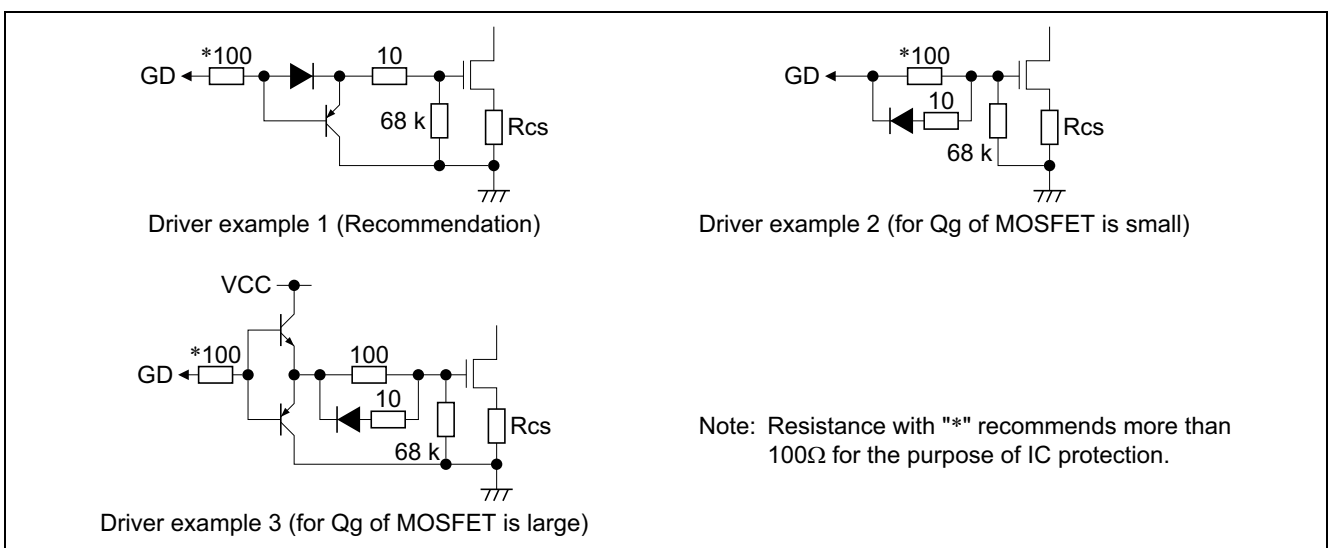


Figure 6

### 3.6 Protect Functions

#### 3.6.1 Over Voltage Protection (OVP)

These functions are for restriction of PFC output voltage rises when output voltage exceeds setting value, and it has two step protect functions.

(1) Dynamic over voltage protection (D-OVP)

Dynamic over voltage protection (D-OVP) discharges COMP pin voltage when FB pin voltage reaches  $1.05 \times V_{fb}$  (2.49 V typ). The Power MOSFET on time is limited gradually, therefore the audio noise is avoided because an inductor current does not stop suddenly.

(2) Static over voltage protection (S-OVP)

Static over voltage protection (S-OVP) stops an output when FB pin voltage reaches  $1.09 \times V_{fb}$ .

Power MOSFET turns off quickly and S-OVP keeps stopping an output till FB pin voltage reaches  $1.05 \times V_{fb}$ .

#### 3.6.2 PFC Output Voltage Drop Protection (D-UVP)

D-UVP (Dynamic Under Voltage Protection) is built in. When FB pin voltage goes down under  $V_{fb} \times 0.93$  by load change or input voltage change, RAMP charge current is reduced to half (25  $\mu\text{A}$  typ), and then  $t_{on}$  expand to twice quickly in order to prevent PFC output voltage drop.

#### 3.6.3 Feedback Open Loop Detection

This function is for detection of abnormalities of dividing resistors in PFC output feedback line.

(1) The resistor opened between PFC output and FB pin:

When FB pin becomes  $FB < 0.5 \text{ V}$ , COMP pin is discharged.

Therefore, a switching is stopped. The detection voltage has 0.2 V hysteresis.

(2) The resistor opened between FB pin and GND:

FB pin is pulled up by PFC output voltage. Therefore, FB pin detects S-OVP and a switching is stopped.

(3) FB pin opened:

FB pin is pulled up by self 300 nA source current.

Therefore, FB pin detects S-OVP and a switching is stopped.

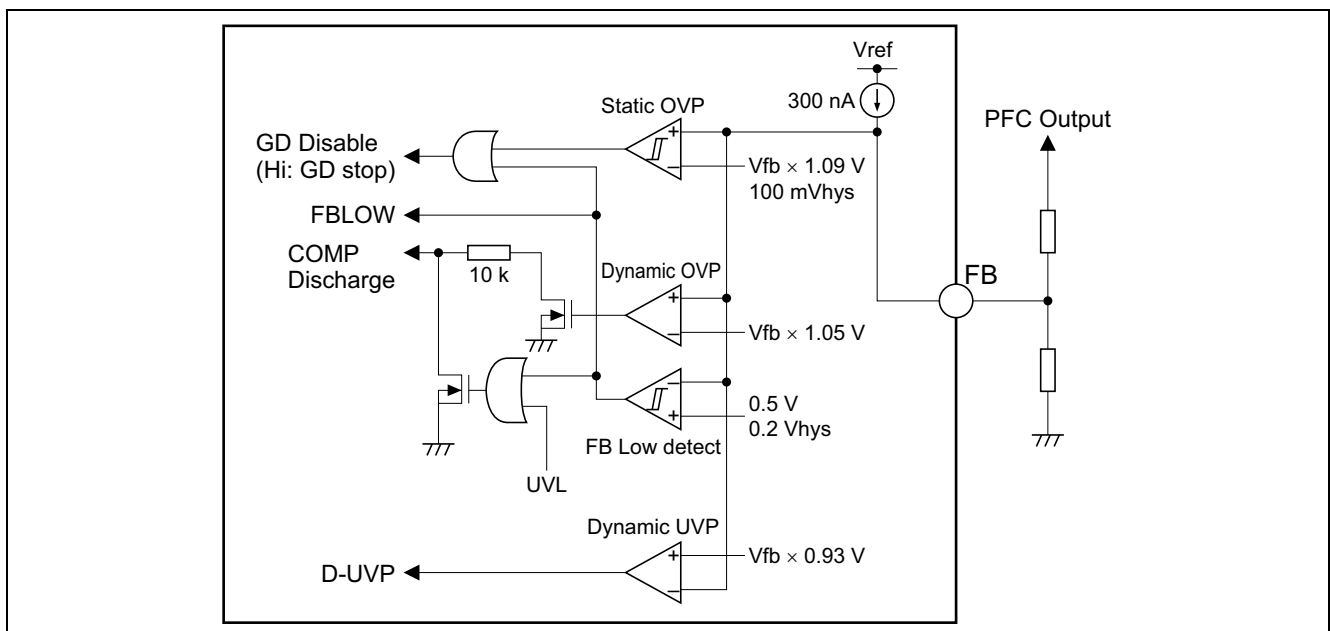


Figure 7 Protect Functions at FB

### 3.6.4 Over current protection (OCP)

This is a function which turns off GD pulse and protects Power MOSFET when drain current of each Master and Slave power MOSFET becomes more than setting value.

OCP pin senses the each Power MOSFET drain current by using an external sense resistor.

When OCP-M or OCP-S pin reaches 0.3 V, an output is disabled by pulse by pulse.

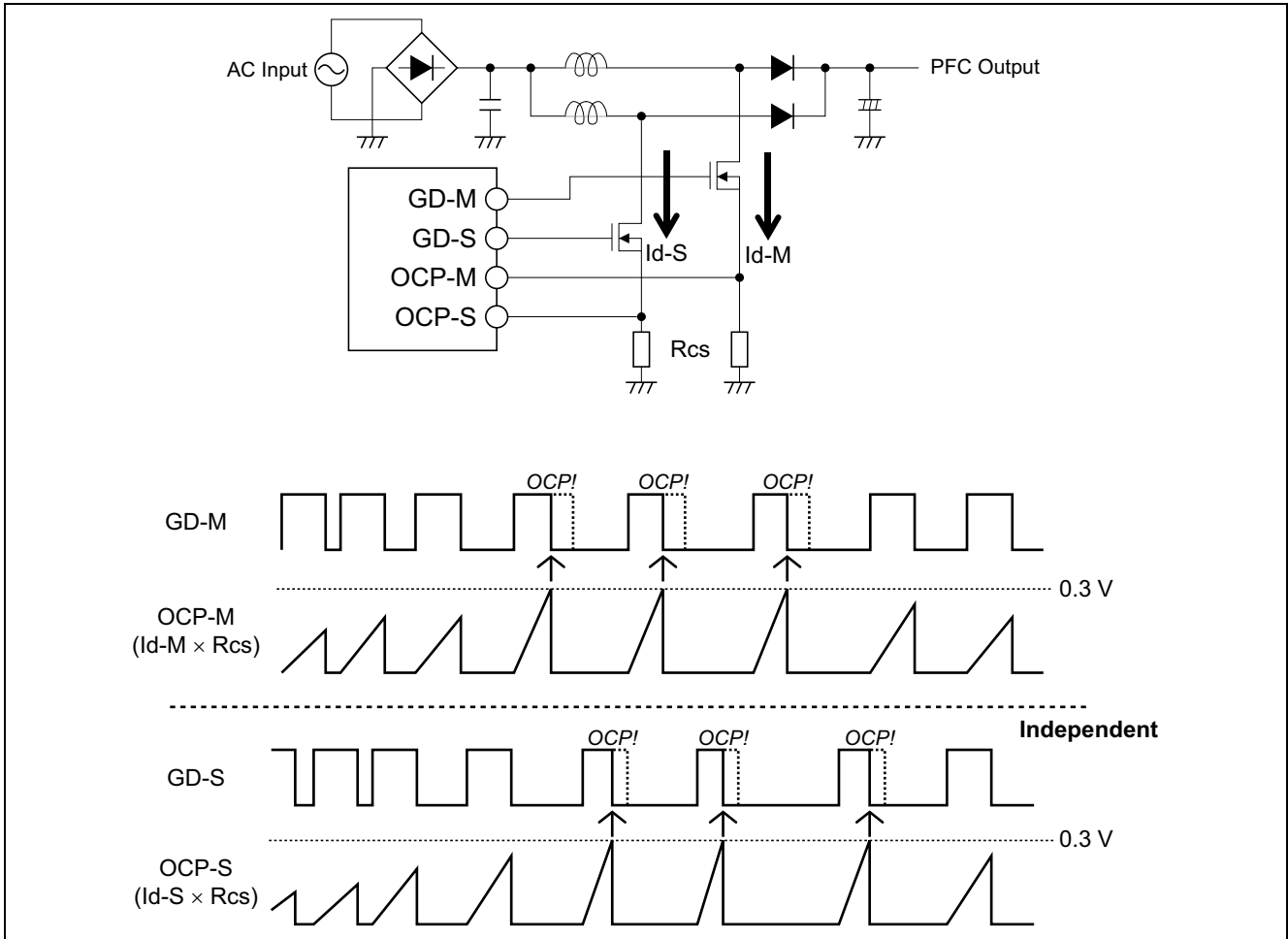


Figure 8

### 3.6.5 Open/Short Detection of Zero Current Detection

This is the function to detect abnormalities of ZCD pin like an open or short and to prevent heating of peripheral components such as boost inductor.

(1) Master ZCD pin can not detect master zero current by ZCD pin open or GND short:

Master operates with restart mode, and maximum on time of master is 1  $\mu$ s in restart mode, and slave does not operate in master restart mode, so that it is possible to avoid heat up of master and slave converters.

(2) Slave ZCD pin can not detect slave zero current by ZCD pin open or GND short:

A switching of master and slave stops to avoid heat up of master converter.

In this case IC stops a switching with latch function, and the latch is reset when VCC voltage is under UVLO threshold voltage.

To detect abnormalities of ZCD-S pin is fulfilled following conditions.

(a) ZCD-S pin is open or GND short, and ZCD signal does not cross the threshold voltage.

(b) Master is not in restart operation.

(c) Master On time is longer than 0.7  $\mu$ s.

When all of above-mentioned (a), (b), and (c) are fulfilled, ZCDS abnormalities of is detected with a delay.

Time until the switching stops by the latch depends on a switching frequency of the master.

This function does not operate at a light load because (b) and (c) are not fulfilled.

However the pulse width is thin at this time, so that it is possible to avoid heat up of master and slave converters.

Notes: 1. Delay time of detection is made by the internal counter, and it is 1024 count of switching.

In case of 10 kHz switching frequency, it will be around 100 ms.

IC carries out count-up start by fulfillment the conditions (a), (b) and (c), and reset when it to be out from these conditions.

2. ZCD open detection might not work correctly by the noise to the ZCD pin.

In that case, it is a potential to improve by adding the few pF capacity on ZCD pin through GND.

### 3.6.6 Soft Start

This is the function to start extending On time of Power MOSFET gradually. It controls the internal Error Amp reference voltage Vfb and prevents PFC output voltage rapidly rising and over shoot. When SS pin voltage is within 0 V to 3.8 V.

SS pin charge current is 10  $\mu$ A typ constant current, and SS time is adjustable by changing capacitor value. In addition, this IC has boost charging function. When FB pin has initial voltage with input voltage, charge current is increased and SS pin is quickly charge to the voltage. Therefore, start up time becomes shorten.

SS pin discharge the capacitor when VCC is under UVLO threshold voltage or FB pin detect to FBLOW. If Soft start function is not needed, please connect with 10 pF capacitor between SS pin and GND or connect 100 k $\Omega$  resistor between SS pin and VREF pin.



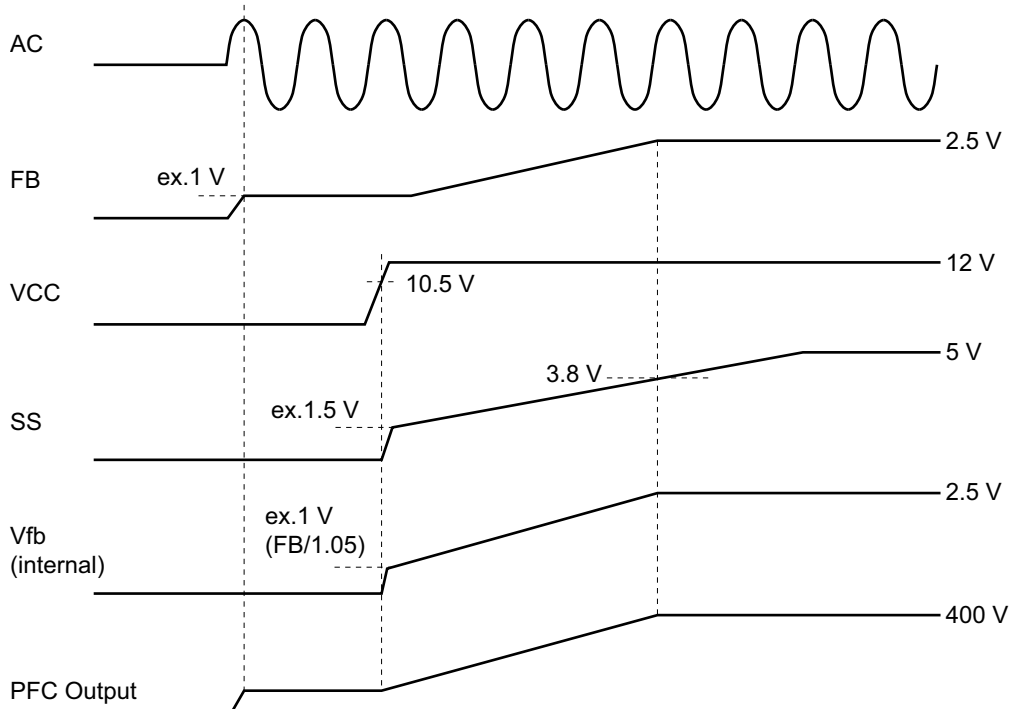
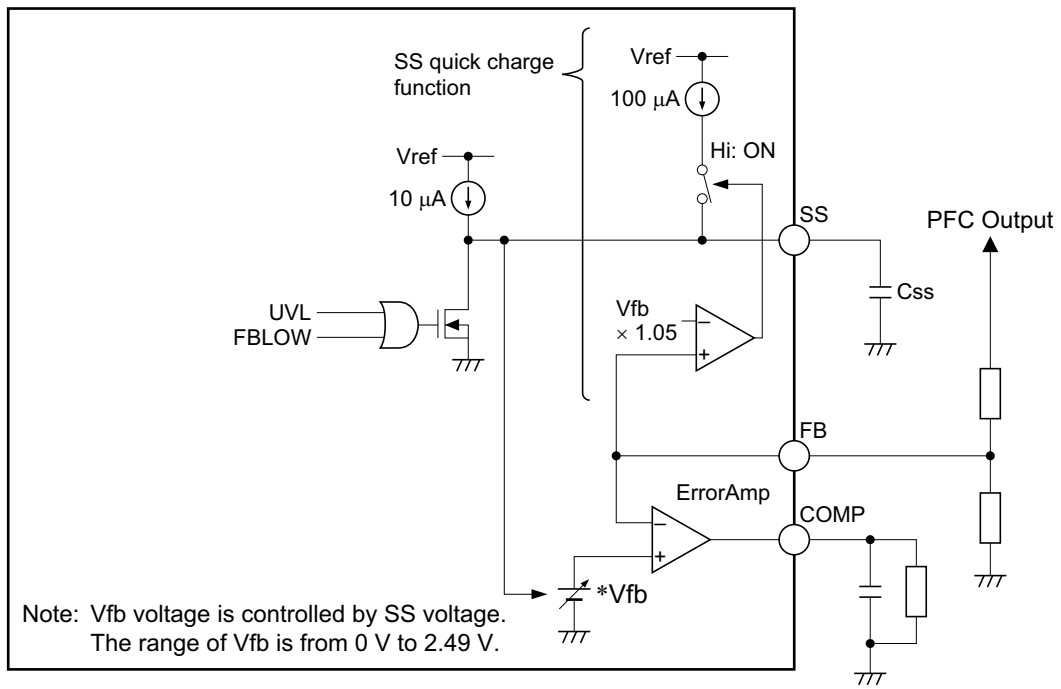


Figure 9 Soft Start Operation

### 3.6.7 ON/OFF Timer Function for Boost Diode Short (TM Function)

A large current will flow to Power MOSFET or boost inductor at boost diode short-circuit, and temperature of them will rise. TM function detects continuous over current at boost diode short-circuit and prevent them heat by limited switching operation.

TM function is enabled to add a timing capacitor  $C_{tm}$  in TM pin. If it is not necessary, TM pin is connected to GND.

(1) Normal operation:

TM pin discharge  $C_{tm}$  by  $I_{snk-tm1} = 45 \mu A$  from  $C_{tm}$ .

(2) Continuous OCP detection (boost diode short-circuit case):

TM pin is charge  $C_{tm}$  by  $I_{src-tm} = -45 \mu A$  to  $C_{tm}$ . Temporary OCP situation, IC goes back status (1).

When TM pin voltage reaches 3.6 V in continuous OCP situation, IC goes to status (3).

(3) TM pin is charged up to 3.6 V

GD pulse is stopped, and TM pin discharge  $C_{tm}$  by  $I_{snk-tm2} = 5 \mu A$  typ. until its voltage reaches 1.4 V. This will be longer off time period to prevent heat.

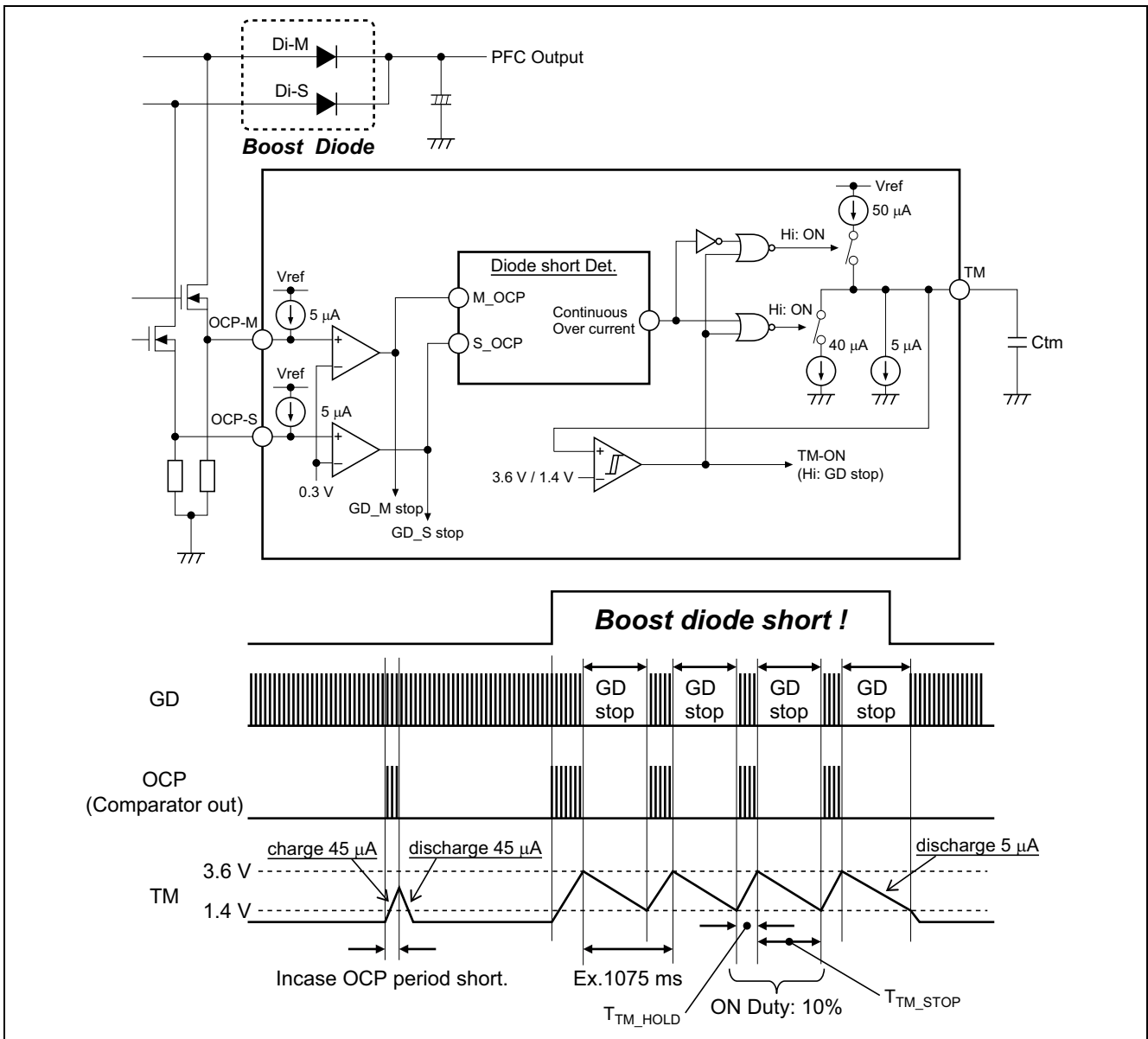


Figure 10 TM Operation

### 3.6.8 TM Function's Advanced Setting

Default ON duty is 10% when TM function uses only capacitor.

When 10% ON duty is not enough to keep temperature rise, ON duty can be adjusted by additional resistor ( $R_{tm}$ ) between TM pin and VREF pin.

When  $R_{tm}$  is used, its value must be over  $1\text{ M}\Omega$ , and our recommendation value is  $2\text{ M}\Omega$ .

If the value is under  $1\text{ M}\Omega$ , there is possibility that GD switching is not restarted after TM pin voltage reaches  $3.6\text{ V}$  at once because charge current is over TM pin current ( $I_{snk-tm2}$ ) so that TM pin cannot reach to  $1.4\text{ V}$  again.

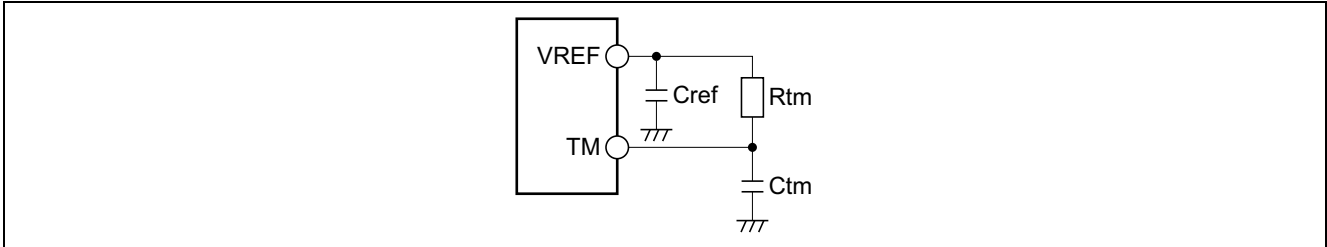


Figure 11 Location of Adding  $R_{tm}$  Resistor

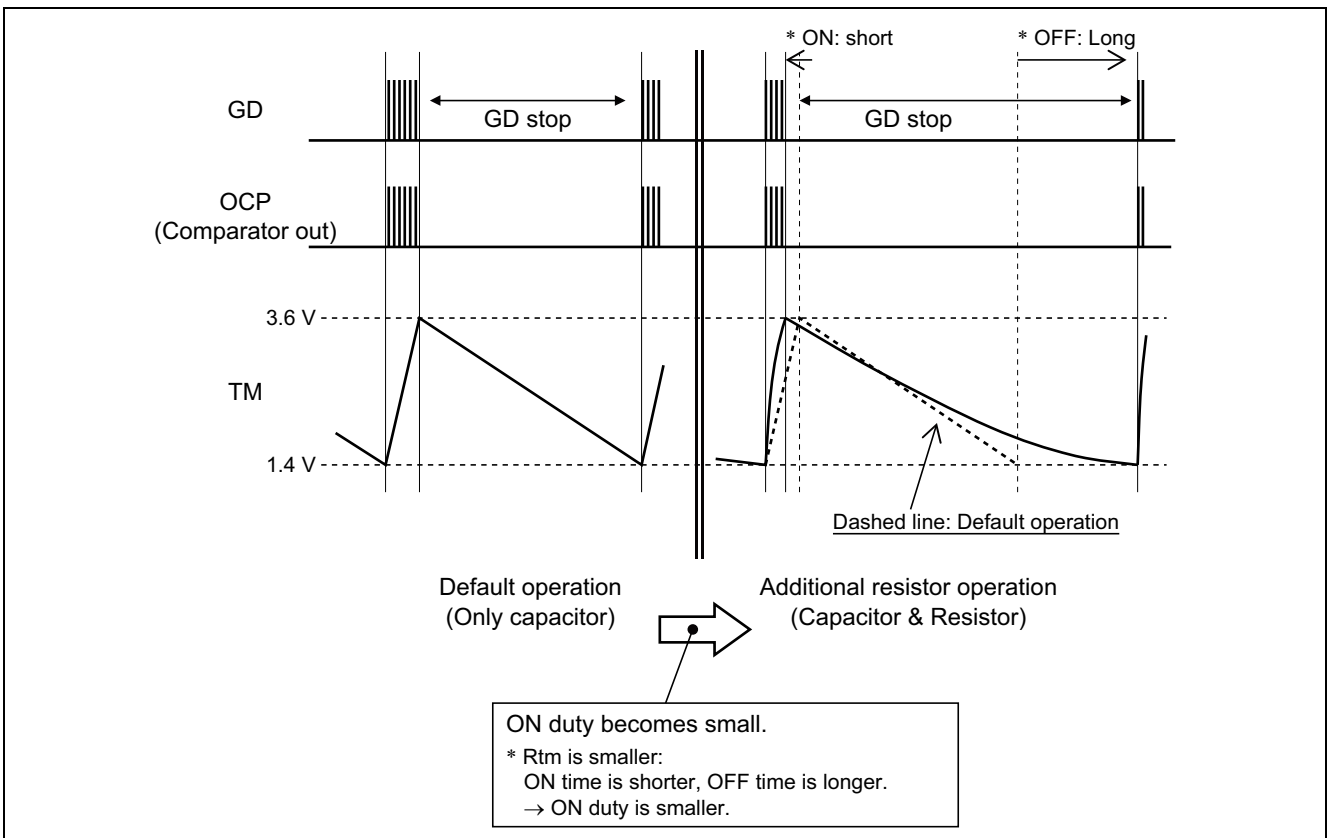


Figure 12 Duty Adjustment by TM Resistor  $R_{tm}$

## 4. Design Guide

Note: "R2A20112A Design-Tool" of excel is available.

### 4.1 PFC Output Voltage

PFC output voltage  $V_o$  is controlled that FB pin input voltage becomes the same as the internal reference voltage  $V_{fb}$  (2.49 V). PFC output voltage is obtained by Equation (1).

PFC output voltage setting should be higher than AC input voltage crest value. In addition, please input a capacitor between FB pin and GND to prevent malfunction by noise. OVP and UVP values are set according with PFC output voltage. Then, it is impossible to set them separately.

$$V_o [V] = \frac{V_{fb}}{R_{FB2}} \times R_{FB1} + V_{fb} \quad (1)$$

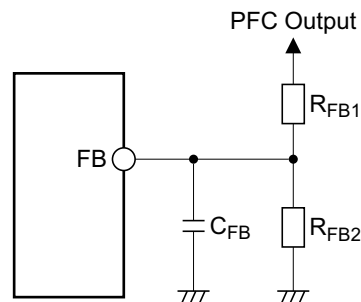
$V_o$  [V]: PFC output voltage

PFC output abnormal voltage detection:

$$V_{DOVP} = V_o \times 1.05 [V]$$

$$V_{SOVP} = V_o \times 1.09 [V]$$

$$V_{DUVP} = V_o \times 0.93 [V]$$



### 4.2 Output Capacitor

The required capacitor value to guarantee voluntary hold-up time\* is calculated by the next Equation (2).

\*Example: AC line drop, AC power off etc.

$$C_o [F] \geq \frac{2 \times P_o \times t_{hold}}{V_o^2 - V_{omin}^2} \quad (2)$$

$t_{hold}$  [s]: Hold-up time

$V_{omin}$  [V]: Minimum output voltage

$P_o$  [W]: Maximum output power

### 4.3 Boost Inductor

The boost inductor value is determined by an output power and a minimum switching frequency.

A minimum switching frequency must become over 20 kHz which is audio frequency to avoid audio noise of an inductor or an input capacitor. Generally it is around 50 kHz.

The boost inductor value is obtained by Equation (3). A conduction loss  $\eta$  input around 0.9.

$$L [H] = \frac{V_{ACLow}^2 \times \eta}{f_{SWLow} \times V_o \times I_{omax} \times \left( 1 + \frac{\sqrt{2} \times V_{ACLow}}{V_o - \sqrt{2} \times V_{ACLow}} \right)} \quad (3)$$

$L$  [H]: Boost inductance

$V_{ACLow}$  [V]: Effective value of minimum AC input voltage

$f_{SWLow}$  [Hz]: Minimum switching frequency

$I_{omax}$  [A]: Maximum output current

#### 4.4 ZCD Auxiliary Winding

ZCD pin voltage in auxiliary winding has to be more than ZCD threshold voltage. It will become minimum when AC input voltage is maximum and is obtained by Equation (4).

$$N_{aux} = \frac{V_{zcd} \times N_p}{V_o - \sqrt{2} \times V_{ACmax}} \quad (4)$$

The following are substituted for  $V_{zcd}$  in the Design tool.

$$V_{zcd} = V_{zcd-lo\_max} + Hys_{zcd\_max} = 1.6 \text{ V} + 410 \text{ mV} = 2.01 \text{ V}$$

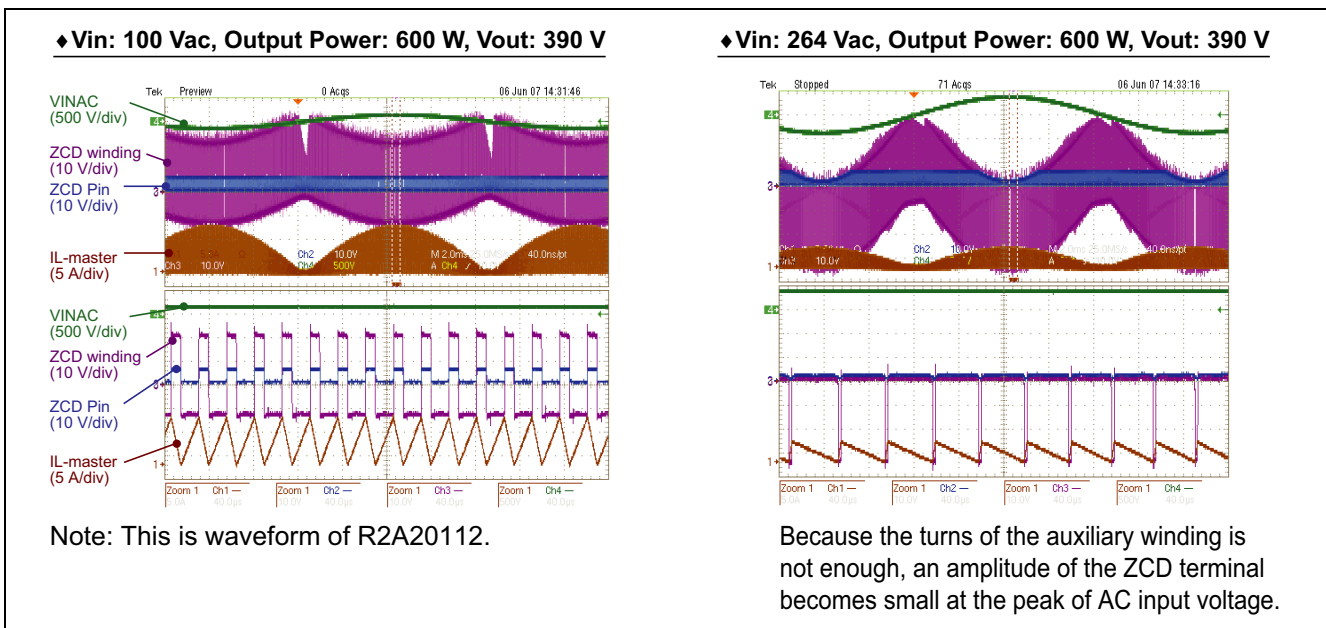
#### Regarding the audio noise of the inductor and the Restart operation in case that AC input voltage is high.

When the AC input voltage exceeds the PFC output voltage, the current that flows directly from AC input to PFC output occurs. In this case, the IC operates with the restart operation because zero current is not detected by ZCD auxiliary winding.

Also, when the AC input voltage is high voltage, the voltage of the both ends of the inductor becomes low voltage. Therefore, if the turns of ZCD auxiliary wiring is not enough, the IC operates the restart operation because the input voltage of the ZCD terminal does not exceed the threshold voltage ( $V_{zcd}$ ).

The input voltage that the IC operates restart operation depends on the ripple voltage of the PFC output voltage or the phase shift of the ripple voltage of the PFC output and the input voltage. Therefore, the input voltage that begins to operate with the restart operation raise by the higher output voltage setting or enlarging the output capacitor value to reduce ripple voltage.

Also, when the restart operation continues, the audio noise of the inductor etc. may occur by restart cycle 280  $\mu$ s (3.6 kHz).



#### 4.5 ZCD Input Resistor $R_{ZCD}$

The maximum ratings of ZCD pin current is  $\pm 3$  mA. So,  $R_{ZCD}$  is selected with 3 mA and under.  $R_{ZCD}$  is obtained by Equation (5).

$$R_{ZCD} [\Omega] = \left[ V_o \times \frac{N_{aux}}{N_p} \right] / I_{ZCD} \quad (5)$$

The following are substituted for ZCD pin current in the Design tool.

$$R_{ZCD} : I_{ZCD} = 1 \text{ mA}, R_{ZCD\_min} : I_{ZCD} = 3 \text{ mA}$$

#### 4.6 Current Calculation for Power MOSFET and Boost Diode

Peak current flowing on a Power MOSFET or a boost diode is expressed in the Equation (6). A conduction loss  $\eta$  input around 0.9.

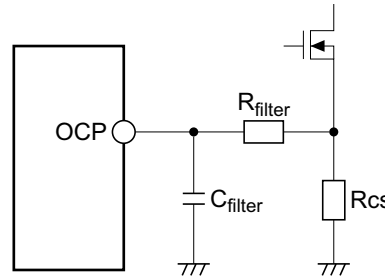
$$I_{pk} [A] = \frac{\sqrt{2} \times P_o}{\eta \times V_{ACLow}} \quad (6)$$

#### 4.7 Over Current Detection Resistor Rcs

Rcs value is obtained by Equation (7). Rcs should be selected larger value than calculated that. Rcs will be a very small resistor (ex: 10 m $\Omega$ ), so please take care pattern impedance. And it is suggested that a CR filter around 300 kHz is put on the OCP pin to avoid a switching noise.

$$R_{cs} [\Omega] = \frac{0.3 V}{I_{LIMIT}} \quad (7)$$

$I_{LIMIT}$  [A]: Over current sense value



#### 4.8 RAMP Pin Capacitor

The maximum on time  $t_{onmax}$  is expressed in the Equation (8). A conduction loss  $\eta$  input around 0.9.

$$t_{onmax} [s] = \frac{L \times V_o \times I_{omax}}{V_{ACLow}^2 \times \eta} \quad (8)$$

COMP pin maximum voltage is  $V_{clamp-comp}$ . So, RAMP pin capacitor  $C_{RAMP}$  is obtained by Equation (9). A conduction loss  $\eta$  input around 0.9.

$$C_{RAMP} [F] = \frac{I_{c-ramp1} \times t_{onmax}}{V_{clamp-comp} - 0.9 V} = \frac{I_{c-ramp1} \times L \times V_o \times I_{omax}}{(V_{clamp-comp} - 0.9 V) \times V_{ACLow}^2 \times \eta} \quad (9)$$

The following are substituted for  $C_{RAMP}$  setting in the Design tool.

$$I_{c-ramp1} = 55 \mu A, \quad V_{clamp-comp} = 4.2 V$$

## 4.9 Soft Start Time

Soft start function can be set a PFC output voltage rising slope by increasing of the reference voltage Vfb gradually. SS pin capacitor C<sub>SS</sub> is obtained by Equation (10).

$$C_{SS} [F] = \frac{V_o}{V_{OUT-SLOPE} \times V_{SS-END}} \times I_{C-SS} \quad (10)$$

$V_{OUT-SLOPE}$  [V/s]: Rising slope of PFC output

$I_{C-SS}$  [A]: Soft start charge current

$V_{SS-END}$  [V]: SS effect END voltage

The following is substituted for Soft start setting in the Design tool.

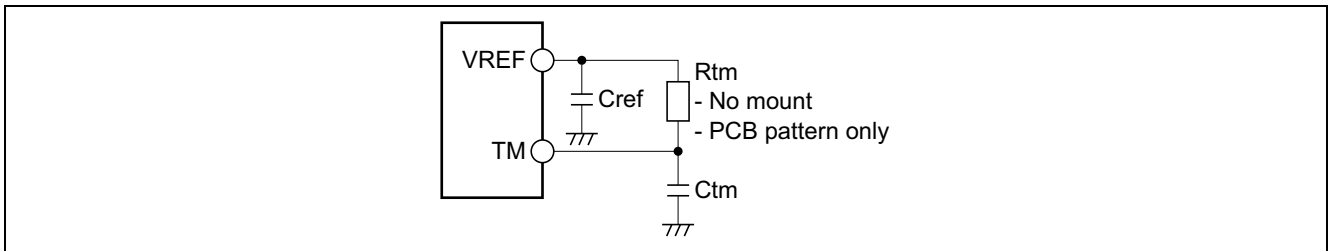
$$I_{C-SS} = 14 \mu A, \quad V_{SS-END} = 3.6 V$$

## 4.10 ON/OFF Timer Setting

Note: Timing Chart is in "3.6.8 TM Function's Advanced Setting".

TM function must not operate except the boost diode is shorted case.

Therefore, it is necessary not to be operate at Start-up, AC Line-drop and Transient-response where OCP is detected. Especially start-up is a long OCP detection period. Therefore, the TM function should not operate at start-up time. The value is 2.2  $\mu F$  to TM capacitor (C<sub>tm</sub>) of the recommendation that doesn't cause the TM operation at the start-up. In addition, preparation of the PCB pattern of the TM pin resistor (R<sub>tm</sub>) for duty adjustment is recommended.



Calculation example of TM operation:

$$T_{TM\_HOLD} = \frac{Hys\_tm \times Ctm}{|Isrc\_tm|} = \frac{2.2 V \times 2.2 \mu F}{45 \mu A} = 107.55 \text{ ms typ}$$

$$T_{TM\_STOP} = \frac{Hys\_tm \times Ctm}{|Isnk\_tm2|} = \frac{2.2 V \times 2.2 \mu F}{5 \mu A} = 968 \text{ ms typ}$$

$$T_{TM\_PERIOD} = T_{TM\_HOLD} + T_{TM\_STOP} = 1.0755 \text{ s typ}$$

$$TM_{ON \text{ duty}} = \frac{T_{TM\_HOLD}}{T_{TM\_PERIOD}} \times 100 = 10.0\% \text{ typ}$$

### 4.11 Frequency Characteristics of Error Amp (gm Amp)

The error amplifier is a transconductance amplifier (following gm amplifier). It does not need negative feedback. Therefore, it is possible to minimize influence on input circuit by a feedback circuit. Gain of gm amplifier is calculated by product of transconductance and output impedance. It is obtained by Equation (11).

G<sub>m-v</sub> is transconductance of the gm amplifier. R<sub>vo</sub> is an output resistor of the gm amplifier itself.

Outline is shown in Figure 13. When each parameters change. Gain and phase characteristics by frequency is shown in Figure 14.

$$G_V = G_{m-v} \times \frac{1}{\frac{1}{R_{vo}} + \frac{1}{R_{eo1}} + j\omega C_{eo1}} + \frac{1}{R_{eo2} + \frac{1}{j\omega C_{eo2}}} \quad (11)$$

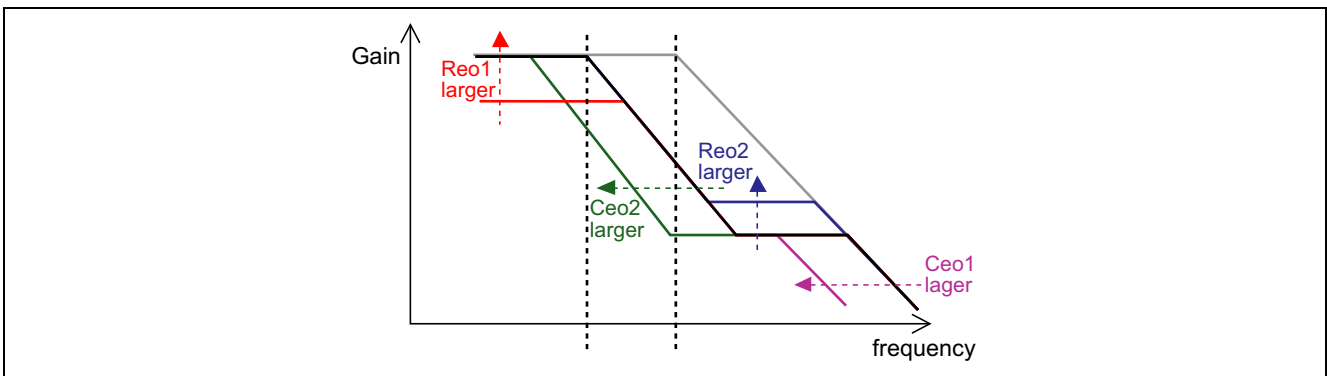
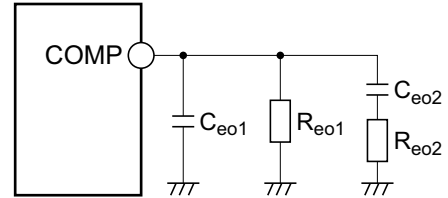


Figure 13 Outline of Gain Frequency Characteristics

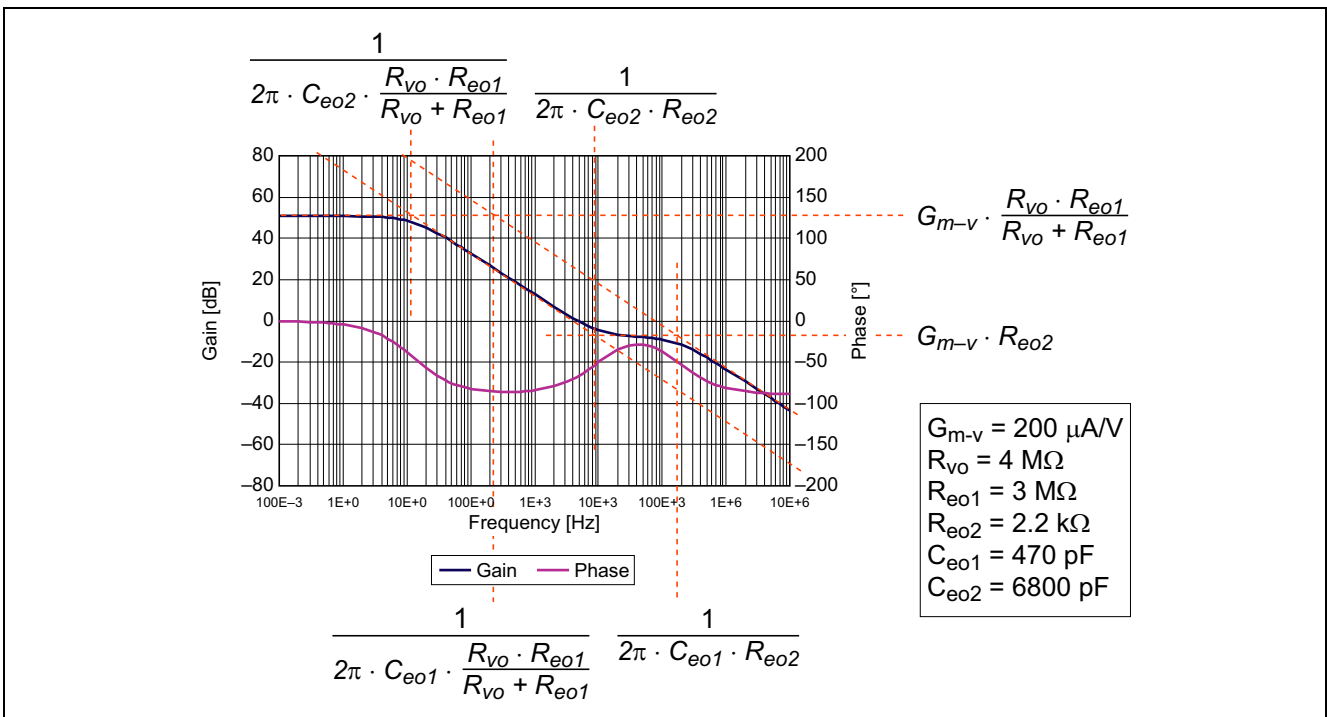


Figure 14 Frequency Characteristics of Error Amp

Please use the R2A20112A Design Tool for checking phase margin etc.



## 5. Usage Note

### 5.1 Board Layout Pattern

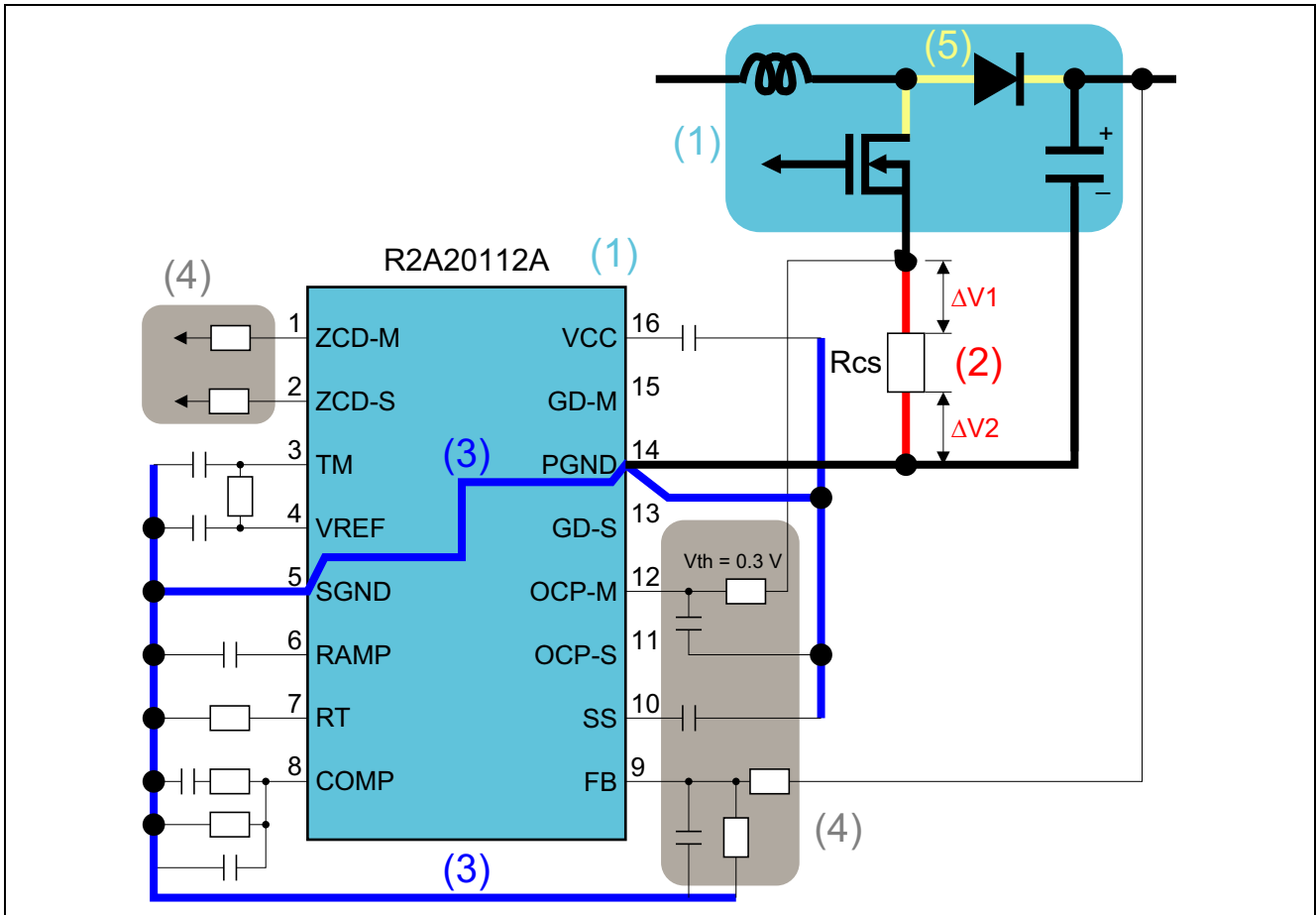


Figure 15 Design Points for Board Layout

- (1) Please make sure PFC IC is located as apart from power stage (MOSFET, Diode, Inductor) as possible. Specially please be careful to MOSFET drain line layout to avoid radiation noise.
- (2) Since  $V_{th}$  of OCP is very low (0.3 V), take care about OCP line impedance and please make  $\Delta V1$ ,  $\Delta V2$  be as small as possible (line would be shortened).
- (3) Please place COMP/VREF external parts as close to the SGND pin as possible. SGND and PGND should be connected in the shortest distance, it is best to connect under IC.
- (4) Please place the filter for OCP-M, OCP-S, ZCD resistor and FB resistor as close to the IC as possible for avoiding radiation noise.
- (5) It is possible to reduce MOSFET drain overshoot by shortening the line between MOSFET drain and cathode of the boost diode and output capacitor.

#### Other notes:

- If a clamp diode (SBD) is connected between OCP (or GD) and GND to reduce minus noise, the anode pin should be connected to output capacitor's GND point separately from IC GND. Because when the diode turns on, large current flow to the GND line of anode.

## 5.2 Remarks for World Wide AC Input

In case of W/W AC input, there is big difference between minimum and maximum AC input voltage, and it has big influence for PFC control.

In design to W/W AC input, it is necessary to use a dynamic range of Error Amp output effectively.

In CRM constant On time control, a state where a certain constant load is assumed. Figure 16 shows the relation between necessary On time and AC input voltage. The necessary On time is decreased according to the rise of AC input voltage. It means that COMP pin voltage is also decreased when AC input voltage is increasing. Because of this, the ratio of change of necessary On time to the Error Amp voltage change becomes large, and the gain of PFC becomes also large. When the gain becomes high, PFC is easy to get influence of PFC output ripple current and voltage, and PF becomes worse. To reduce this effect, it is necessary to use wide dynamic range of the Error Amp.

Specifically, RAMP capacitor value\* is fitted so that COMP voltage becomes 4.3 V typ. of clamp voltage, at minimum AC input and maximum output power.

Note: \* In Design tool, RAMP capacitor value is calculated to proper value automatically. Our proposal value is 0 to 10% larger than calculated value in Design tool. If its value is too large, characteristics get worse. On the other hand, if it is too small, maximum output power is decreased.

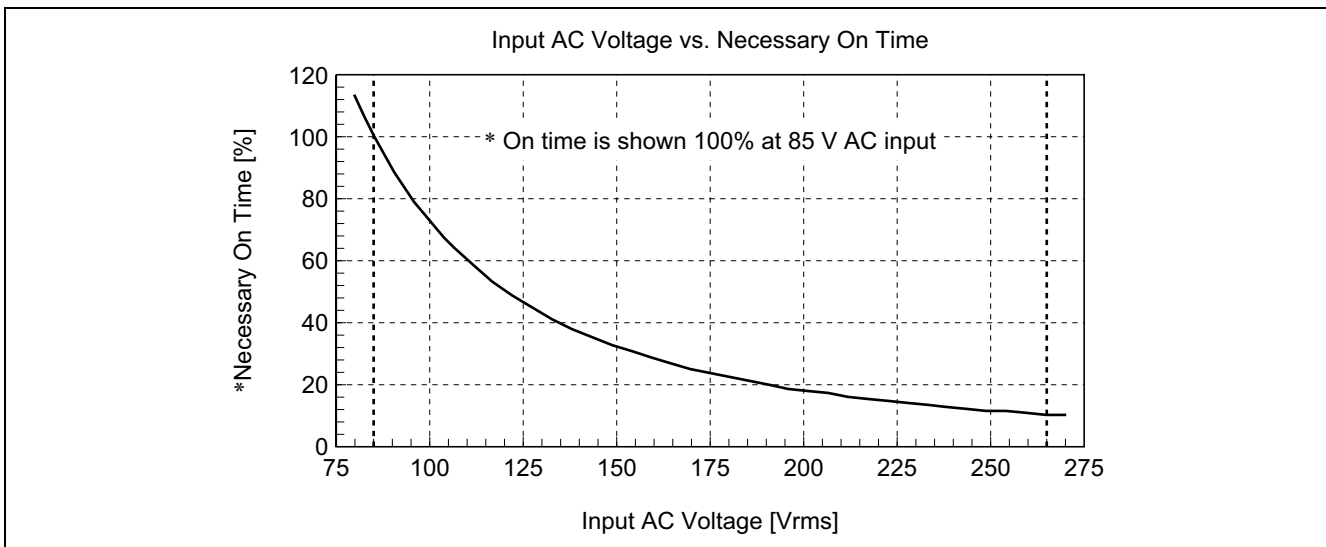


Figure 16

## Website and Support

Renesas Electronics Website

<http://www.renesas.com/>

Inquiries

<http://www.renesas.com/inquiry>

All trademarks and registered trademarks are the property of their respective owners.



## Notice

- All information included in this document is current as of the date this document is issued. Such information, however, is subject to change without any prior notice. Before purchasing or using any Renesas Electronics products listed herein, please confirm the latest product information with a Renesas Electronics sales office. Also, please pay regular and careful attention to additional and different information to be disclosed by Renesas Electronics such as that disclosed through our website.
- Renesas Electronics does not assume any liability for infringement of patents, copyrights, or other intellectual property rights of third parties by or arising from the use of Renesas Electronics products or technical information described in this document. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
- You should not alter, modify, copy, or otherwise misappropriate any Renesas Electronics product, whether in whole or in part.
- Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation of these circuits, software, and information in the design of your equipment. Renesas Electronics assumes no responsibility for any losses incurred by you or third parties arising from the use of these circuits, software, or information.
- When exporting the products or technology described in this document, you should comply with the applicable export control laws and regulations and follow the procedures required by such laws and regulations. You should not use Renesas Electronics products or the technology described in this document for any purpose relating to military applications or use by the military, including but not limited to the development of weapons of mass destruction. Renesas Electronics products and technology may not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations.
- Renesas Electronics has used reasonable care in preparing the information included in this document, but Renesas Electronics does not warrant that such information is error free. Renesas Electronics assumes no liability whatsoever for any damages incurred by you resulting from errors in or omissions from the information included herein.
- Renesas Electronics products are classified according to the following three quality grades: "Standard", "High Quality", and "Specific". The recommended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below. You must check the quality grade of each Renesas Electronics product before using it in a particular application. You may not use any Renesas Electronics product for any application categorized as "Specific" without the prior written consent of Renesas Electronics. Further, you may not use any Renesas Electronics product for any application for which it is not intended without the prior written consent of Renesas Electronics. Renesas Electronics shall not be in any way liable for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for an application categorized as "Specific" or for which the product is not intended where you have failed to obtain the prior written consent of Renesas Electronics. The quality grade of each Renesas Electronics product is "Standard" unless otherwise expressly specified in a Renesas Electronics data sheets or data books, etc.  
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; and industrial robots.  
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control systems; anti-disaster systems; anti-crime systems; safety equipment; and medical equipment not specifically designed for life support.  
"Specific": Aircraft; aerospace equipment; submersible repeaters; nuclear reactor control systems; medical equipment or systems for life support (e.g. artificial life support devices or systems), surgical implantations, or healthcare intervention (e.g. excision, etc.), and any other applications or purposes that pose a direct threat to human life.
- You should use the Renesas Electronics products described in this document within the range specified by Renesas Electronics, especially with respect to the maximum rating, operating supply voltage range, movement power voltage range, heat radiation characteristics, installation and other product characteristics. Renesas Electronics shall have no liability for malfunctions or damages arising out of the use of Renesas Electronics products beyond such specified ranges.
- Although Renesas Electronics endeavors to improve the quality and reliability of its products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please be sure to implement safety measures to guard them against the possibility of physical injury, and injury or damage caused by fire in the event of the failure of a Renesas Electronics product, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult, please evaluate the safety of the final products or system manufactured by you.
- Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please use Renesas Electronics products in compliance with all applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive. Renesas Electronics assumes no liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
- This document may not be reproduced or duplicated, in any form, in whole or in part, without prior written consent of Renesas Electronics.
- Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products, or if you have any other inquiries.  
(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.  
(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.



### SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

**Renesas Electronics America Inc.**  
2880 Scott Boulevard Santa Clara, CA 95050-2554, U.S.A.  
Tel: +1-408-588-6000, Fax: +1-408-588-6130

**Renesas Electronics Canada Limited**  
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada  
Tel: +1-905-898-5441, Fax: +1-905-898-3220

**Renesas Electronics Europe Limited**  
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.  
Tel: +44-1628-585-100, Fax: +44-1628-585-900

**Renesas Electronics Europe GmbH**  
Arcadiastrasse 10, 40472 Düsseldorf, Germany  
Tel: +49-211-65030, Fax: +49-211-6503-1327

**Renesas Electronics (China) Co., Ltd.**  
7th Floor, Quantum Plaza, No.27 ZhiChunLu Haidian District, Beijing 100083, P.R.China  
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

**Renesas Electronics (Shanghai) Co., Ltd.**  
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China  
Tel: +86-21-5877-1818, Fax: +86-21-6887-7858 / -7898

**Renesas Electronics Hong Kong Limited**  
Unit 1601-1613, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong  
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

**Renesas Electronics Taiwan Co., Ltd.**  
13F, No. 363, Fu Shing North Road, Taipei, Taiwan  
Tel: +886-2-8175-9600, Fax: +886 2-8175-9670

**Renesas Electronics Singapore Pte. Ltd.**  
1 harbourFront Avenue, #06-10, keppel Bay Tower, Singapore 098632  
Tel: +65-6213-0200, Fax: +65-6278-8001

**Renesas Electronics Malaysia Sdn.Bhd.**  
Unit 906, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia  
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

**Renesas Electronics Korea Co., Ltd.**  
11F., Samik Lavi'de' or Bldg. 720-2 Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea  
Tel: +82-2-558-3737, Fax: +82-2-558-5141