ISL9241 Operation Modes

Abstract

The ISL9241 is a Buck-Boost battery charger that supports Narrow Voltage Direct Charging (NVDC) and Hybrid Power Buck-Boost (HPBB/Bypass) operation modes. It also has special features such as Supplemental mode (Intel Vmin Active Protection), USB On-the-Go (OTG), and USB PD operation modes (by operating the charger in reverse direction). All modes are configurable by firmware. This document explains how to configure the ISL9241 to operate and transition between the different modes through SMBus and I^2C communication.

Contents

1. ISL9241 Operation Modes

The ISL9241 buck-boost charger supports several operation modes depending on battery availability and power requirements. The ISL9241 can switch between modes during system operation using only firmware. When a battery is the only power source in the system, the ISL9241 operates in Battery Only mode, consuming very little current and transferring power to the system with very high efficiency. When an adapter is plugged into the system, the ISL9241 starts up initially in NVDC mode and can be set up for other modes through firmware from a controller on the board.

ISL9241 Operation Modes:

- NVDC mode (default): see Narrow Voltage Direct Charging (NVDC) Mode
- Bypass mode with battery charging: see Bypass Mode with Battery Charging
- Reverse Turbo mode with battery charging: see Reverse Turbo Boost (RTB) Mode with Battery Charging
- Battery Only mode: see Battery Only Mode
- Supplemental mode (Intel Vmin Active Protection (VAP)): see Supplemental Mode (Intel VAP)

1.1 Narrow Voltage Direct Charging (NVDC) Mode

In Narrow Voltage Direct Charging (NVDC) mode, the power from the adapter provides power to the system loads and for battery charging. All power from the adapter passes through the power stage and the inductor. The advantage of NVDC mode is that the system voltage can be regulated near the battery voltage. This allows you to select lower voltage components for all the voltage regulators connected at the output system node, resulting in smaller size and higher efficiency in the subsequent stages. This mode is more suitable for lower power operation and for operation in Boost mode and Buck-Boost mode.

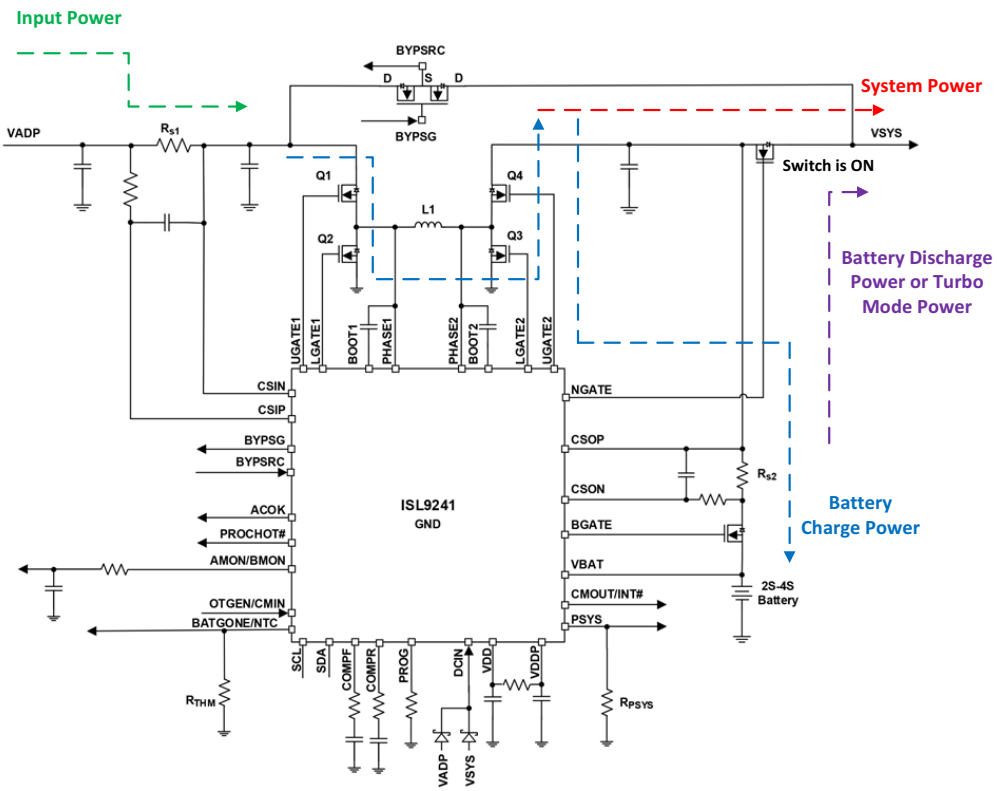

Figure 1. NVDC Operation Mode

When the system power increases, the available adapter power provides power to the system first. Any remaining power is used to charge the battery.

1.1.1 NVDC Turbo Mode

When the system power exceeds the power that can be provided by the adapter, the ISL9241 regulates the adapter current at the Adapter Current Limit value. The remaining power to the system is provided from the battery, so the adapter and the battery provide the system power together. This is called NVDC Turbo mode.

1.2 Bypass Mode with Battery Charging

When the adapter voltage is higher than the battery voltage, the ISL9241 can be operated in Bypass mode. In Bypass mode, the adapter is connected directly to the system and the system power is provided directly from the adapter. The charging and discharging power goes through the power stage and inductor.

When the available adapter power is higher than the power consumed by the system, the remaining power can be used to charge the battery. The converter switches in the forward direction, delivering power from the adapter to charge the battery. When the battery is not charging, switching can be disabled. .

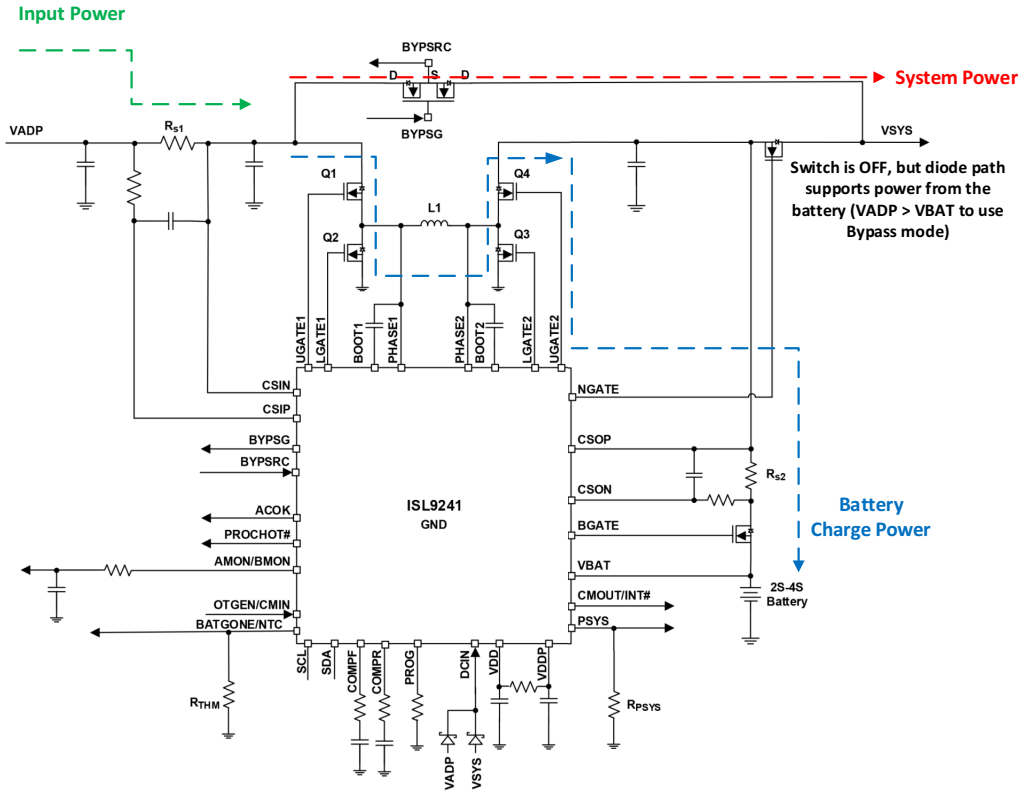

Figure 2. Bypass Mode with Battery Charging

1.3 Reverse Turbo Boost (RTB) Mode with Battery Charging

If the ISL9241 is configured to operate in Bypass mode, Reverse Turbo Boost (RTB) mode can be enabled. RTB mode is useful when the adapter alone cannot handle the peak power demands from the system. In RTB mode, the battery supplements the adapter power by operating the ISL9241 in the reverse direction.

Initially, when the system load is lower than the adapter power, all the system power is provided from the adapter. As the system load increases, the ISL9241 provides power from the adapter up to the programmed Adapter Current Limit. When the Adapter Current Limit is reached, the ISL9241 operates in the reverse direction, boosting up the power from the battery and providing the remaining needed power in addition to the adapter power. The ISL9241 can go from forward battery charging to RTB mode automatically depending on the load demand. When RTB mode is enabled, the battery FET (connected to BGATE) is always turned on.

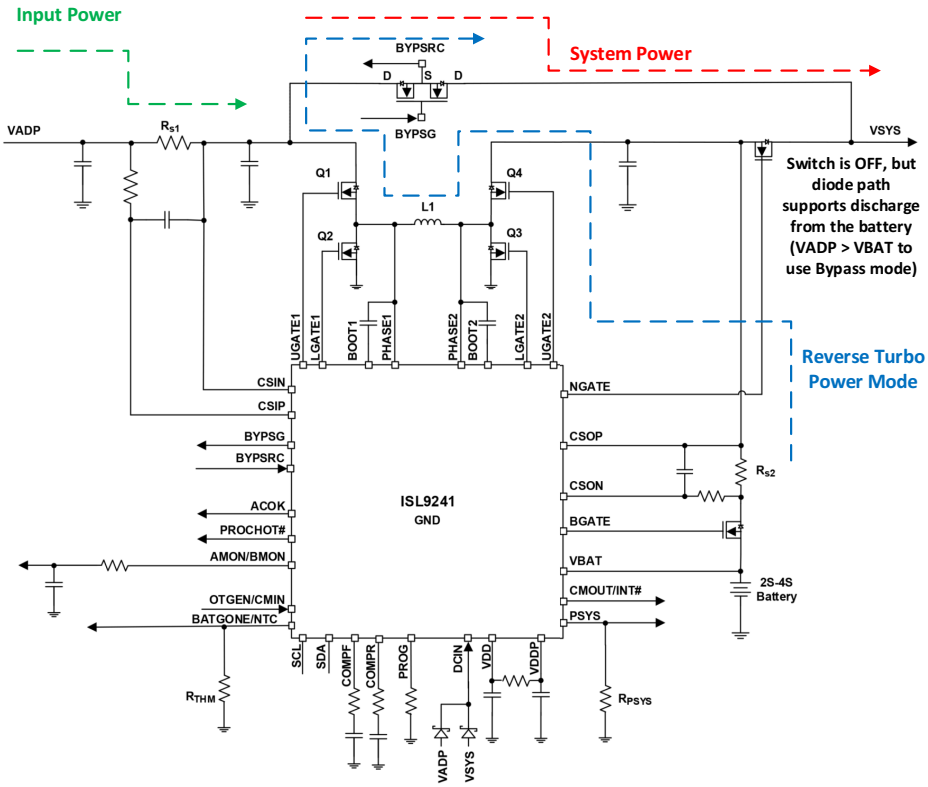

Figure 3. Reverse Turbo Boost with Battery Charging

1.4 Battery Only Mode

When no adapter is present in the system, the ISL9241 provides all system load demands directly from the battery. In this case, the system power passes only through the Battery FET and the FET connected to NGATE, so the efficiency in Battery Only mode is very high. Because the control loop and several features are not needed in Battery Only mode, these features can be turned off and the ISL9241 can operate in a low power state, consuming very little current for operation.

When the ISL9241 is operating in Battery Only mode, you can connect a battery-powered device to the USB port (adapter side). The ISL9241 can support battery-powered devices by operating in the reverse direction and providing power from the battery to the adapter terminal/USB port. This is called On-the-Go (OTG) mode, but supports USB-OTG and USB-PD. The ISL9241 can operate in Reverse Buck/Boost mode or Buck-Boost mode and provides a programmable 5V to 20V output at the USB port.

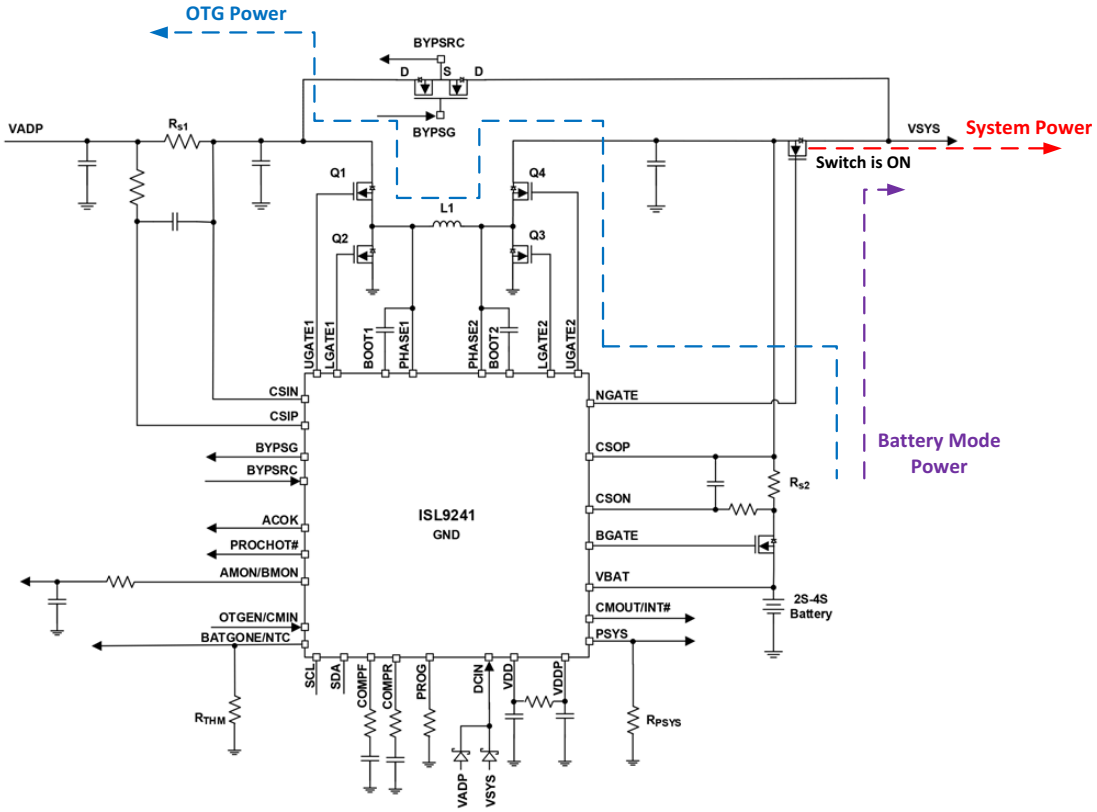

Figure 4. Battery Only Mode and OTG Mode

1.5 Supplemental Mode (Intel VAP)

Use Supplemental mode or Intel VMIN Active Protection (VAP) when the battery voltage is sufficient to provide power to the system but the impedance from the battery to the system causes a large voltage drop, limiting the power that can be drawn without crashing the system. This mode also supports rare peak power events that are higher than what the battery power can support. Use this mode when there is only a battery in the system and the adapter port is open.

When the battery voltage is high, the ISL9241 operates in reverse direction (OTG mode) and stores some energy from the battery in the input capacitors (on the adapter side) at high voltage.

If the system voltage starts falling below a threshold during a high system load event due to high battery impedance or low battery voltage, the energy from the input capacitor supplements the battery power and holds up the system voltage until the load event ends.

After receiving the command to exit the mode, the energy stored in the input capacitors can be discharged using an internal discharge path so that an external power source can be safely connected.

This mode's setup can be controlled by an external microcontroller or host controller on the system. Several parameters can be programmed to achieve the needed response from the ISL9241.

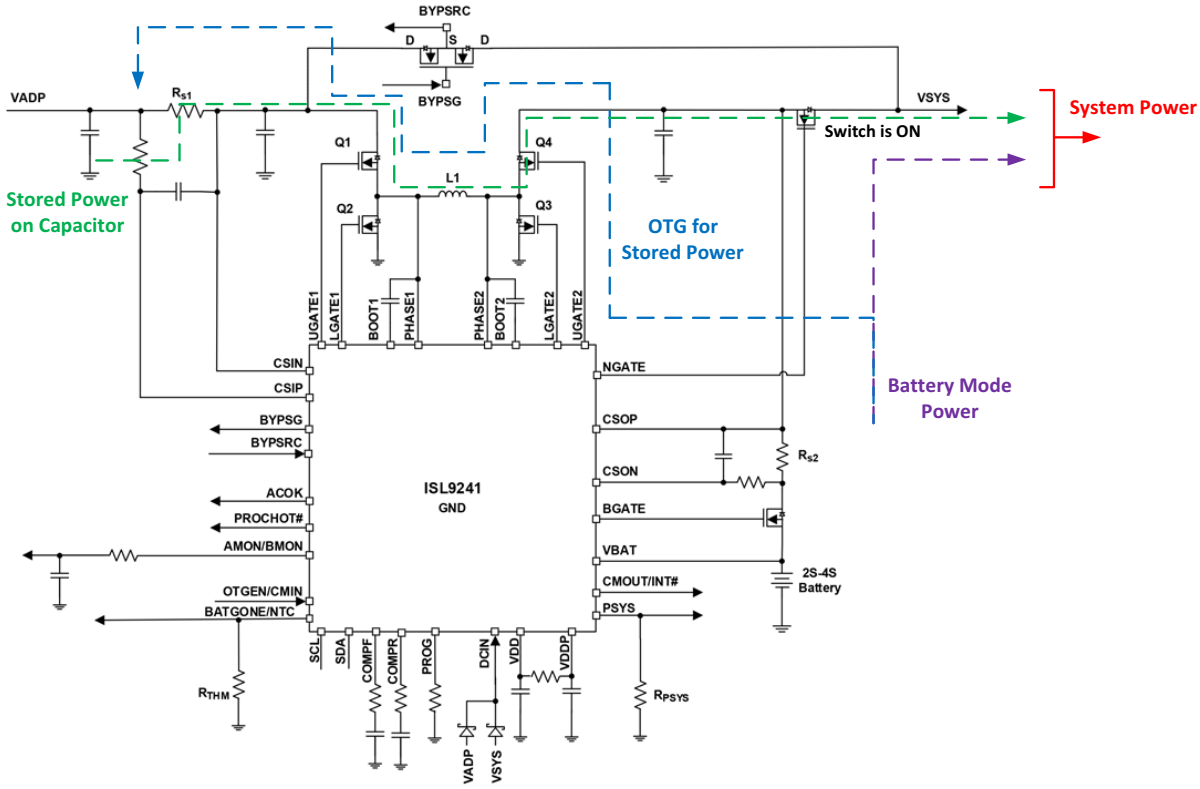

Figure 5. Supplemental Mode (Intel VMIN Active Protection)

2. Transitioning Between Modes (NVDC/Bypass/RTB)

You can use firmware commands to configure the ISL9241 to transition between the different modes. Figure 6 shows the major and minor states that the ISL9241 can operate in and the transitions between them. The commands in this document are suggestions/recommendations. You can start with these commands for your first implementation/evaluation, but you must test the commands on your system to see if the commands need to be modified for your application in your final implementation.

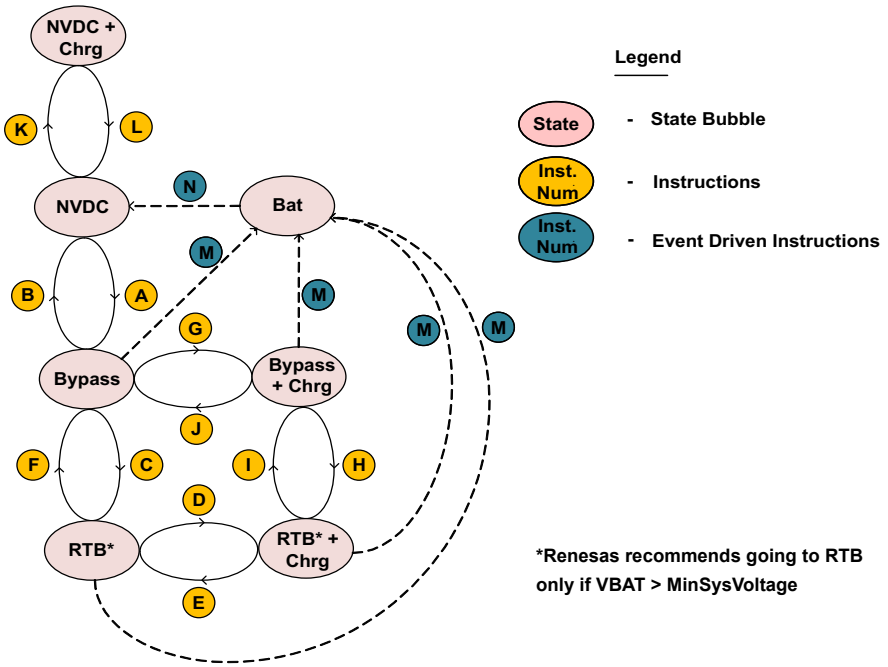

Figure 6. Transition State Diagram

Bypass State: Set up the system with the Bypass gates ON to make VSYS = VADP and allow flow of current from the adapter directly to the load. In this state, the adapter is connected directly to the system, but the ISL9241 is not switching, so the charging and reverse turbo boost functions are disabled.

(BYPSG = on, NGATE = off, BGATE = off, MaxSysV = 0, RTB bit = 0, CC = 0, MinSysV= 0)

Bypass + Charging State: The adapter is connected directly to the system (Bypass) and charging is enabled, but the turbo boost function is disabled. Use this state when the adapter can support the entire system load.

(BYPSG = on, NGATE = off, BGATE = on, MaxsysV = non-zero, RTB bit = 0, CC = non-zero, MinsysV = non-zero)

Reverse Turbo-Boost State (RTB): The Bypass gates are ON and Reverse Turbo Boost is enabled and primed to meet any load requirements. The battery can supplement the adapter to provide power in this mode. Charging is disabled.

(BYPSG = on, NGATE = off, BGATE = on, MaxsysV = non-zero, RTB bit = 1, CC = 0, MinsysV = 0)

RTB + Charging State: An extension of RTB with battery charging enabled.

(BYPSG = on, NGATE = off, BGATE = on, MaxsysV = non-zero, RTB bit = 1, CC = non-zero, MinsysV = non-zero)

Bat State: Reached when the adapter is unplugged and ACOK goes low. The system load is supported by the battery.

(BYPSG = off, NGATE = on, BGATE = on, MaxsysV = non-zero, RTB bit = 0, CC = 0, MinsysV = 0)

2.1 Transitioning from NVDC or NVDC + CHRG to Bypass

Note: To transition from NVDC mode to Bypass mode, turn off charging first. The system load must be reduced so that the ISL9241 input current never exceeds the Adapter Current Limit, ensuring smooth transition.

The output voltage of the ISL9241 is raised to the adapter voltage and the Bypass FETs are closed. When the system is connected to the adapter, NGATE is turned off to isolate the system from the output of the ISL9241. The ISL9241 output is then ramped down close to the battery voltage so that charging can be enabled safely any time. The steps in Table 1 ensure that the transition and subsequent operation are smooth.

Table 1. Transitioning from NVDC (or NVDC + CHRG) Mode to Bypass Mode

Step Number	Function Description	Register Name	Value (Decimal)	Read/ Write	Register Address
L	NVDC + CHRG to NVDC				
1	Set Charge current register to 0 to disable fast charging	ChargeCurrentLimit	0	Write	0x14
2	Set MinSysVoltage register to 0 to disable trickle charging	MinSysVoltage	0	Write	0x3E
A	NVDC to Bypass				
Preparation	Set adapter current limit to appropriate value	ACLIM	Adapter specific	Write	0x3F
Preparation	Reduce system load below ACLIM				
Preparation	Enable ADC (to read ADC values) if using it after Step2	Control 3[0]	1	Write	0x4C
1	Turn on the V_{IN}/V_{OUT} comparator so the Bypass gate turns off when the adapter is removed	Control 0[5]	1	Write	0x39
2	Set MaxsysV = VADP (from ADC or PD controller) - 2V For > 20V adapter, set to max of 18.304V	Vin ADC		Read	0x87
		MaxSysVoltage register	Vin ADC register - 2V	Write	0x15
	Three options: ▪ Wait fixed time (see Calculating Wait Time to calculate wait time) ▪ Wait fixed time and read ADC to confirm VSYS = MaxsysV register ▪ Poll ADC and check when VSYS = MaxsysV register				
3	Set ACOK reference to (800mV + ADC tolerance) higher than the battery full charge voltage (so the charger can detect and let the input ramp down during adapter removal events) and also Vin_ADC - 3V to account for ADC tolerance and I*R drop	ACOKREF	Vin_min - I*R drop (~2V) > ACOKREF > VBAT+1.1V	Write	0x40
4	Turn on Bypass gate, turn off NGATE, set Charge pumps to 100% and Enable 10mA CSOP sink	Control 0	Hex 3860	Write	0x39
5	Stop switching after 1ms (Wait time for Bypass FET to turn on)	MaxsysV register	0	Write	0x15
6	Disable 10mA discharge after waiting for CSOP to drop to VBAT, (Equation 2)	Control 0	Hex 1860	Write	0x39
7	Force Forward Buck/ Reverse Boost mode	Control 4[10]	1	Write	0x4E

Suggestions:

- If the adapter is removed at any time and ACOK goes low during Steps 1 to 3, stop executing the commands and complete steps for Bypass to BAT state.
- If the adapter is removed after Step 4, complete all steps and then execute the commands for Bypass to BAT.
- If the adapter is removed after completing all steps, first transition to Bypass state (from Bypass+Charging or Reverse Turbo Boost) and then transition to BAT state.
- CV mode regulation is not recommended in Bypass mode without Charging or Reverse Turbo boost. So enable charging and Reverse Turbo Boost along with setting MaxsysV to non-zero value.
- NGATE FET and Bypass FET power good signals can be read from the Information 1 register (0x3A) to ensure that there is no unexpected behavior in the system.
- Enable slew rate control, Control 4 [13], if output caps are high and inrush can be high to prevent protection from tripping. Capacitor can be added on Bypass gate if inrush during turn on needs to be limited.

2.2 Transitioning from Bypass to NVDC or NVDC + CHRG

Note: To transition from Bypass mode to NVDC, turn off charging and RTB mode first. The system load must be reduced so that the system current never exceeds the ISL9241 Adapter Current Limit value.

After turning off the battery FET, the ISL9241 output is ramped up to the adapter voltage. The NGATE FET is closed, connecting the output of the ISL9241 to the system. The Bypass FETs then open, isolating the adapter and the system output. The ISL9241 output and system are ramped down close to the battery voltage so that charging can be enabled safely any time. The system is regulated close to the battery voltage at the value programmed in the MaxSystemVoltage register. Complete the steps in Table 2 to transition from Bypass mode to NVDC mode or NVDC + Charge mode.

Table 2. Transitioning from Bypass Mode to NVDC (or NVDC + CHRG) Mode

Step Number	Function Description	Register Name	Value (Decimal)	Read/ Write	Register Address
B	Bypass to NVDC				
Preparation	Reduce system load below ACLIM				
1	Disable Force Forward Buck/ Reverse Boost mode	Control 4[10]	0	Write	0x4E
2	Turn off V_{IN}/V_{OUT} comparator	Control 0[5]	0	Write	0x39
3	Set MaxsysV = VADP (from ADC or PD controller) - 2V For > 20V adapter, set to max of 18.304V	Vin ADC register		Read	0x87
		MaxSysVoltage register	Vin ADC register - 2V	Write	0x15
	Three options: ▪ Wait fixed time (see Equation 3 to calculate wait time) ▪ Wait fixed time and read ADC to confirm VSYS = MaxSysVoltage register ▪ Poll ADC and check when VSYS = MaxsysV register				
4	Turn off Bypass gate, turn on NGATE, set charge pumps to 100%, Enable 10mA current source	Control 0	Hex 2040	Write	0x39
5	Set MaxSysVoltage = Battery full charge voltage after 1ms	MaxSysVoltage register	Battery specific	Write	0x15

Table 2. Transitioning from Bypass Mode to NVDC (or NVDC + CHRG) Mode (Cont.)

Step Number	Function Description	Register Name	Value (Decimal)	Read/ Write	Register Address
6	Disable 10mA discharge on CSOP after 10ms (or until CSOP ramps down to MaxsysV as determined by Equation 2), set charge pumps to 2%	Control 0	Hex 0000	Write	0x39
K	NVDC to NVDC + CHRG				
1	Set MinSysVoltage to non-zero value to enable trickle charging	MinSysVoltage	Battery specific	Write	0x3E
2	Set charge current limit to non-zero value to allow charging	ChargeCurrentLimit	Battery specific	Write	0x14

2.3 Transitioning to Charging and Reverse Turbo Boost (RTB) States

When the ISL9241 has transitioned completely into Bypass mode (or NVDC mode), enable the charging and/or Reverse Turbo Boost (RTB) modes using the commands in Table 3.

Table 3. Transitioning Between Bypass Mode and Charging and Reverse Turbo Boost States

Transition	From State	To State	Step Number	Function Description	Register Name	Value (Decimal)	Register Address
C	Bypass	RTB (Reverse Turbo Boost)	1	Reduce system load below ACLIM			
			2	Enable Reverse Turbo Boost function	Control 0[0]	1	0x39
			3	Set MaxSysVoltage register to full battery charge voltage	MaxSysVoltage	Battery specific	0x15
D	RTB	RTB + CHRG	1	Set MinSysVoltage to non-zero value to enable trickle charging	MinSysVoltage	Battery specific	0x3E
			2	Set charge current limit to non-zero value to allow charging	ChargeCurrentLimit	Battery specific	0x14
E	RTB + CHRG	RTB	1	Disable fast charging	ChargeCurrentLimit	0	0x14
			2	Disable trickle charging	MinSysVoltage	0	0x3E
F	RTB	Bypass	1	Reduce system load below ACLIM			
			2	Disable switching	MaxSysVoltage	0	0x15
			3	Disable reverse turbo boost function	Control 0[0]	0	0x39

Table 3. Transitioning Between Bypass Mode and Charging and Reverse Turbo Boost States (Cont.)

Transition	From State	To State	Step Number	Function Description	Register Name	Value (Decimal)	Register Address
G	Bypass	Bypass+ CHRG	1	Set MinSysVoltage to a non-zero value to enable trickle charging	MinSysVoltage	Battery specific	0x3E
			2	Set charge current limit to a non-zero value to allow charging	ChargeCurrentLimit	Battery specific	0x14
			3	Set MaxSysVoltage register to full battery charge voltage	MaxSysVoltage	Battery specific	0x15
H	Bypass + CHRG	RTB+ CHRG	1	Reduce system load below ACLIM			
			2	Enable Reverse Turbo Boost function	Control 0[0]	1	0x39
I	RTB + CHRG	Bypass+ CHRG	1	Reduce system load below ACLIM			
			2	Disable reverse turbo boost function	Control 0[0]	0	0x39
J	Bypass + CHRG	Bypass	1	Disable switching	MaxSysVoltage	0	0x15
			2	Disable fast charging	ChargeCurrentLimit	0	0x14
			3	Disable trickle charging	MinSysVoltage	0	0x3E

2.4 Adapter Removal Events

When the ISL9241 operates in NVDC mode, it can automatically detect adapter removal and operate in Battery Only mode independently. When the ISL9241 is in Bypass mode (with or without charging and Reverse Turbo Boost), it can detect the adapter removal event and automatically turn off the bypass FETs. Additional commands from the host controller are needed to turn on the NGATE FETs so the device can deliver full power from the battery with minimal voltage drop and loss. The following commands from the host also ensure that the Bypass FETs are not automatically turned on when the adapter is plugged in the next time (for example, a low-voltage adapter that cannot support Bypass mode).

Table 4. Adapter Removal Events[1]

Transition	From State	To State	Step #	Function Description	Register Name	Value (Decimal)	Register Address
M	Bypass/ Bypass+Chrg/ RTB/ RTB+Chrg	BAT		Monitor ACOK – when ACOK goes low, complete the following steps before connecting another adapter			
			1	Disable Force Forward Buck/Reverse Boost bit	Control 4[10]	0	0x4E
			2	Set Charge current register to 0 to disable fast charging (Optional for transitioning from Bypass/ RTB state)	ChargeCurrentLimit	0	0x14
			3	Set MinSysVoltage register to 0 to disable trickle charging (Optional for transitioning from Bypass/ RTB state)	MinSysVoltage	0	0x3E
			4	Turn off BYPSG, Turn on NGATE, Disable Charge pump 100% and disable V_{IN}<V_{OUT} comparator	Control 0	0	0x39
			5	Set MaxSysVoltage register to full charge voltage (Optional for transitioning from Bypass+Chrg/RTB/RTB+Chrg state)	MaxSysVoltage	Battery or system specific	0x15
			6	Disable ADC	Control 3[0]	0	0x4C
			7	BGATE to Normal operation	Control 1[6]	0	0x3C
			8	Reset ACOKref register to normal value to detect low voltage (5V or 9V) adapter during next plug-in event	ACOKREF	3.6V or required level	0x40
N	BAT	NVDC		Monitor ACOK – when ACOK goes High, automatically transition to NVDC	-	-	-

1. The register values shown are an example. Modify these values for your platform.

2.5 Calculating Wait Time

The following sections provide expressions to calculate the wait time for a given platform.

2.5.1 Calculating Time to Charge VSYS Node Before Turning on Bypass Gate

Before enabling the Bypass gates, the VSYS output must be almost equal to VADP to avoid any large current shoot-through that can damage bypass gates. The MaxSysVoltage register must be set to VADP – [safe margin]. VSYS is then ramped up. The time to proceed to the next step can be determined in several ways. You can use a fixed wait time or use the ADC to check when VSYS reaches VADP – [safe margin]. To calculate the fixed wait time, note that the VSYS ramp rate is usually limited by the adapter current loop. The estimated ramp time can be determined by Equation 1:

(EQ. 1) $$T = \frac{C_{OUT}}{VADP \times ILIM} \times \left(\frac{VSYS^2(final) - VSYS^2(initial)}{2} \right)$$

Renesas recommends setting the fixed wait time to twice the T value to account for approximations. Set the safe margin to around 1% of the VADP voltage avoid any gain errors that can cause the output to be higher than the set value. Lower values can result a higher current event because the Bypass FET has a low $r_{DS(ON)}$. **Note**: the MaxSystemVoltage register is limited to a maximum output of 18.304V.

2.5.2 Calculating Wait Time to Allow CSOP to Discharge to VBAT

A 10mA discharge current is applied on the CSOP pin. This implies the time taken to discharge is:

(EQ. 2) $$T = \frac{C_{CSOP} \times (V_{CSOP} - V_{BAT})}{I_{DISCHARGE}}$$

2.5.3 Calculating Time to Charge VSYS Node Before Turning on NGATE

The MaxSystemVoltage register is set to VADP – [safe margin]. This is again done to avoid high current events while turning NGATE FET on. The MaxSystemVoltage register is limited to a max output of 18.304V. To determine if the output voltage has ramped up to the correct value, use a fixed wait time (or ADC poll). Use Equation 3 to calculate the time:

(EQ. 3) $$T = \frac{C_{CSOP}}{VADP \times ILIM} \times \left(\frac{V_{CSOP}^{\ 2}(final) - V_{CSOP}^{\ 2}(initial)}{2} \right)$$

Renesas recommends setting the fixed wait time to twice the T value to account for approximations.

3. Transitioning to OTG Mode

You can transition to OTG mode from Battery Only mode two ways:

- If the General purpose comparator is enabled, use the Enable OTG mode control bit (Control1[11]) to enable OTG mode (the OTGEN pin and Supplemental mode bit are “do not care” conditions in this case)
- If the General purpose comparator is disabled, turn on the OTGEN pin and enable the OTG mode control bit (Control1[11]) to turn on OTG mode. Ensure the Supplemental mode bit is disabled

4. Transitioning to Supplemental Mode (Intel VAP)

4.1 Entering Supplemental Mode

Complete the following steps to enter Supplemental mode from Battery Only mode.

1. Set the OTGEN pin to high.
2. Set the Charge current limit to 1A (or a calculated value).
3. Disable the general purpose comparator (Control 2[3]).
4. Disable the digital OV/ OTGUV. (Control 3[15])
5. Disable the analog OV. (Control 7[7])
6. Set DCHOT to 8A.
7. Set OTGVoltage to 20V.
8. Enable the Supplemental mode bit (Control 1[10]).
9. Disable Supplemental mode by disabling the Supplemental mode register bit or by setting the OTGEN pin to low.

4.2 Calculating Charge Current Limit

OTG mode has a current limit set by the OTGCurrent register. Because Supplemental mode charges the input capacitor, the current does not flow through the sense resistor so it cannot be used to control the current. Enabling Supplemental mode with 20V OTGVoltage can result in a high slew rate on the voltage and high current from the battery. To prevent battery discharge current from reducing the VSYS voltage, limit the slew on the input capacitor by limiting the battery discharge current.

The amount of battery discharge current allowed varies with battery voltage. For example, under the following hypothetical conditions, the charge current limit should be set to 2A.

Low_VSYS_PROCHOT# = 6V

V_{BAT} = 6.8V

Total impedance from battery pack to VSYS = 0.2Ω

Total battery discharge current allowed = (V_{BAT} - Low_VSYS_PROCHOT#)/Rimp = 4A

To limit the battery discharge current to 4A, set the charge current limit register to half of 4A (2A).

Because battery discharge current is more critical at low battery voltages, you can set a higher discharge current limit when the battery is high and a lower value when battery gets close to the Low_VSYS_PROCHOT# setting.

4.3 Discharging Input Capacitor Before Plugging in Adapter

There are two options to discharge the input capacitor if an adapter plug in event is detected before the adapter is connected to the ISL9241 input (before closing the back to back FETs before the ISL9241).

- Control 0[15] lets the system controller discharge the input capacitor at any time using a 10mA internal current source on the CSIN pin
- Control 0[14] automatically discharges the input capacitor using the 10mA source for 50ms if Supplemental mode is exited and the ISL9241 enters the READY state

5. Revision History

Rev.	Date	Description
3.02	Aug 22, 2023	Updated the Bypass Mode with Battery Charging section. Updated the Transitioning from NVDC or NVDC + CHRG to Bypass section. Updated the Transitioning from Bypass to NVDC or NVDC + CHRG section. Updated the Adapter Removal Events section. Updated Equations 1 and 3. Updated the Entering Supplemental Mode section.
3.01	Aug 29, 2022	Updated Table 4.
3.00	Jan 6, 2022	Applied new template. Removed Related Literature section. Updated Transitioning from NVDC or NVDC + CHRG to Bypass section. Updated Tables 1 and 2.
2.00	Jan 10, 2019	Changed the order of steps in the NVDC Mode to Bypass Mode steps. Added steps to the Adapter unplug/removal events - to set BGATE to normal operation and adjust ACOKREF in all transitions to BAT state on page 9. Added last two sentences in the first paragraph of Section 2 on page 7.
1.01	Dec 11, 2018	Corrected list of figures on page 1.
1.00	Oct 23, 2018	Initial release

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