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April 1st, 2010
Renesas Electronics Corporation

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M16C/80 Group
Protect Operation

1.0 Abstract
The following explains the protect operation.

2.0 Introduction
Operation (1) Setting “1” in the write-enable bit of system clock control registers 0 and 1 and main clock division register (PRC0) causes system clock control register 0 and 1 and main clock division register to be in write-enabled state.

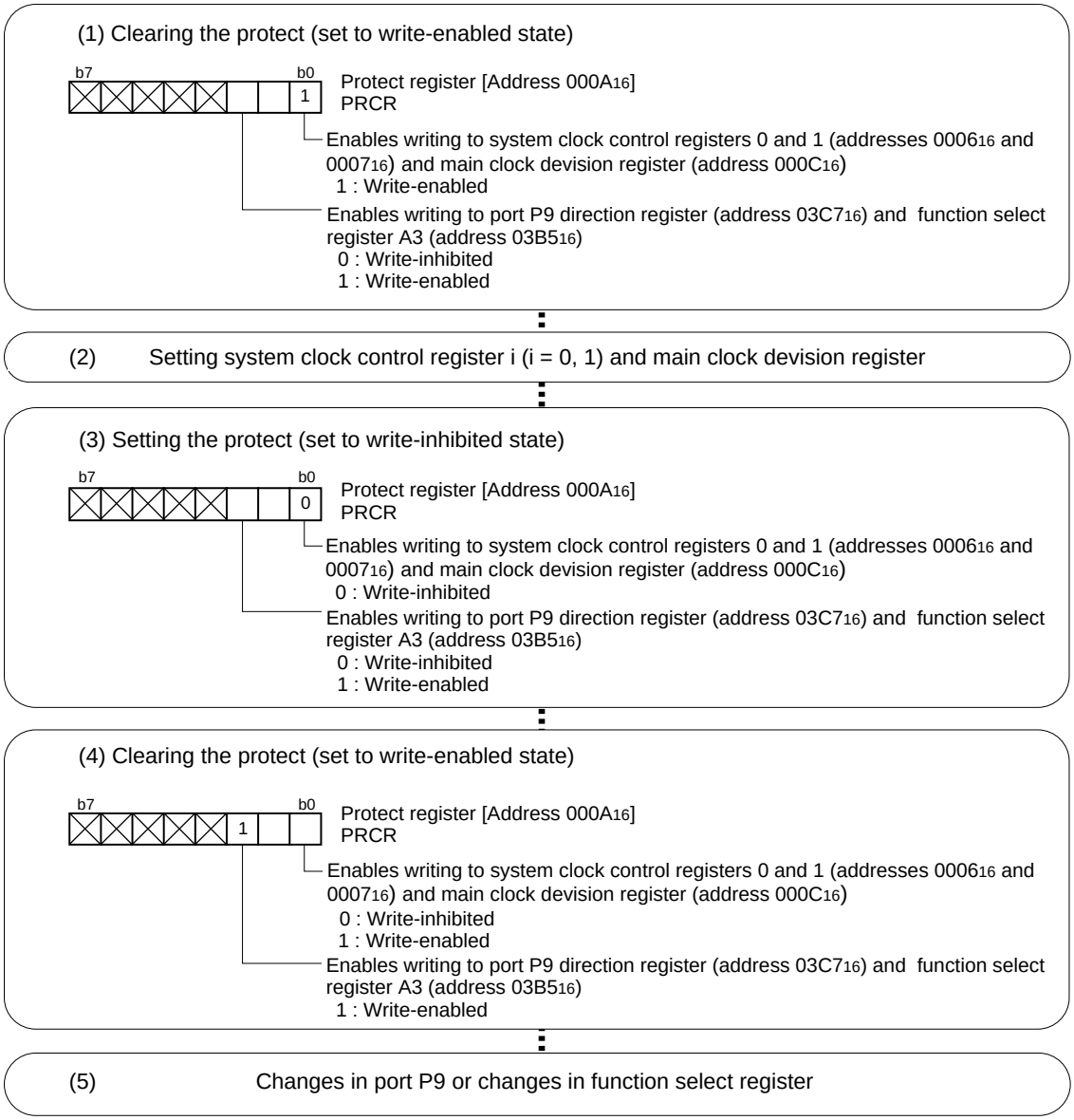
(2) The contents of system clock control register 0 and 1 and that of main clock division register are changed.

(3) Setting “0” in PRC0 causes system clock control register 0 and 1 and main clock division register to be in write-inhibited state.

(4) To change the contents of processor mode register 0 and that of processor mode register 1, follow the same steps as in dealing with system clock control registers.

(5) The write-enable bit of port 9 direction register and function select register A3 (PRC2) goes to “0” when the next write instruction is executed after write-enabled state is readied. Make changes in input/output and function select register A3 immediately after the instruction that sets “1” in PRC2 (avoid causing an interrupt). Also take measures to prevent DMA transfer from being executed.

3.0 Set-up procedure



4.0 Programming Code

```
;***************************************************************************************
;
;   M16C/80 Program Collection
;
;   FILE NAME : rjj05b0121_src.a30
;   CPU       : M16C/80 Group
;   FUNCTION  : Protect Operation
;   HISTORY   : 2003.06.16  Ver 1.00
;
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;
;***************************************************************************************
;***************************************************************************************
;       Include
;***************************************************************************************
        .LIST       OFF             ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr80100.inc    ;Reads the file that defined SFR
        .LIST       ON              ;Starts outputting lines to the assembler list file
;
;***************************************************************************************
;       Symbol definition
;***************************************************************************************
ROM_TOP         .EQU    0FFC000H    ;Start address of ROM
FIXED_VECT_TOP  .EQU    0FFFFDCH    ;Start address of fixed vector
;
M_PM0    .EQU    10000000B    ;Processor mode register 0
;                |||||++-----;Processor mode bit
;                ||||||        (00:Single-chip mode)
;                |||||+-------;R/W mode select bit
;                ||||+--------;Software reset bit
;                ||++---------;Multiplexed bus space select bit
;                ||            (Valid in microprocessor and memory expansion modes 1,2 and 3)
;                |+-----------;Reserved bit (Must always be set to "0")
;                +------------;BCLK output disable bit
;                              (1:Function set by bit 0,1 of system clock control register 0)
M_PM1    .EQU    11000000B    ;Processor mode register 1 <Flash memory version>
;                ||||||++-----;External memory area mode bit
;                ||||||        (Valid in memory expansion mode or in microprocessor mode)
;                |||||+-------;Internal memory wait bit (0:No wait state)
;                ||||+--------;Reserved bit (Must always be set to "0")
;                ||++---------;ALE pin select bit
;                ||            (Valid in memory expansion mode or in microprocessor mode)
;                ++-----------;Reserved bit (Must always be set to "1")
;                              (Rewrite this bit when the main clock is in division by 8 mode)
;
```

```
M_CM0    .EQU    00001000B    ;System clock control register 0
;                |||||++-----;Clock output function select bit (00:I/O port P53)
;                |||||+-------;WAIT peripheral function clock stop bit
;                |||||         (0:Do not stop peripheral function clock in wait mode)
;                ||||+--------;Xcin-Xcout drive capacity select bit (1:HIGH)
;                |||+---------;Port Xc select bit (0:I/O port)
;                ||+----------;Main clock (Xin-Xout) stop bit (0:On)
;                |+-----------;Watchdog timer function select bit
;                |             (0:Watchdog timer interrupt)
;                +------------;System clock select bit (0:Xin, Xout)
M_CM1    .EQU    00100000B    ;System clock control register 1
;                |||||||+-----;All clock stop control bit (0:Clock on)
;                |||++++------;Reserved bit (Must always be set to "0")
;                ||+----------;Xin-Xout drive capacity select bit
;                ||            (1:HIGH)
;                ++-----------;Reserved bit (Must always set to "0")
;
M_MCD    .EQU    00010010B    ;Main clock division register
;                |||+++++-----;Main clock division select bit (10010:No division mode)
;                +++----------;Nothing is assigned (When write, set "0")
;
;******************************************************************************
;       Program area
;******************************************************************************
;============================================================================
;       Start up
;============================================================================
        .SECTION    PROGRAM, CODE  ;Declares section name and section type
        .ORG        ROM_TOP        ;Declares start address
RESET:
;
;============================================================================
;       Protect Operation
;============================================================================
        ; Clearing the protect (set to write-enabled state)
        MOV.B    #00000011B, prcr
;                       |+---------;Enables writing to system clock control registers 0,1 and
;                       |           main clock division register (1:Write-enabled)
;                       +----------;Enables writing to processor mode register 0,1 (1:Write-enabled)
        ; Setting processor mode register
        MOV.B    #M_PM0,     pm0
        MOV.B    #M_PM1,     pm1
        ; Setting system clock control register
        MOV.B    #M_CM0,     cm0
        MOV.B    #M_CM1,     cm1
        ; Setting main clock division register
        MOV.B    #M_MCD,     mcd
        ; Setting the protect (set to write-inhibited state)
        MOV.B    #00000000B, prcr
;                       |+---------;write-inhibited (cm0,cm1)
;                       +----------;write-inhibited (pm0,pm1)
;
        MOV.B    #00H,       p9    ;Clears port P90-P97
        ; Clearing the protect (set to write-enabled state)
        MOV.B    #00000100B, prcr
;                      +-----------;Enables writing to port P9 direction register and
;                                   function select register A3
        ; Changes port P9 direction
        MOV.B    #0FH,       pd9   ;Sets P90-P93 as output port, P94-P97 as input port
        ; Clearing the protect (set to write-enabled state)
        MOV.B    #00000100B, prcr
        ; Changes in function select register A3
        MOV.B    #00H,       ps3   ;Sets Port P90-P97 as I/O port
;
```

```
MAIN:
        JMP      MAIN
;
;=============================================================================
;       Dummy interrupt processing program
;=============================================================================
dummy:
        REIT
;
;*****************************************************************************
;       Setting of fixed vector
;*****************************************************************************
        .SECTION    F_VECT, ROMDATA
        .ORG        FIXED_VECT_TOP
;
        .LWORD    dummy    ;Undefined instruction
        .LWORD    dummy    ;Overflow
        .LWORD    dummy    ;BRK instruction execution
        .LWORD    dummy    ;Address match
        .LWORD    dummy    ;
        .LWORD    dummy    ;Watchdog timer
        .LWORD    dummy    ;
        .LWORD    dummy    ;NMI
        .LWORD    RESET    ;Reset
;
        .END
```

5.0 Reference

Renesas Technology Corporation Semiconductor Home page

http://www.renesas.com/

Technical Support

E-mail: support_apl@renesas.com

Data Sheet

M16C/80 group Rev. E3
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User's Manual

M16C/80 group Rev. B
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