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M16C/64 Group

Procedure for successive serial I/O transmission/reception using the DMAC

1. Abstract

This application note presents the procedure for successive serial I/O transmission/reception using the DMAC and an example on how to use it.

2. Introduction

This application note is applied to the M16C/64 group microcomputers.

This program can be operated under the condition of M16C family products with the same SFR (Special Function Register) as M16C/64 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation.

3. Explanation of the example procedure

The example procedure selects serial I/O transmission (or reception) for the cause of request to the DMAC, and writes the next data to the transmit buffer (or reads from the receive buffer) at high speed in synchronism with the I/O transmission. This operation is performed successively as many times as the number of DMAC transfers needed.

3.1 Example connection

Figure 1 shows an example device connection for successive transmission/reception.

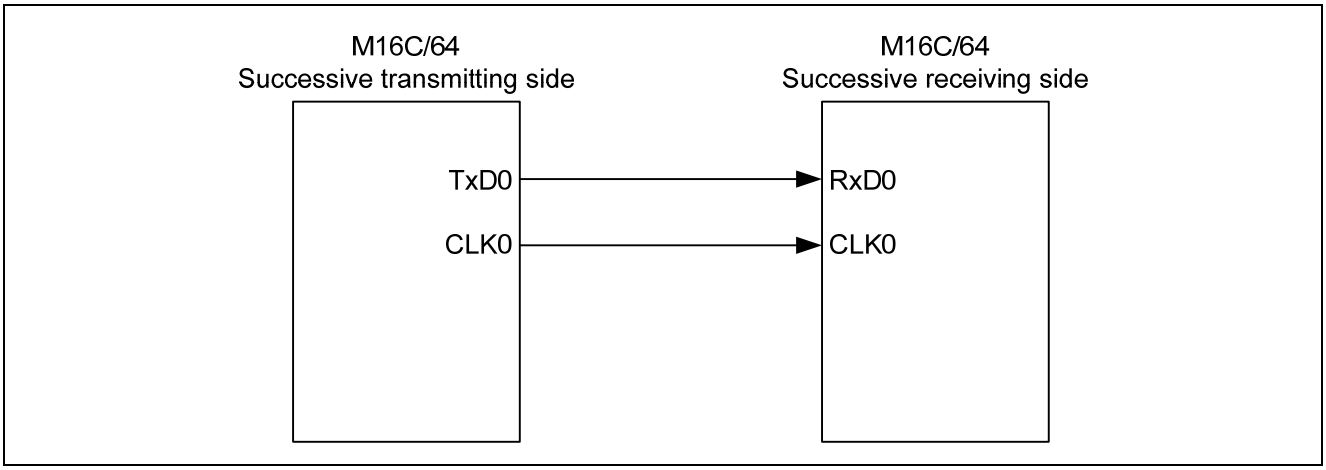


Figure 1. Example Connection for Successive Transmission/Reception

3.2 Setting-up successive transmission

The following shows how to set up the device for the case where 8 bytes of data are successively transmitted.

Usage Example:

· System

VCC1=VCC2=5.0V, XIN=16MHz

· DMAC Setting

DMA Request Factors=UART0 transfer, Single transfer, Transfer unit = 8 bits, Transfer source address direction=Forward direction, Transfer destination address direction=fixed (U0TB register)

· Serial I/O Setting

Clock synchronous serial I/O mode, BRG count source = f_{1SIO}, Bit Rates=62500bps (BRG=127), Transmit Interrupt Cause=Transmit buffer empty

Operation:

Specify UART0 transmission for the cause of request to the DMAC and after writing the first byte to the UART0 transmit buffer, transmit the remaining 7 bytes of data successively using a UART0 transmit interrupt request as a trigger. Figure 2 shows successive transmission/reception timing.

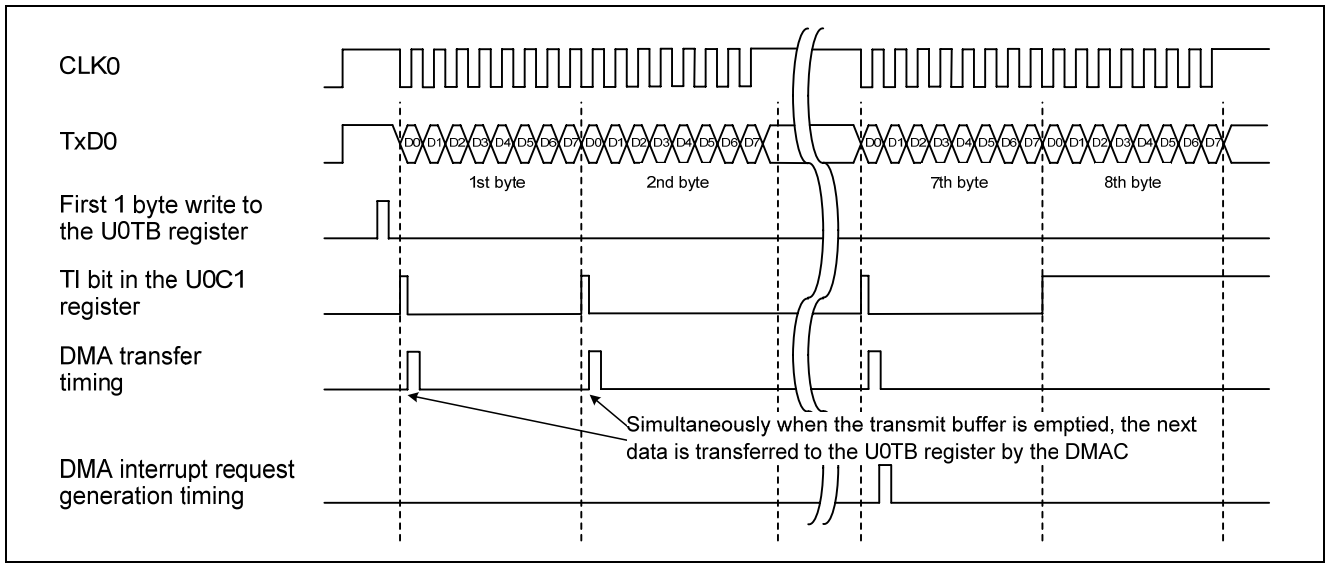
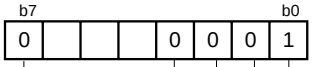


Figure 2. Successive Transmission/reception Timing

(1) Setting the serial I/O

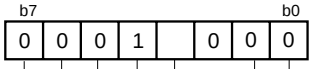
Setting UART0 transmit/receive mode register



UART0 transmit/receive mode register [Address 0248h] U0MR

Serial I/O mode select bit
b2 b1 b0
0 0 1 : Clock synchronous serial I/O mode
Internal/external clock select bit
0 : Internal clock
TxD, RxD I/O polarity reverse bit
0 : No reverse

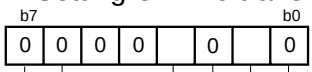
Setting UART0 transmit/receive control register 0



UART0 transmit/receive control register [Address 024Ch] U0C0

U0BRG count source select bit
b1 b0
0 0 : f_{1SIO} is selected
Transmit register empty flag
0 : Data present in transmit register (during transmission)
1 : No data present in transmit register (transmission completed)
$\overline{CTS}/\overline{RTS}$ disable bit
1 : $\overline{CTS}/\overline{RTS}$ function disabled
Data output select bit
0 : CMOS output
CLK polarity select bit
0 : Transmit data is output at falling edge of transfer clock
Transfer format select bit
0 : LSB first

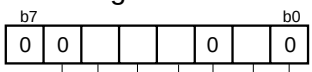
Setting UART0 transmit/receive control register 1



UART0 transmit/receive control register 1 [Address 024Dh] U0C1

Transmit enable bit
0 : Transmission disabled
Transmit buffer empty bit
0 : Data present in U0TB register
1 : No data present in U0TB register
Receive enable bit
0 : Reception disabled
Receive complete flag
0 : No data present in U0RB register
1 : Data present in U0RB register
Data logic select bit
0 : No reverse
Error signal output enable bit
0 : Output disabled

Setting UART transmit/receive control register 2

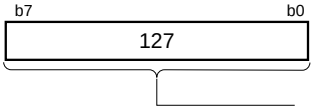


UART transmit/receive control register 2 [Address 0250h] UCON

- UART0 transmit interrupt cause select bit
  0 : Transmit buffer empty
- UART1 transmit interrupt cause select bit
- UART0 continuous receive mode enable bit
  0 : Continuous receive mode disabled
- UART1 continuous receive mode enable bit
- UART1 CLK, CLKS select bit 0
- UART1 CLK, CLKS select bit 1
- Separate UART0 $\overline{CTS}/\overline{RTS}$ bit
  0 : $\overline{CTS}/\overline{RTS}$ shared pin

Set the U0SMR register (UART0 special mode register), U0SMR2 register (UART0 special mode register 2), U0SMR3 register (UART0 special mode register 3), and U0SMR4 register (UART0 special mode register 4) to “00h”.

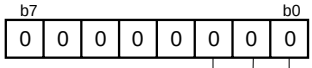
Setting UART0 bit rate register



UART0 bit rate register [Address 0249h] U0BRG

When the BRG count source = f_{1SIO} and $f(X_{IN})$ = 16MHz,
the transfer rate is $(16 \times 10^6) / 2 (127 + 1)$ = 62,500 bps

Setting UART0 transmit interrupt control register

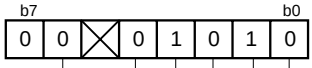


UART0 transmit interrupt control register [Address 0051h] S0TIC

- Interrupt priority level select bit
  b2 b1 b0
  0 0 0 : Level 0 (interrupt disabled)

(2) Setting the DMAC

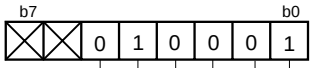
Setting DMA0 source select register



DMA0 source select register [Address 0398h] DM0SL

- DMA request source select bit
  b4 b3 b2 b1 b0
  0 1 0 1 0 : UART0 transmit
- DMA request source expansion select bit
  0 : Basic request source

Setting DMA0 control register



DMA0 control register [Address 018Ch] DM0CON

Transfer unit bit select bit
1 : 8 bits

Repeat transfer mode select bit
0 : Single transfer

DMA request bit
0 : DMA not requested

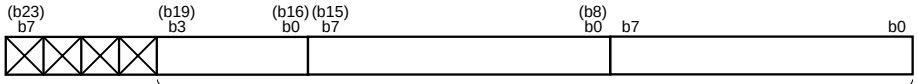
DMA enable bit
0 : Disabled

Source address direction select bit
1 : Forward (Bit 4 and bit 5 cannot be set to “1” simultaneously)

Destination address direction select bit
0 : Fixed (Bit 4 and bit 5 cannot be set to “1” simultaneously)

Setting DMA0 source pointer

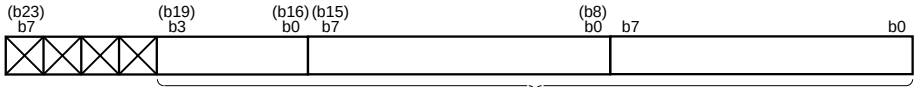
DMA0 source pointer [Address 0182h to 0180h] SAR0



Set the source address of transfer

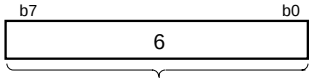
Setting DMA0 destination pointer

DMA0 destination pointer [Address 0186h to 0184h] DAR0



Set the destination address (U0TB) of transfer

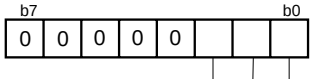
Setting DMA0 transfer counter



DMA0 transfer counter [Address 0189h to 0188h] TCR0

Since the first byte of 8-byte successive transmission is written and then transferred to the U0TB register directly (not transferred by the DMAC), set the value “6” here so that 7 bytes will be transferred by DMA

Setting DMA0 interrupt control register



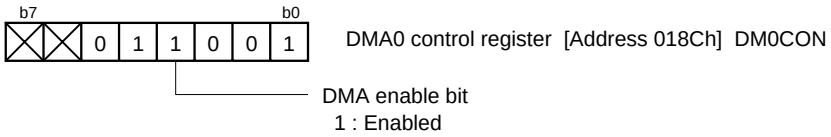
DMA0 interrupt control register [Address 004Bh] DM0IC

Interrupt priority level select bit
Set the interrupt priority level

(3) Enables interrupt (I flag = “1”)

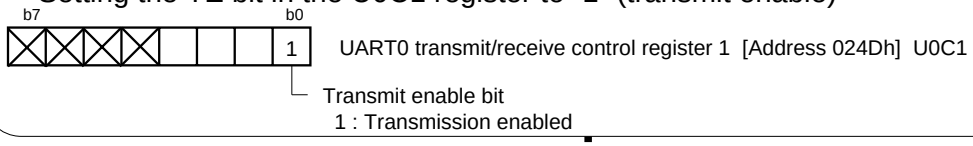
(4) Setting DMA0 control register back again (to enable DMA)

Setting DMA0 control register



(5) Enables transmit

Setting the TE bit in the U0C1 register to “1” (transmit enable)



(6) Starting successive transmissions

Write the first byte of successive transmit data to the U0TB register. Thereafter, the other bytes of data are successively transmitted by means of the DMAC transfer initiated by a UART0 transmit interrupt request until the count set in the DMA transfer counter expires.

(7) DMAC transfer complete interrupt processing

Set the DMAC transfer complete flag.

3.3 Setting-up successive reception

The following shows how to set up the device for the case where 8 bytes of data are successively received.

Usage Example:

· System

VCC1=VCC2=5.0V, XIN=16MHz

· DMAC Setting

DMA Request Factors=UART0 reception, Single transfer, Transfer unit = 16 bits (including an error flag), Transfer source address direction=fixed (U0RB register), Transfer destination address direction=Forward direction

· Serial I/O Setting

Clock synchronous serial I/O mode, External clock (Note), Continuous receive mode enabled

Note:
When the input at the CLK0 pin before data reception is high (or low if the CKPOL bit in the U0C0 register = 1), the conditions described below must be met:
- TE bit in the U0C1 register = 1 (transmission enabled)
- RE bit in the U0C1 register = 1 (reception enabled)
- U0RB register is read

Operation:

Specify UART0 reception for the cause of request to the DMAC and after a dummy read of the UART0 receive buffer, receive the data successively using a UART0 receive interrupt as a trigger. Figure 3 shows successive reception timing.

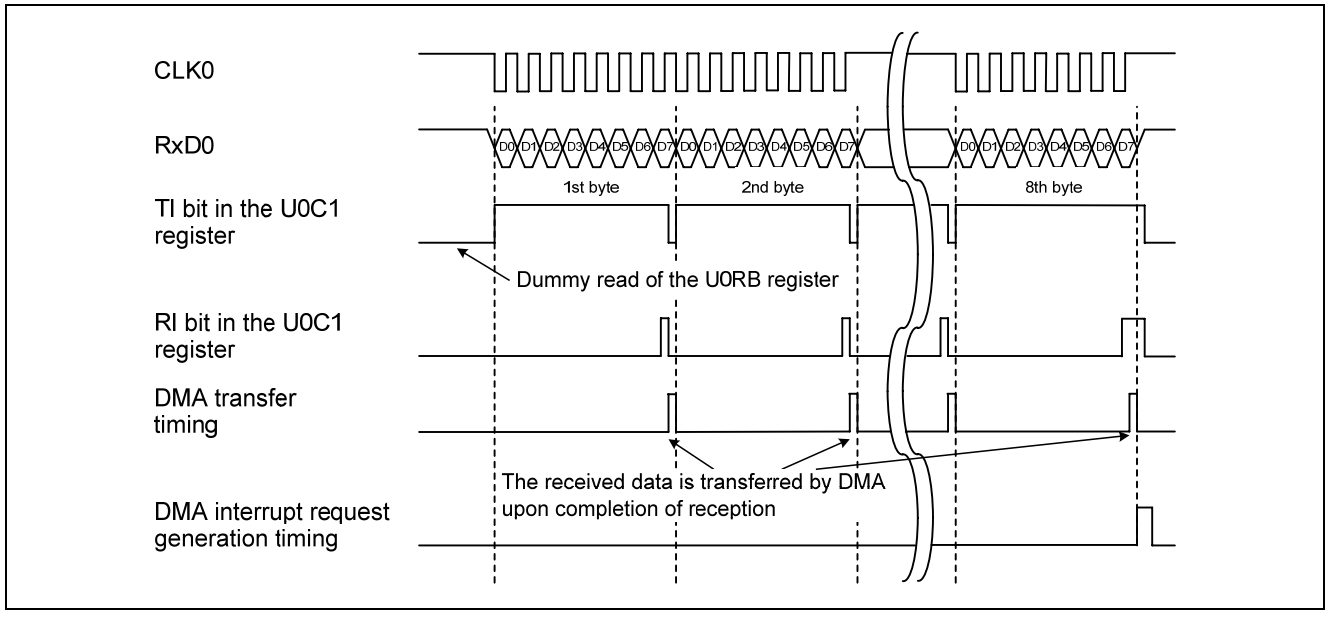
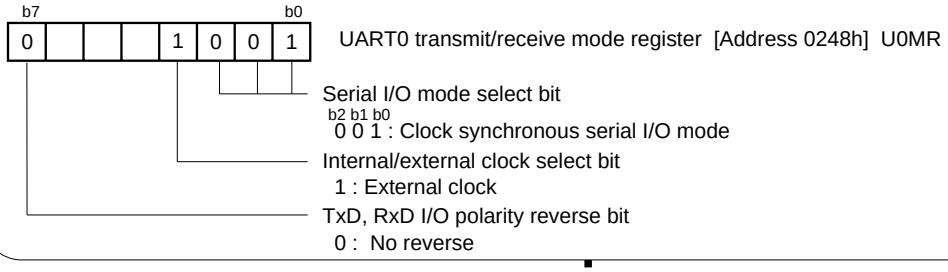


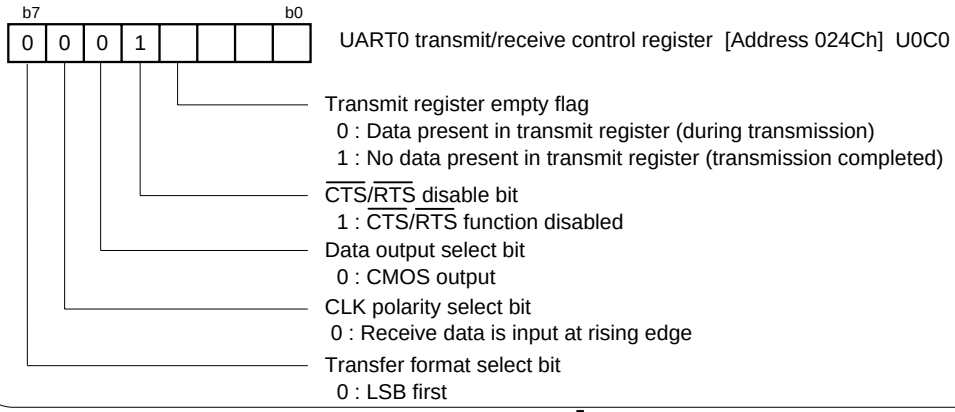
Figure 3. Successive Reception Timing

(1) Setting the serial I/O

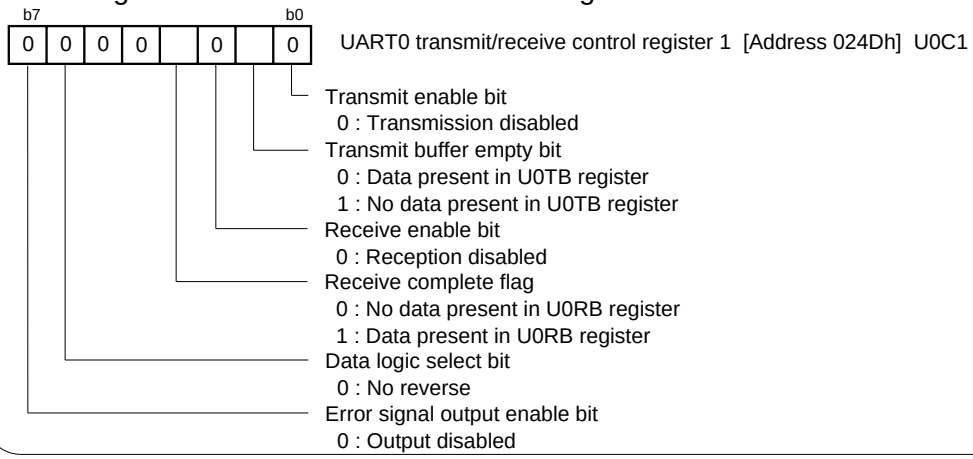
Setting UART0 transmit/receive mode register



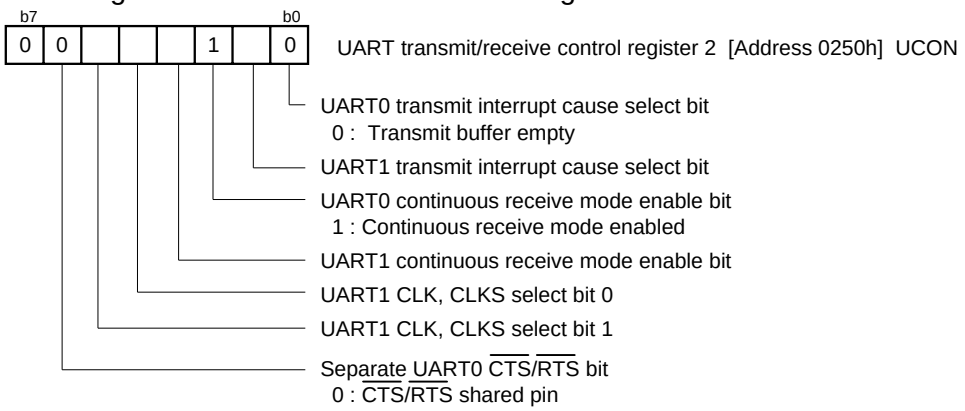
Setting UART0 transmit/receive control register 0



Setting UART0 transmit/receive control register 1

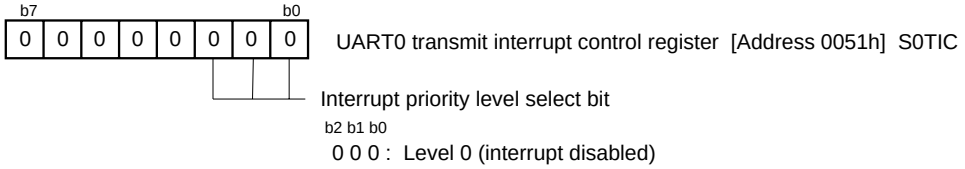


Setting UART transmit/receive control register 2



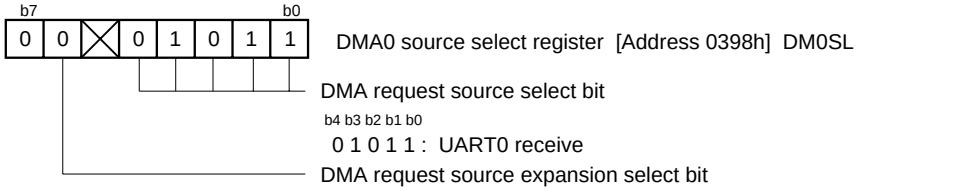
Set the U0SMR register (UART0 special mode register), U0SMR2 register (UART0 special mode register 2), U0SMR3 register (UART0 special mode register 3), and U0SMR4 register (UART0 special mode register 4) to “00h”.

Setting UART0 transmit interrupt control register

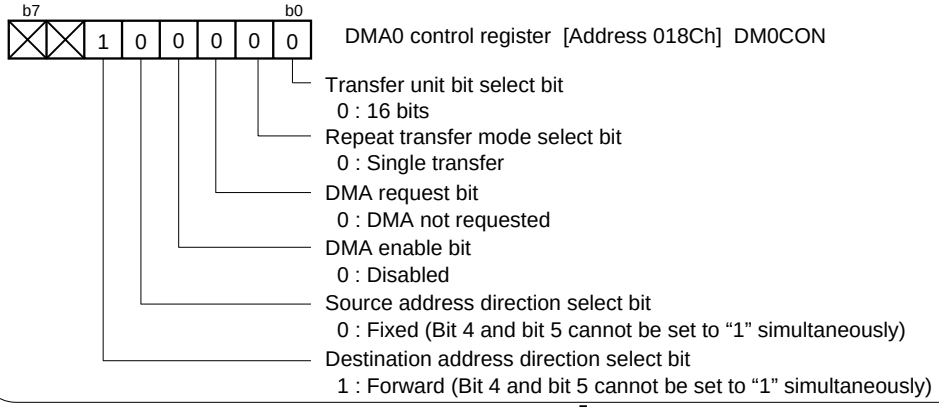


(2) Setting the DMAC

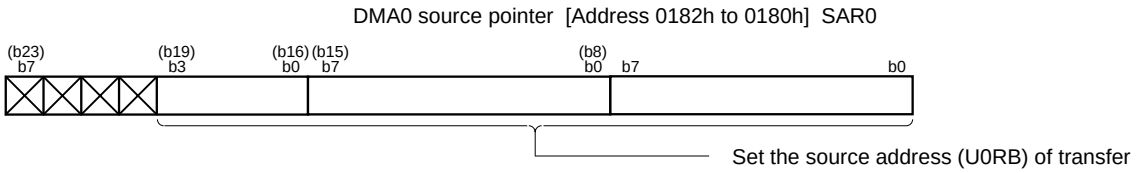
Setting DMA0 source select register



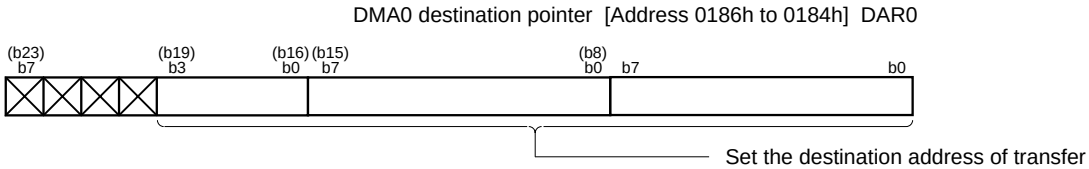
Setting DMA0 control register



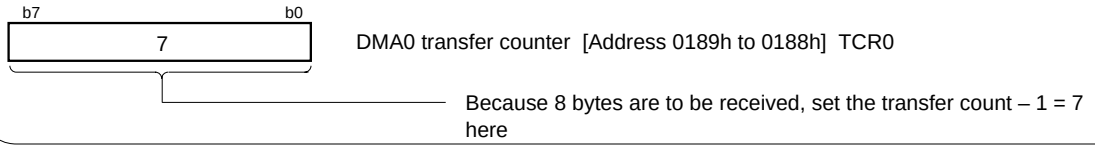
Setting DMA0 source pointer



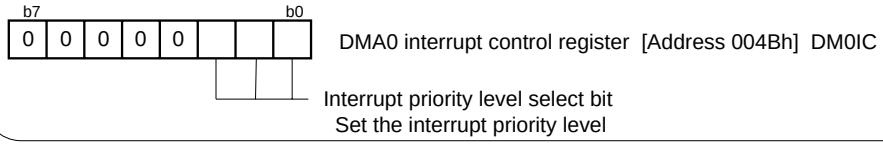
Setting DMA0 destination pointer



Setting DMA0 transfer counter



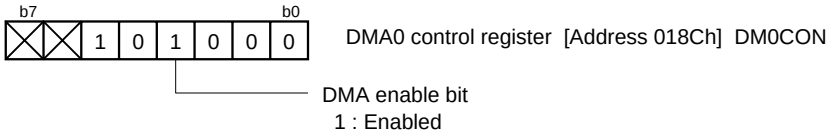
Setting DMA0 interrupt control register



(3) Enables interrupt (I flag = “1”)

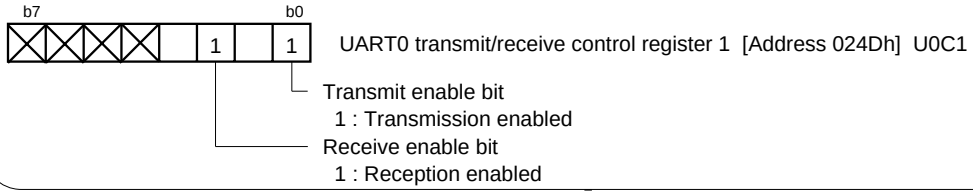
(4) Setting DMA0 control register back again (to enable DMA)

Setting DMA0 control register



(5) Enables transmit/receive

Set the TE and RE bits in the U0C1 register both to “1”, to enable transmission and reception.



(6) Starting successive reception

Access the U0RB register for dummy read to initiate successive reception.

(7) DMAC transfer complete interrupt processing

Check the received data for errors and, if necessary, reinitialize the serial I/O as error processing.

4. Reference

Hardware manual

M16C/64 Group Hardware Manual

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