MOSFET
Power MOS FET Application Note

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Introduction

This document describes MOSFET characteristics and basic usage based on the contents included in the MOSFET data sheet.

Contents

1. What is MOSFET?

MOSFET is the abbreviation for Metal Oxide Semiconductor Field Effect Transistor, a semiconductor device that delivers faster switching and lower losses compared to the bipolar power transistor.

With high-speed and low-loss characteristics, MOSFETs are used in a wide range of fields, from consumer and industrial equipment to in-vehicle devices, including electronic devices, factory automation equipment, power circuits (DC-DC converters, etc.), and motor drive inverters.

Figure 1 shows a MOSFET (Nch) equivalent circuit, and Figure 2 shows a comparison of the structures and features of a MOSFET (Nch) and a bipolar transistor (NPN type).

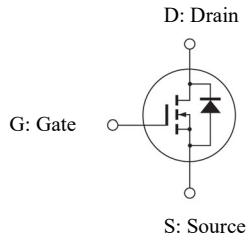
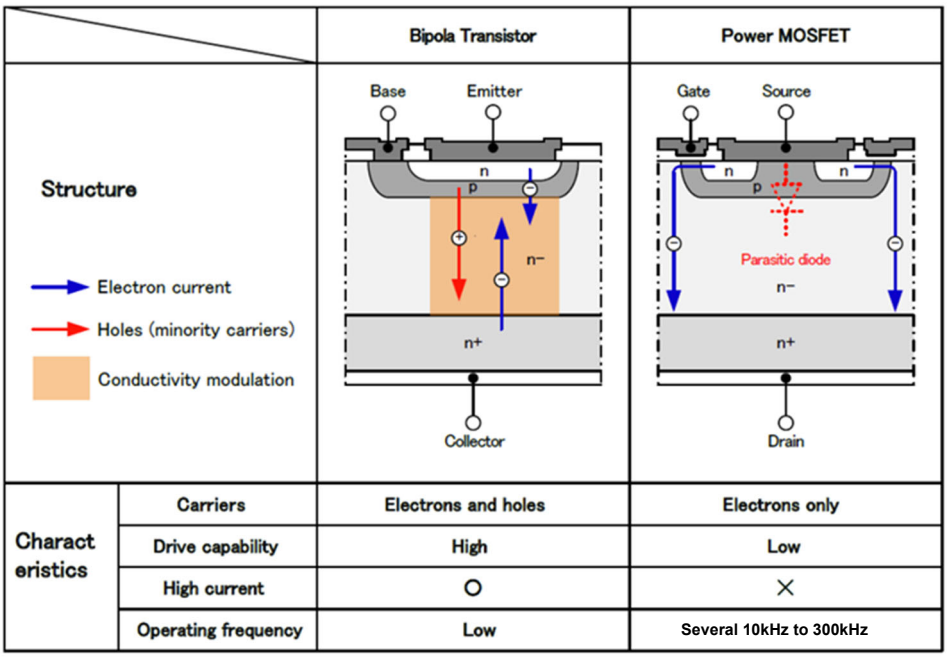


Figure 1. MOSFET(Nch) Equivalent circuit

An NPN-type bipolar transistor is a current-controlled device in which an N-type semiconductor emitter with high impurity concentration and a P-type semiconductor base are sandwiched between N-type semiconductor collectors. When a forward voltage is applied to the base-emitter PN junction, current flows between the base and emitter due to the recombination of electrons injected from the emitter and holes injected from the base layer. However, since the number of electrons injected from the emitter, which has a higher impurity concentration than the holes injected from the base layer, is larger, a large number of electrons that have not recombined with the holes pass through the base layer and diffuse to the collector, applying a positive voltage. As a result, current flows between the collector and emitter.

On the other hand, a MOSFET is a voltage-controlled device consisting of a metal-oxide semiconductor structure, or MOS structure. Specifically, a P-type semiconductor is sandwiched between the drain of an N-type semiconductor with high impurity concentration and the source of an N-type semiconductor. An insulated gate electrode is positioned on the P-type semiconductor which is coated with aa silicon oxide film for insulation. When a positive voltage is applied to the gate electrode, electrons in the P-type semiconductor are attracted to each other so that an inversion layer with the characteristics of an N-type semiconductor appears. The drain and source are connected by the N-type semiconductor. Applying a positive voltage between the drain and source causes current to flow from the drain to the source.

In addition, while bipolar transistors apply current flow with electrons and holes as carriers, MOSFETs only allow current to flow with electron carriers, enabling high-speed switching operations.



		Bipola Transistor	Power MOSFET
Charact eristics	Carriers	Electrons and holes	Electrons only
	Drive capability	High	Low
	High current	○	×
	Operating frequency	Low	Several 10kHz to 300kHz

Figure 2. Basic Transistor Structure Comparison

2. Terminology Explanations

2.1 Absolute Maximum Ratings

Absolute maximum ratings are the rated values determined to ensure safe use of MOSFET devices. Exceeding these absolute maximum ratings even momentarily can result in device deterioration or breakdown. Therefore, always use MOSFETs within the absolute maximum values listed here.
Note that when no absolute maximum rating is specified, Ta=25℃.

Table 1. Absolute Maximum Ratings

Characteristic	Symbol	Definition
Drain to source voltage	V_{DSS}	Maximum voltage that can be applied between drain and source when short-circuiting gate and source
Gate to source voltage	V_{GSS}	Maximum voltage that can be applied between gate and source when shorting drain and source
Drain current	I_D	Maximum allowable current for drain terminal
Peak drain current	$I_{D(pulse)}$	Maximum allowable current for drain terminal during pulse operation
Reverse drain current	I_{DR}	Maximum allowable current for parasitic diode
Avalanche current	I_{AP}	Maximum allowable drain current during single avalanche operation
Avalanche energy	E_{AS}	Maximum allowable energy during single avalanche operation
Allowable channel dissipation	P_{ch}	Maximum allowable power loss between drain and source
Channel temperature	T_{ch}	Maximum allowable channel temperature
Storage temperature	T_{stg}	Allowable temperature range for storage when power is not applied

Usage note:
Even when this product is used under conditions (usage temperature/current/voltage, etc.) within absolute maximum ratings, continuous use under an extreme load (high temperature, large current, high applied voltage, or extreme temperature variations, etc.) may decrease reliability significantly. Please confirm the Renesas Electronics Semiconductor Reliability Handbook (usage notes, recommendations, and derating concepts and methods) and each individual reliability information for each device (reliability evaluation report, predicted failure rate, etc.) in order to design a sufficiently reliable product.

2.2 Electrical Characteristics

Table 2 provides a list of MOSFET electrical characteristics and definitions.
Note that when no absolute maximum rating is specified, Ta=25°C.

Table 2. Electrical Characteristics

Characteristic	Symbol	Definition
Drain to source breakdown voltage	$V_{(BR)\ DSS}$	Drain to source voltage for specified drain current by shorting gate to source
Drain cutoff current	I_{DSS}	Drain current when specified voltage is applied between drain and source by shorting gate to source
Gate cutoff current	I_{GSS}	Gate current when specified voltage is applied between gate and source by shorting drain to source
Gate to source threshold voltage	$V_{GS(off)}$	Gate to source voltage used for specified drain current when specified drain to source voltage is applied
Drain to source ON resistance	$R_{DS(on)}$	Drain to source resistance for specified drain current when specified gate to source voltage is applied
Input capacitance	C_{iss}	Input capacity for specified gate to source voltage, specified drain to source voltage, and specified frequency
Output capacitance	C_{oss}	Output capacity for specified gate-source voltage, specified drain-source voltage, and specified frequency
Reverse transfer capacitance	C_{rss}	Reverse transfer capacitance capacity for specified gate to source voltage, specified drain to source voltage, and specified frequency
Total gate charge	Q_g	Electric charge required to apply specified voltage between gate and source
Gate to source charge	Q_{gs}	Electric charge required to increase gate-source voltage to threshold voltage
Gate to drain charge	Q_{gd}	Increased electric charge due to mirror effect between voltage and gate and drain
Turn-on delay time	$t_{d(on)}$	The time it takes for the drain to source voltage to fall to a given voltage the moment the gate to source voltage rises to a given voltage (refer to Section 3.5. Switching Characteristics)
Rise time	t_r	The time it takes for the drain to source voltage to fall from a given voltage to another (refer to Section 3.5. Switching Characteristics)
Turn-off delay time	$t_{d(off)}$	The time it takes for the drain to source voltage to rise to a given voltage the moment the gate to source voltage falls to a given voltage (refer to Section 3.5. Switching Characteristics)
Fall time	t_f	The time it takes for the drain to source voltage to rise from one specified voltage to another (refer to Section 3.5. Switching Characteristics)
Body-drain diode forward voltage	V_{DF}	The source to drain voltage when a given current flows toward the parasitic diode
Body-drain diode reverse recovery time	t_{rr}	The given amount of time during which the reverse recovery current is flowing in (through?) the parasitic diode (refer to Section 3.6 Body Diode Characteristics)
Body-drain diode reverse recovery charge	Qrr	The amount of charge amount for a given time during which reverse recovery current flows through the parasitic diode (refer to Section 3.6 Body Diode Characteristics)

3. Electrical Characteristics

3.1 Rated Current, Power Dissipation

Figure 3 shows the relationship between allowable channel dissipation and case temperature.

Generally, allowable channel dissipation is rated at case temperature Tc = 25 ° C; allowable channel dissipation is limited as the case temperature increases. The allowable channel dissipation when TC = 25°C or higher can be obtained using the following equation:

$$Pch = \frac{(Tchmax - Tc)}{\theta ch-c}$$

Tch max : Absolute Maximum Ratings Tch
Tc : Case Temperature
Θch-c : Channel to Case Thermal Resistance

Note that when Tc is less than 25°C, channel dissipation remains at the specified by the absolute maximum rating

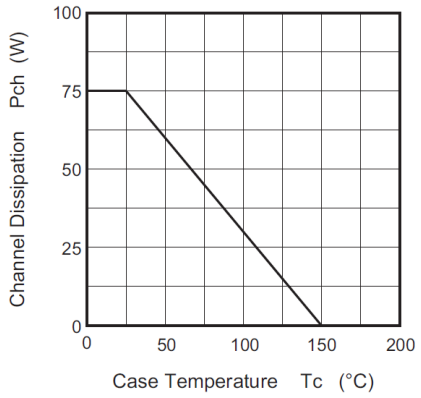


Figure 3. Allowable channel dissipation vs. case temperature
(Ex:200V/20A/0.1Ωtyp)

3.2 Safe Operating Area

Always confirm individual data sheets for the safe operating area of the MOSFET you are using in your design. Note that the safe operation area is a design value included in the conditions specified by Renesas Electronics. Figure 4 shows the safe operating area (SOA) for Renesas MOSFETs. The SOA is divided into five limited areas, as follows.

① : Area 1: Current Rating Limit Line
Area is limited by maximum rated drain peak current ID(pulse).

② : Area 2: On state resistance RDS(on) Limit Line
Area is limited by on state resistance.

③ : Area 3: Channel Dissipation Limit line
Area limited by channel dissipation Pch; calculated by the channel dissipation calculation equation described in Section 3.1

④ : Area 4: Secondary Breakdown Line
Not all MOSFET products have secondary breakdown lines. Note that products that do have a secondary breakdown line are limited to a smaller safe operation area.
Also be aware that the channel dissipation calculation equation described in section 3.1 does not apply to the secondary breakdown line.

⑤ : Area 5: Voltage Rating Limit Line
Area is limited by maximum rated drain to source voltage. VDSS.

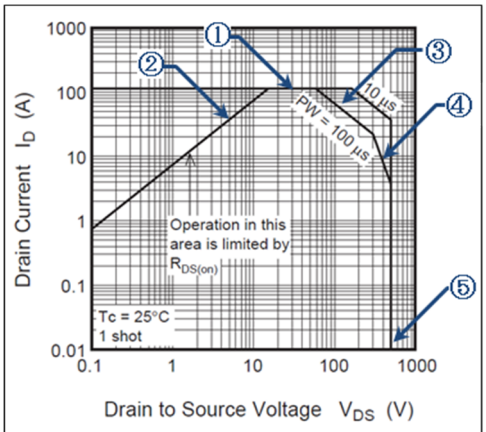


Figure 4. Safe Operating Area（SOA）
(Ex:500V/38A/0.105Ωtyp)

3.3 Electrostatic Characteristics

Figure 5 shows an example of output characteristics for MOSFET semiconductors.
The output characteristics show the drain to source voltage when drain current is flowing under any gate voltage conditions. This drain to source voltage is affects on state dissipation.
Also note that this drain to source voltage varies due to gate voltage and case temperature. Make sure to take this into consideration when designing a product.

Figure 6 shows an example of drain to source saturation voltage vs. gate to source voltage characteristics.
Drain to source saturation voltage VDS(on) decreases as gate to source voltage VGS increases and the change in VDS(on) decreases. Therefore, MOSFET devices must be used at a VGS in an area where VDS(on) saturation is low. On the other hand, MOSFETs are not recommended for use in low VGS areas because VDS(on) dissipation is high in such areas, leading to an increase in dissipation.

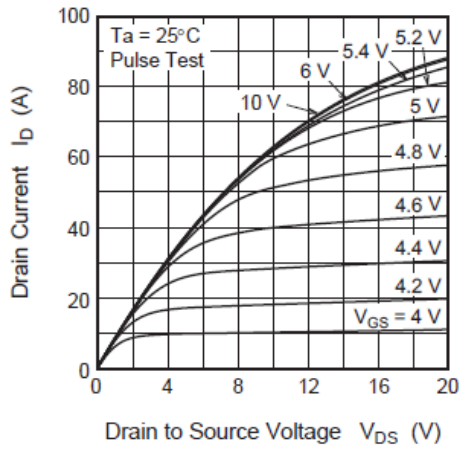


Figure 5. Output Characteristics
(Ex:500V/38A/0.105Ωtyp)

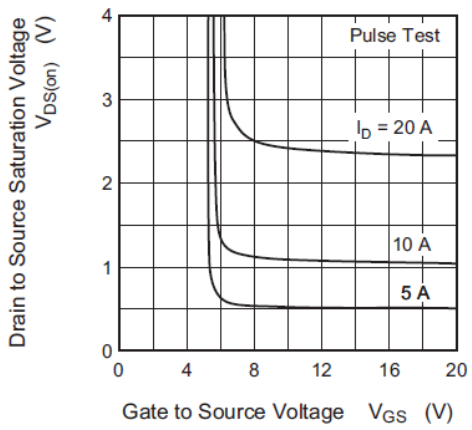


Figure 6. Drain to Source Saturation Voltage vs.
Gate to Source Voltage
(Ex:200V/20A/0.1Ωtyp)

Figure 7 and 8 show temperature dependency examples of drain to source resistance and gate to source cutoff voltage. Since drain to source on-resistance has a positive temperature dependency, it becomes difficult to flow current when heat is generated by MOSFET operations, and current concentration is less likely to occur during parallel operations. On the other hand, the gate to source cutoff voltage has a negative temperature dependency, so the cutoff voltage may drop at high temperatures, which may cause malfunctions due to noise, and the cutoff voltage may increase at low temperatures. This may prevent the MOSFET from turning on sufficiently. For this reason, it is necessary to verify these characteristics when designing.

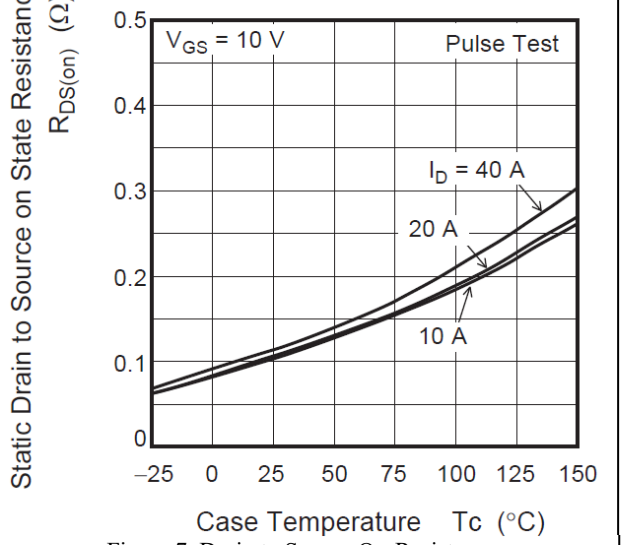


Figure 7. Drain to Source On-Resistance RDS(on) Temperature (Ex:500V/40A/0.102Ωtyp)

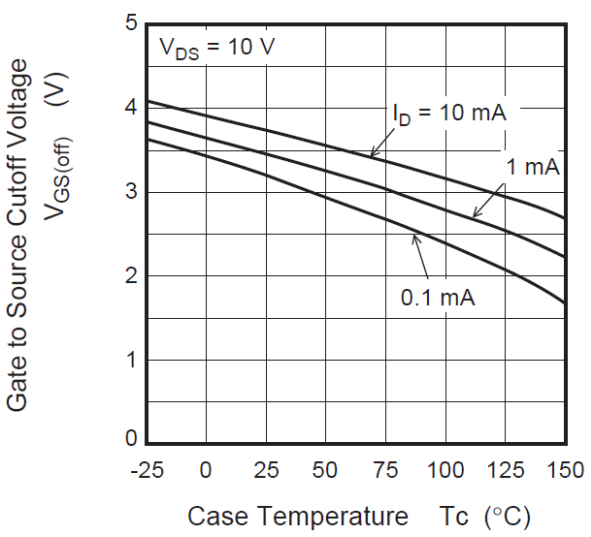


Figure 8. Gate to Source Cutoff Voltage Temperature Dependency (Ex:500V/40A/0.102Ωtyp)

Figure 9 shows an example of drain current vs. gate voltage characteristics.
Drain current vs. gate voltage characteristics depend on temperature. Drain current centers on the cross point, with a positive temperature coefficient in the area where gate voltage is low, and a negative temperature coefficient in the area where gate voltage is high. Because power devices generate heat when operating, if using a few devices in parallel, use them in the negative temperature coefficient area to maintain a balanced drain current.

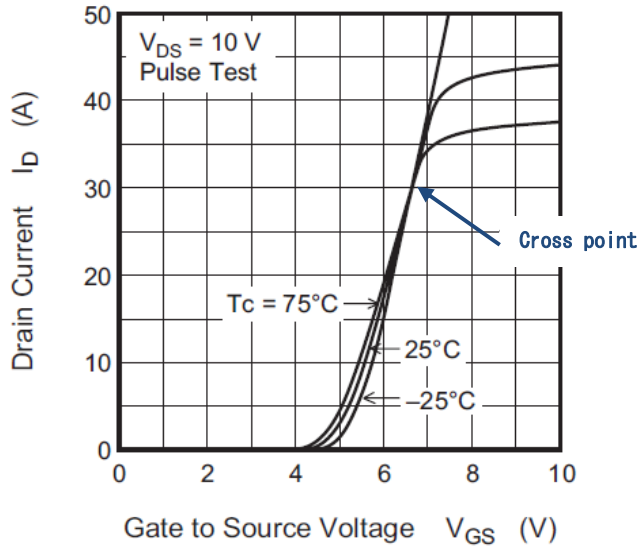


Figure 9. Transfer Characteristics (Ex:200V/20A/0.1Ωtyp)

3.4 Capacitance Characteristics

3.4.1 Ciss, Coss, Crss

Figure 10 shows an example of capacitance between terminals as well as capacitance vs. drain to source voltage characteristics.

Input capacitance Ciss, output capacitance Coss, and reverse transfer capacitance have the following relationships.

Ciss = Cgs + Cgd
Coss = Cds + Cgd
Crss = Cgd

provided that,
Cgs: Gate to source capacitance
Cds: Drain to source capacitance
Cgd: Gate to drain capacitance

Measurement conditions for the following specify drain to source voltage VDS, gate-source voltage VGS, and frequency f.

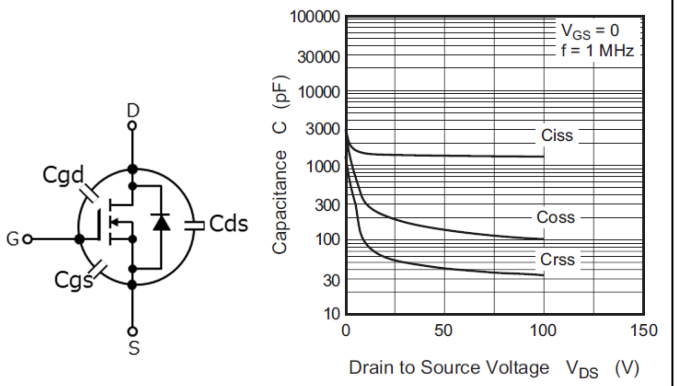


Figure 10. Terminal to Terminal Capacitance
(Ex:200V/20A/0.1Ωtyp)

3.4.2 Gate Charge Characteristics

Figure 11 shows an example of gate charge characteristics.
MOSFET gate charge characteristics are the parameters that determine drive current and drive loss. The characteristics curve in Figure 11 is divided into three sections. The following describes operations for each sectional period.

＜Period 1＞
Gate voltage is raised to the cutoff voltage at which drain current starts to flow. The section rising from VGS=0V charges the gate to source capacitance Cgs.

＜Period 2＞
During the transition from period 1 to saturated region, drain to source voltage changes and gate to drain capacitance Cgd is charged. During this period, because the apparent capacitance increases due to the mirror effect, VGS is constant. However, the MOSFET goes to a fully ON state, eliminating the VDS change and the mirror effect.

＜Period 3＞
On state resistance of MOSFET goes to a saturated state and VDS no longer changes.
VGS voltage increases over time.

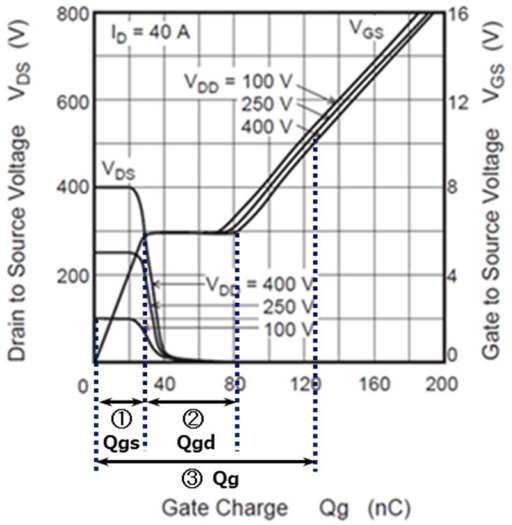


Figure 11. Gate Charge Characteristics
(Ex:500V/40A/0.102Ωtyp)

3.4.3 How to Determine Gate Drive Current

Gate drive current is determined by gate series resistance Rg, signal source resistance Rs of the drive circuit, element internal resistance rg, and drive voltage VGS(ON), and is as expressed in the following equation.

$$I_{G(peak)} = \frac{V_{GS(on)}}{Rg + Rs + rg}$$

Accordingly, the output stage of the drive circuit must be designed with current drive capability equal to or larger than IG(peak). The actual peak current tends to be smaller than the calculated value due to the drive circuit delay and the delay in the dIG/dt rise of the gate current due to factors such as the wiring inductance from the drive circuit to the gate pad of the MOSFET chip.

Furthermore, switching loss and surge voltage during switching depend on Rg.

Surge voltage during switching operations can be suppressed by increasing the value of Rg, but increasing the value too much can result in extensive switching loss. In order to achieve the best balance of component performance and total loss, consider these factors when selecting the most appropriate Rg.

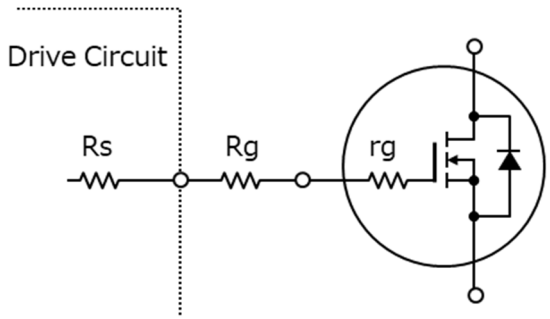


Figure 12. Resistance Component of Drive Circuit

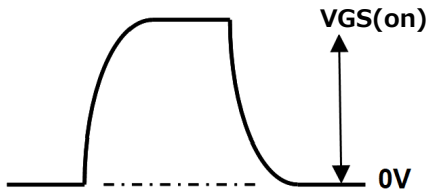


Figure 13. Gate Terminal Drive Waveform

3.4.4 Drive Loss Calculation

When all the generated loss of the drive circuit is consumed by these resistance components, the drive loss is expressed by the following equation. (f: switching frequency)

$$P_{(Drive\ Loss)} = V_{GS(on)} \times Qg \times f$$

3.5 Switching Characteristics

As MOSFETs are switching elements, switching speed (turn-on time, turn-off time) is an important parameter that affects efficiency (loss). Figure 14 shows the resistance load of the switching measurement circuit.

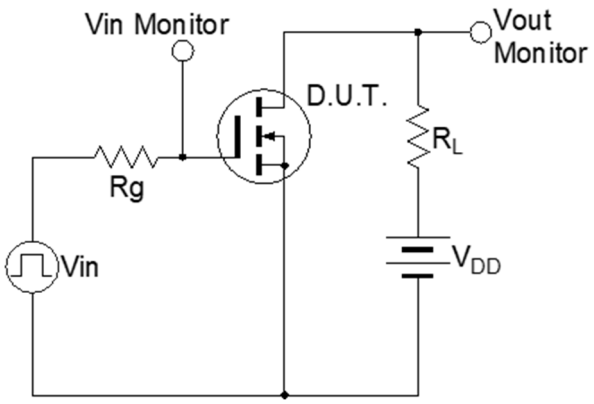


Figure 14. Switching Characteristic Measurement Circuit: resistance load

Switching time is measured by dividing it into the four periods shown in Figure 15. These times vary greatly depending on the conditions of Tch, ID, VDS, VGS, and Rg, and are therefore measured under the conditions specified in the data sheet.

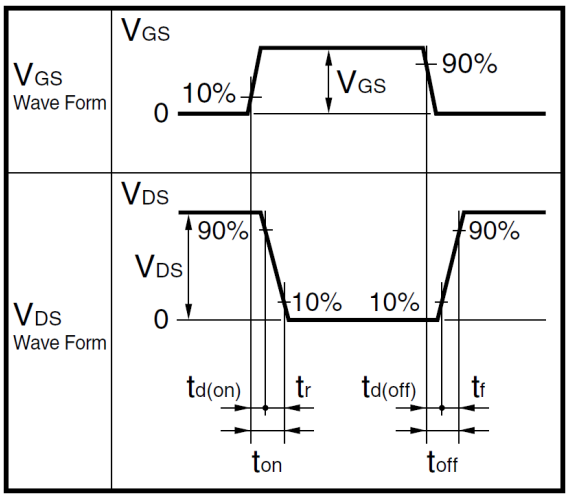


Figure 15. Switching Waveform

$t_{d(on)}$ (turn-on delay time)
The time until gate to source voltage rises to 10% and drain to source voltage falls to 90%.

t_r (rise time)
The time until drain to source voltage falls from 90% to 10%.

$t_{d(off)}$ (turn-off delay time)
The time until gate to source voltage falls to 90% and drain to source voltage rises to 10%.

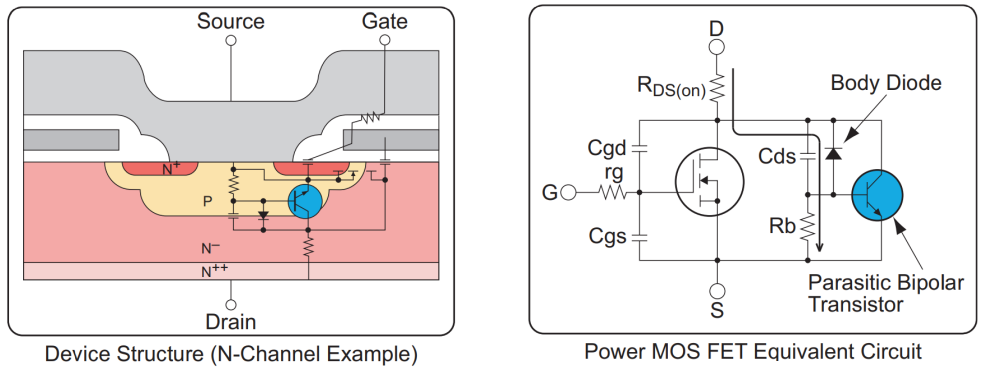
t_f (fall time)
The time drain to source voltage rises from 10% to 90%

3.6 Body Diode Characteristics

Figure 16 shows the power MOSFET structure and equivalent circuit. As seen in the figure, the 3.6 body diode is formed between the source to drain due to its structure, and also referred to as a Body diode or parasitic diode.

The body diode may be used as a free wheel diode for regenerative current flow to the inverter circuit for motor control.

When utilizing it in this manner and reverse voltage is applied immediately after the regenerative current, the MOSFET may be damaged depending on the circuit and operating conditions.



Device Structure (N-Channel Example)

Power MOS FET Equivalent Circuit

Figure 16. Power MOS FET Component Structure and Equivalent Circuit

3.6.1 Characteristics of Body Diode between Source and Drain

Figure 17 shows an example of characteristics of reverse drain current vs. source to drain voltage. This diode boasts characteristics similar to those of ordinary diodes. When used in a bridge circuit of a motor drive application, an output stage of a PWM amplifier, etc., it may be possible to omit the external rectifier diode.

In addition, when a channel is formed by positively biasing VGS, the current flows in the same manner in the both direction. In the small current area, this becomes straight line IDR × Ron, enabling a smaller VF than that of an ordinary diode. This can be extremely useful for certain applications.

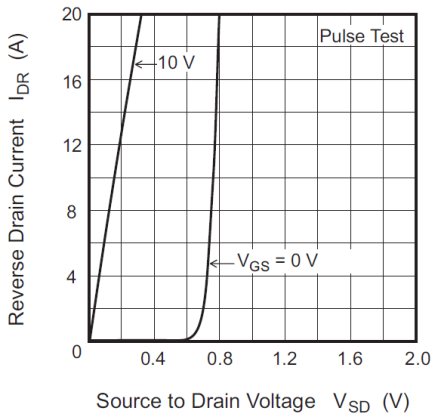


Figure 17. Reverse Drain current vs. Drain to Source Voltage
(Ex：100V/20A/17mΩtyp)

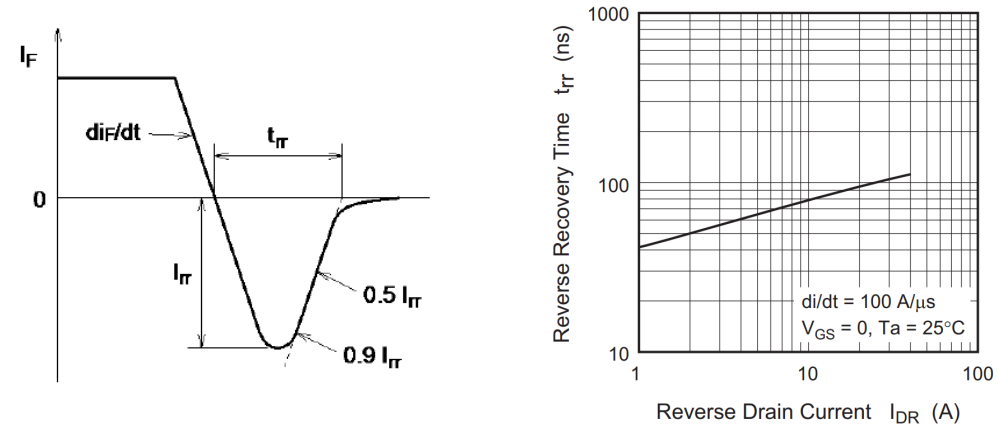
3.6.2 Body Diode Reverse Recovery Characteristics

The accumulated minority carriers are emitted when switching from the state of forward current to the state of backward current for Body Diode. The time until the minority carriers are completely discharged is called reverse recovery time trr. The current at that time is called reverse recovery current Irr, and those integral value is called reverse recovery charge Qrr.

$$\mathrm{Qrr} = \frac{1}{2} Irr \times trr$$

For example, in a synchronous rectifier circuit, the high-side MOSFET turns off, and a dead time is set between the turn-off and turn-on of the low-side MOSFET, during which trr, Irr, and Qrr occur. （Figure19）

The trr period is equivalently short-circuited, resulting in a large loss. In addition, in general, a fast trr and small Irr (small Qrr) are desirable as the operating frequency is restricted during switching operations. Note that these characteristics depend on forward current I_F and di_F/dt.



(a) Body Diode Reverse Recovery Characteristic

(b) Body Diode Reverse Recovery Time
(Ex：200V/20A/0.054Ωtyp)

Figure 18. Body Diode Switching Characteristic

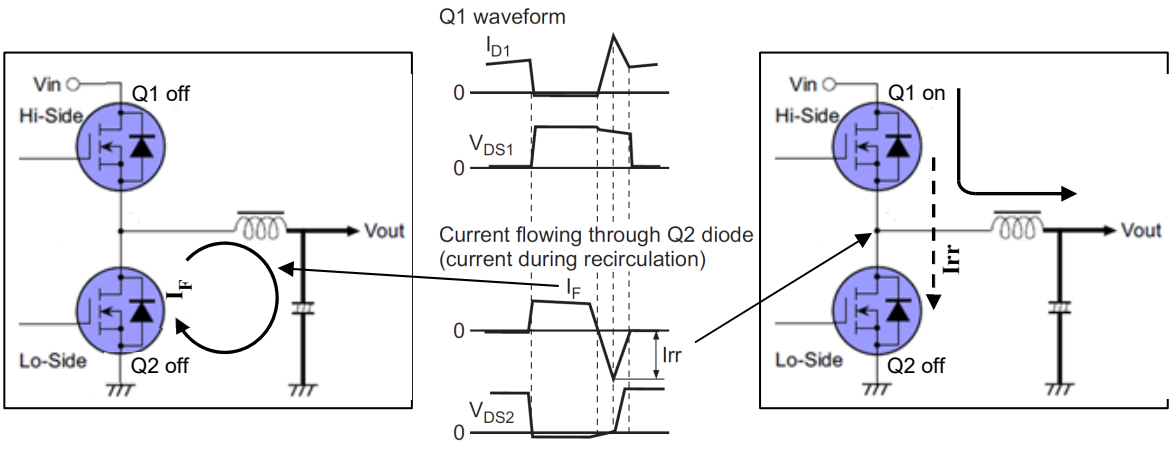


Figure 19. Reverse recovery operation of body diode
in synchronous rectification type DC / DC converter

3.6.3 Body Diode Destruction Mechanism

Figure 20 shows the destruction mechanism of the body diode.

Body diode destruction resistance has improved considerably, and structural measures have been taken to inhibit parasitic bipolar transistor operations, so that the problem of destruction almost never occurs during normal use. However, if a reverse voltage is applied immediately after the forward current IF is applied to the body diode, such as when used as a freewheel diode, the MOSFET may be damaged depending on the circuit and operating conditions, so care must be taken.

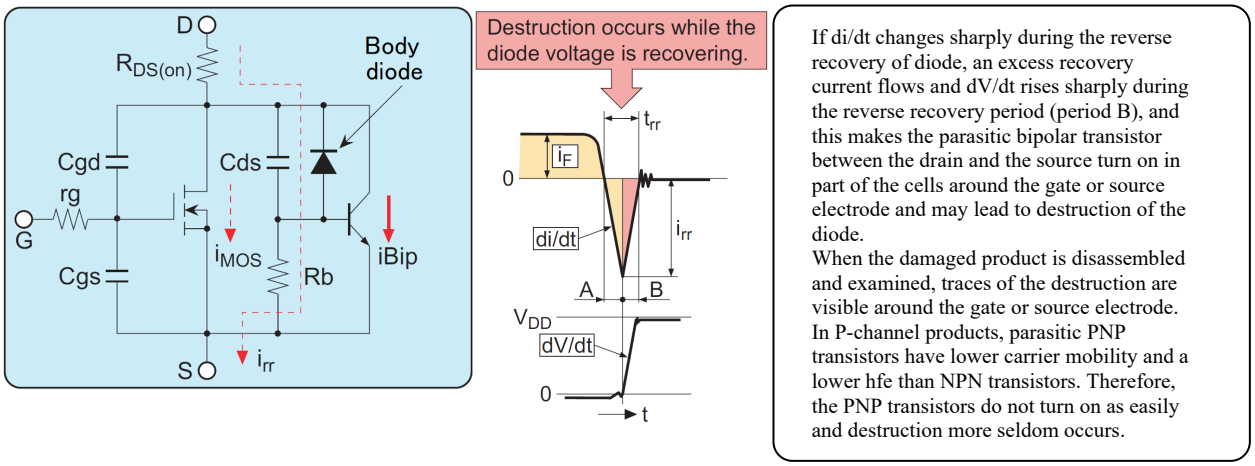


Figure 20. Body Diode Destruction Mechanism

Figure 21 shows examples (usage notes) of body diode destruction circuit countermeasures.

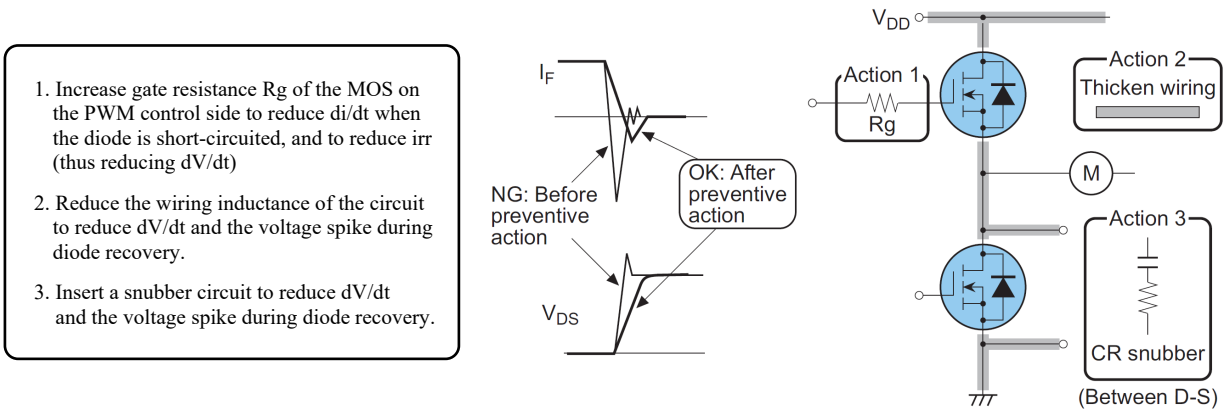


Figure 21. Examples of Body Diode Destruction Circuit Countermeasures

3.7 Avalanche Operation

Avalanche operation means that the flyback voltage that occurs when the switching operation is off with a inductive load or the spike voltage due to leakage inductance enters the breakdown region that exceeds the power MOS FET drain rated voltage, and it is the phenomenon that avalanche current flows from drain to source.

Some MOSFETs have a one-shot or repetitive avalanche operation standard, but the meaning of “repetitive” refers to, for example, a surge voltage that enters continuously (transiently continuous) when the power is turned on.
Note that operation that constantly exceeds the rated voltage is not applicable.

There are following three modes of MOSFET destruction caused by avalanche operation.

1. Current destruction mode
2. Energy destruction mode
3. dV/dt destruction mode

Each destruction mode is described below.

3.7.1 Avalanche destruction mode I (current destruction)

MOSFET is formed by a collection of many small FET cells (a large number of FET cells connected in parallel). Especially for low-voltage products of 250V or less, in order to reduce the on-resistance of the element, each FET cell is miniaturized, a trench is formed on the surface, and a gate is embedded therein (the FET cell area is reduced) to improve performance. Figure 22 shows the cross-sectional structure and equivalent circuit of the FET cell of the trench structure FET chip. In the cross-sectional structure, an NPN-type parasitic transistor is configured between the N+ layer connected to the source electrode, the P layer forming the channel, and the N- layer on the drain side.

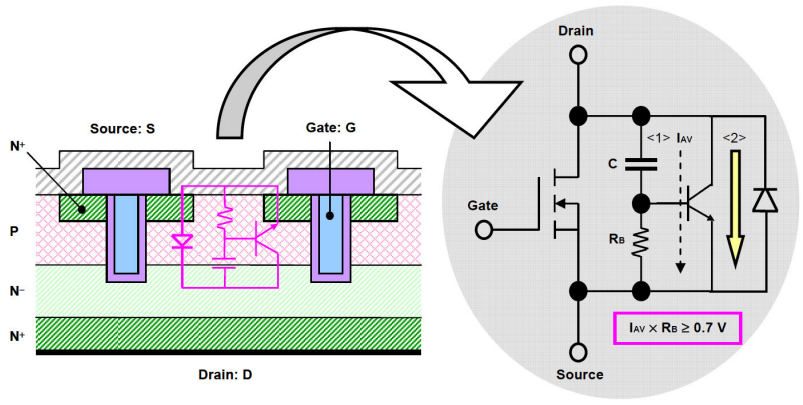
The following describes how current destruction of FET occurs within this structure.

(1) When voltage exceeding the rated value is applied between the drain and source, a breakdown current (avalanche current: IAV) flows.

(2) This current (IAV①) flows from the drain to the source through the resistance component (RB) of the P layer via the parasitic capacitance (C) in a pulsed manner.

(3) At this point, when IAV current increases and voltage across RB exceed the VBE on voltage value of the parasitic NPN transistor, the NPN transistor turns on.

(4) As a result, the overcurrent (IAV②) amplified by the parasitic transistor flows to the collector side and the parasitic transistor (=FET) is destroyed by the heat generated from the large current.
To avoid current destruction, it is necessary to minimize the parasitic capacitance (C) and resistance component (RB) as much as possible when designing the cell structure. Also be aware that destruction current affected by temperature. The higher the temperature, the smaller the current that leads to destruction.
However, in general, the effect of temperature on current destruction is less than that the effect of the energy destruction area, as described later.



<1> A voltage exceeding the rated breakdown voltage (V_{DSS}) of the element is applied and the parasitic transistor is biased by R_B.

<2> The parasitic transistor is turned off, causing a high current to flow and destroy the cell.

Figure 22. FET Cell Cross-Sectional Structure and Equivalent Circuit of Trench Structure FET Chip

3.7.2 Avalanche Destruction Mode II (energy destruction)

Avalanche operational waveform (Figure 23) for the L load switching circuit , the FET channel temperature (Tch) rises during avalanche operations (t_{AV}). This is because the energy of avalanche voltage ($V_{(BR)DSS}$) and avalanche current (I_{AV}) is consumed by the FET.

The energy destruction mode means that energy is applied to the FET and the PN junction exceeds the upper limit temperature and breaks. At this time, the destruction energy (E_{AV}) is determined by the following requirements.

–

$$E_{AV} = \frac{1}{2} L \cdot I_{AV}^2 \frac{V_{(BR)DSS}}{V_{(BR)DSS} - V_{DD}}$$

- L value (in proportion to t_{AV})
- Peak current I_{AV} flowing into the L load (in proportion to the ON time of the L load)
- Avalanche voltage $V_{(BR)DSS}$ of the FET

In addition, energy destruction is caused by temperature rise, and is directly affected by the channel temperature (starting Tch) just before entering the avalanche operation.

Note: The avalanche energy withstand (E_{AS}) guaranteed in Renesas product data sheets is generally a guaranteed value at starting Tch = 25 °C.

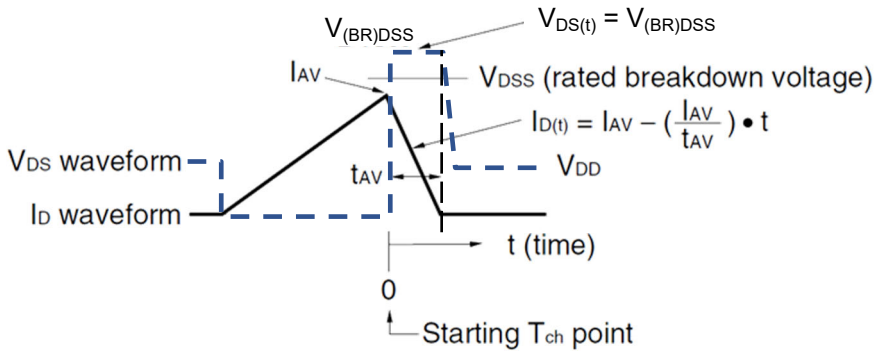


Figure 23. L Load Switching Circuit and Avalanche Operation Waveform of FET

3.7.3 Avalanche Destruction Mode III (dV/dt destruction)

The following describes the third factor, the relationship between avalanche destruction withstand and dV/dt. Figure 23 shows the measured value of the avalanche breakdown current IAP dependency on dV/dt tolerance. In MOSFETs, as shown in Figure 16, a parasitic bipolar transistor is formed between the drain and source. When dV/dt is steep, a transient current flows through the capacitor Cds. Since this transistor is turned on, the destruction withstand is reduced. In the example of Figure 23, dV/dt ≤ 10V/ns is considered a safe area. This value depends on the individual element.

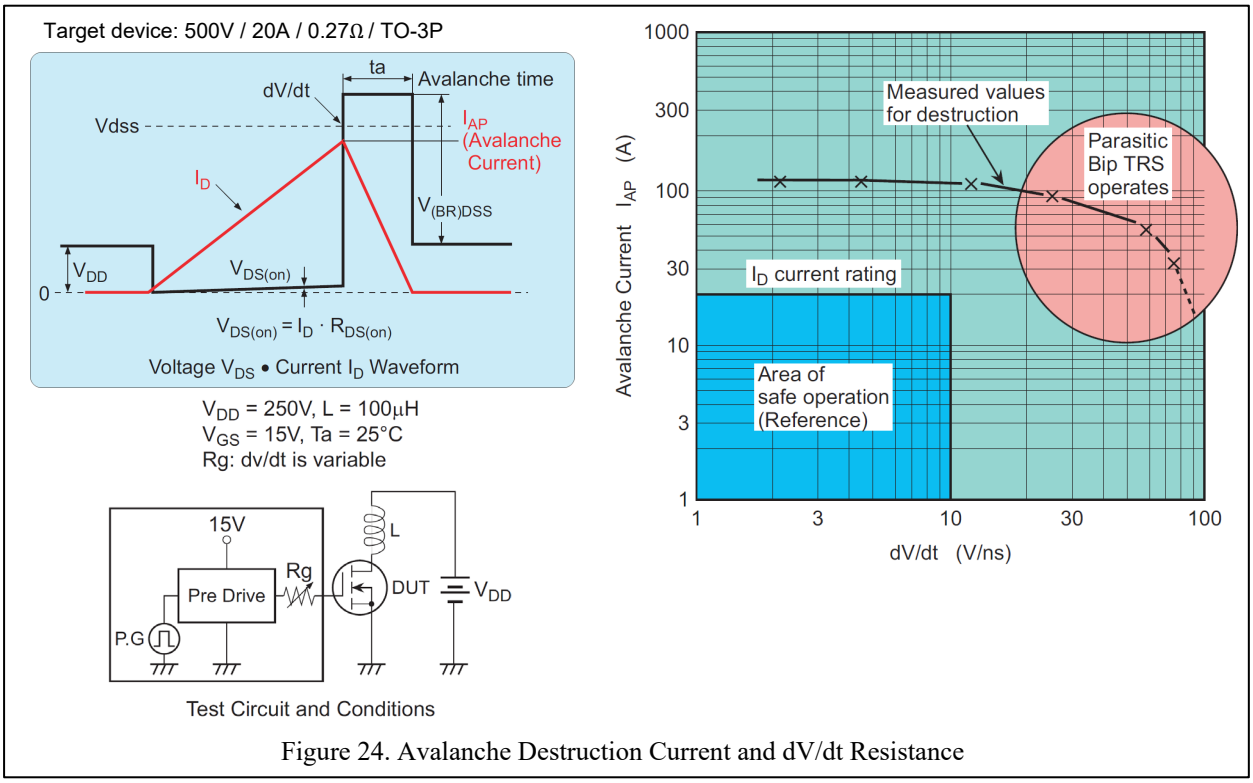


Figure 24. Avalanche Destruction Current and dV/dt Resistance

3.8 Non-Isolated Synchronous Rectification Converter Low-Side Self-Turn-On Phenomenon

Figure25 illustrates the low-side self-turn-on phenomenon in a non-isolated synchronous rectification circuit.
This phenomenon occurs at the switching timing at which high-side component Q1 is turned on while low-side component Q2 is off, and when the Q2 drain-source voltage changes abruptly from $V_{DS} \approx 0$ to V_{DS} = Vin, Ciss is charged via Crss of Q2, and Q2, which should really be off, is turned on.

The gate-source voltage of the Low side element at this time is expressed by the following equation.

$$V_{GS}(Q2) = \{Cgd/(Cgs + Cgd)\} \times dV(t)$$

That is to say, when VGS(Q2) exceeds VGS(off) of Q2, self-turn-on occurs.
As a result, Q1 and Q2 become on simultaneously, and excessive loss is generated, component heat radiation and a temperature rise are caused, leading to degradation of efficiency.

The following 2 points are generally given as self-turn-on circuit countermeasures.

1. Make only the high-side component turn-on time slower (suppress dV/dt).
2. Insert a capacitance C externally between the gate and source of the low-side component and (by making (KS = (Crss/Ciss + Crss) smaller) improve the self-turn-on margin.

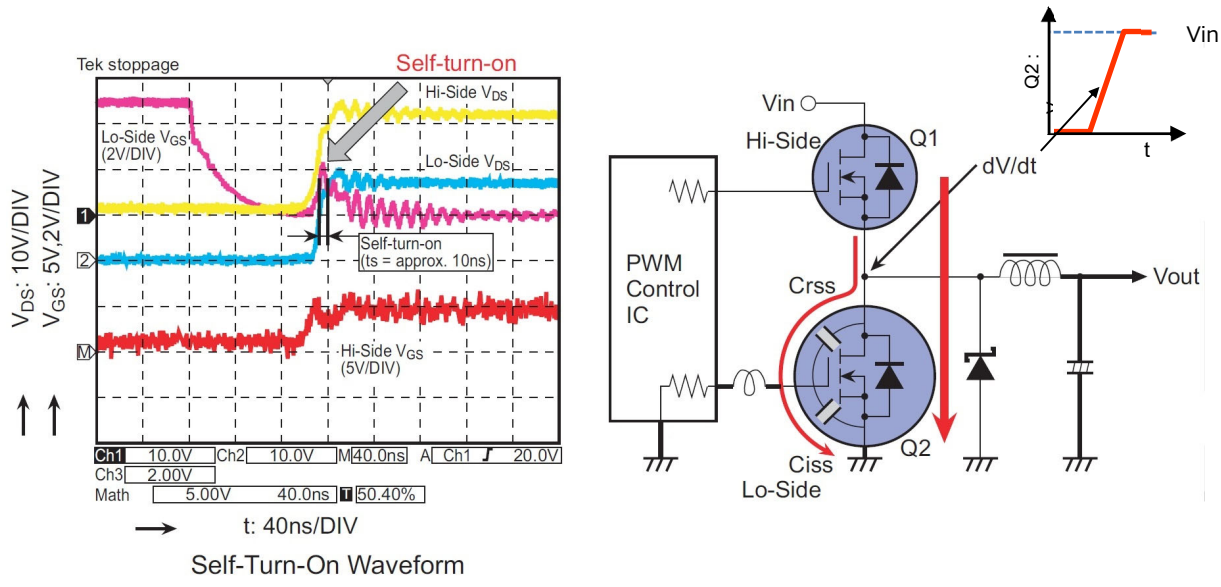


Figure 25. Non-Isolated Synchronous Rectification Converter Low-Side Self-Turn-On Phenomenon

4. MOSFET Loss

When determining whether the MOSFET is operating within the rating, the voltage and current can be confirmed by measuring, but it is difficult to confirm the channel temperature.

This section describes the procedure for calculating the channel temperature Tch from the operating waveform and the device case temperature Tc.

The channel temperature Tch calculated here is an estimated value.

(1) Channel temperature calculation procedure

The procedure for calculating the channel temperature when the same operating waveform is repeatedly input is shown below.

①Square wave approximation of operating waveform

Drain current ID and drain-source voltage VDS operating waveform is divided into MOSFET switching operating period and conduction period, and the loss in each period is calculated based on the ID and VDS waveform state and approximated to a square wave. (Figure 26)

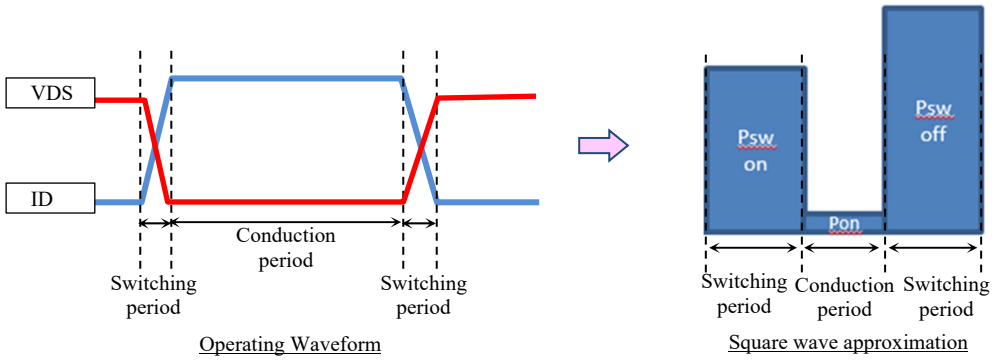


Figure 26. Square wave approximation of operating waveform

⒜When the VDS and ID waveforms cross (rise x fall) (Figure 27), use the following formula.

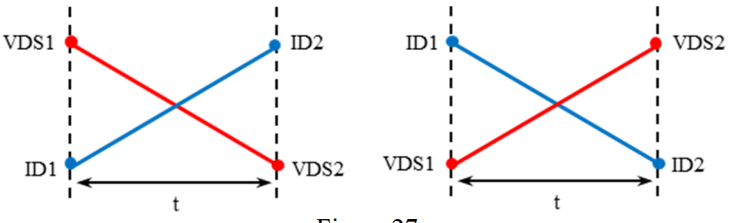


Figure 27

$P=1/6\times\{(2\times ID1\times VDS1)+(2\times ID2\times VDS2)+(ID1\times VDS2)+(ID2\times VDS1)\}$

⒝When the VDS and ID waveforms rise or fall with each other (Figure 28), use the following formula.

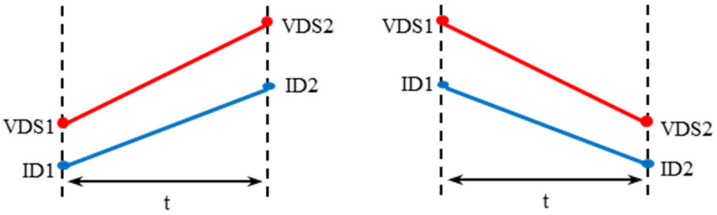


Figure 28

$P=[1/3\times\{(VDS2-VDS1)\times(ID2-ID1)\}]+[1/2\times\{(ID1\times VDS2)+(ID2\times VDS1)\}]$

⒞The loss during the conduction period is calculated from the drain current ID and the on-resistance RDS (on).

$P=(ID)^2\cdot RDS(on)$

② The following operating waveform can be obtained by summarizing the power for each period calculated in the calculations (a)～(c).

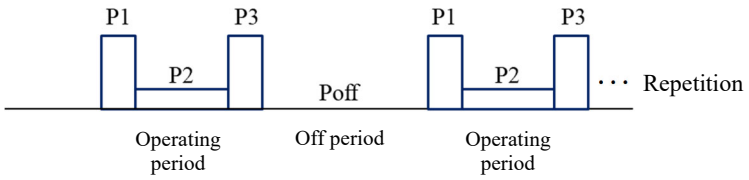


Figure 29

③ For power loss waveforms in which the same operating waveform is repeatedly input, it is easy and highly accurate to calculate by combining the waveforms for one or two cycles from the average value of the operating waveform over the entire period.

For that purpose, calculate the average loss Pav for the entire period and the average loss Pon for the operating period excluding the rest period in one cycle from the operating waveform obtained in No. 2, and create a square wave approximation waveform as shown in Figure 30.

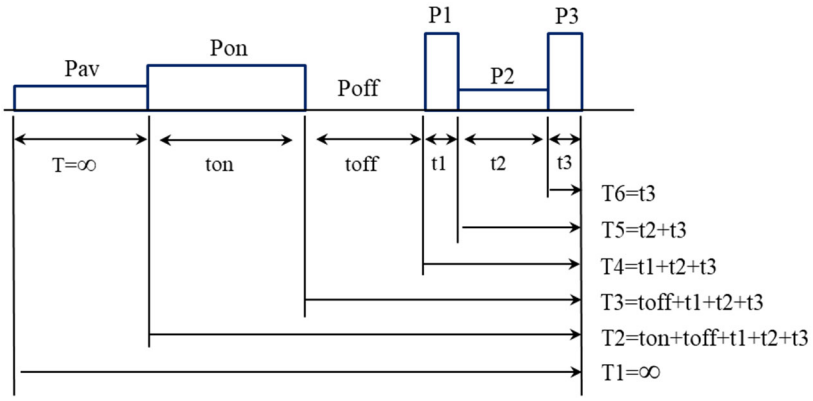


Figure 30

The following is a concrete example.

Average loss during operation period Pon: The average loss for one cycle of the loss waveform (P1 to P3) is calculated as follows.

$$Pon = (P1 \cdot t1 + P2 \cdot t2 + P3 \cdot t3)/T4 \qquad T4 = t1 + t2 + t3.$$

Average loss for all periods Pav: The average value of one cycle (P1 to P3) of the loss waveform and the rest period (Poff), which is calculated as follows.

$$Pav = (Pon \cdot T4)/T3 \qquad T3 = toff + t1 + t2 + t3$$

Channel temperature rise ΔTch：Calculate using the following formula using the Average loss for all periods Pav, the Average loss during operation period Pon, the loss for one cycle of the operating period, and the thermal resistance.

$$\Delta Tch = Pav \cdot Rth(T1) + (Pon - Pav) \cdot rth(T2) + (Poff - Pon) \cdot rth(T3) + (P1 - Poff) \cdot rth(T4) + (P2 - P1) \cdot rth(T5) + (P3 - P2) \cdot rth(T6) \ldots \text{formula -1}$$

As shown in Figure 30, T1~T6 are as follows.

T1= T=∞
T2=ton+toff+t1+t2+t3
T3=toff+t1+t2+t3
T4=t1+t2+t3
T5=t2+t3
T6=t3

④ The channel case thermal resistance Rth (ch-C) required for the calculation of the channel temperature rise ΔTch is read from the curve of 1 shot in the thermal resistance graph.(Figure 31)

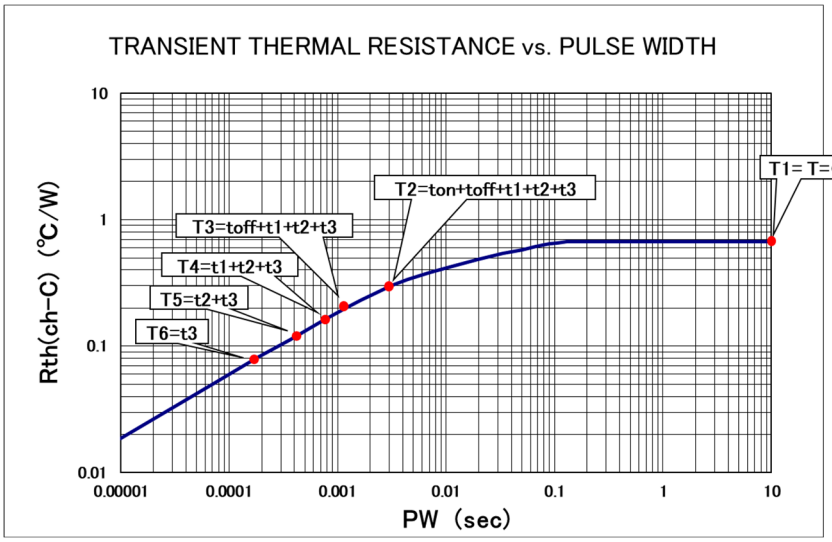


Figure 31

⑤ The channel temperature Tch is calculated from the device case temperature Tc and the channel temperature rise ΔTch under the conditions of use.

$$Tch = Tc + \Delta Tch$$

[Example of Calculation]

Calculate the channel temperature when the MOSFET case temperature Tc = 60 ° C, square wave approximate waveform P1 = P3 = 25W, P2 = 10W, and pulse width is as follows. (Figure32)

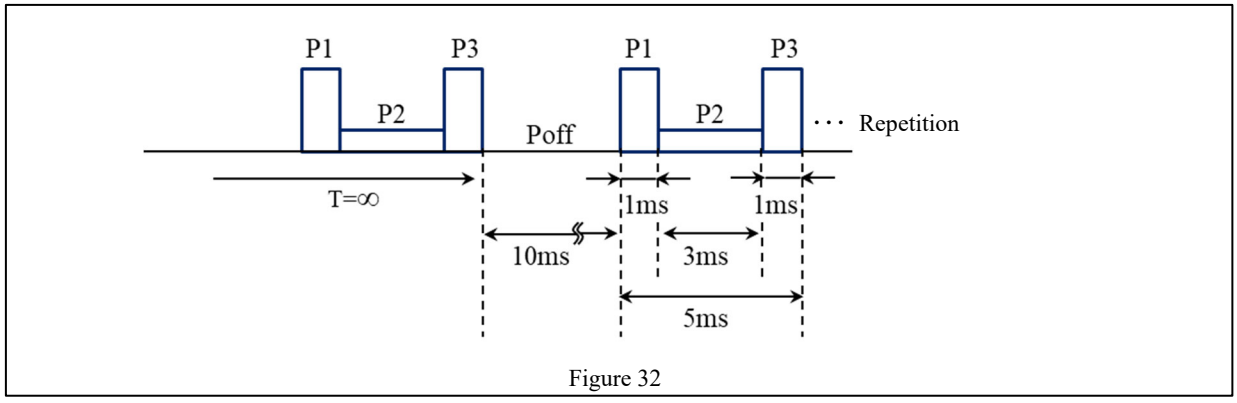


Figure 32

The above is a power loss waveform in which the same operation waveform is repeatedly input, so calculate by adding the waveform for one cycle to the average value for the entire period. (Figure 33)

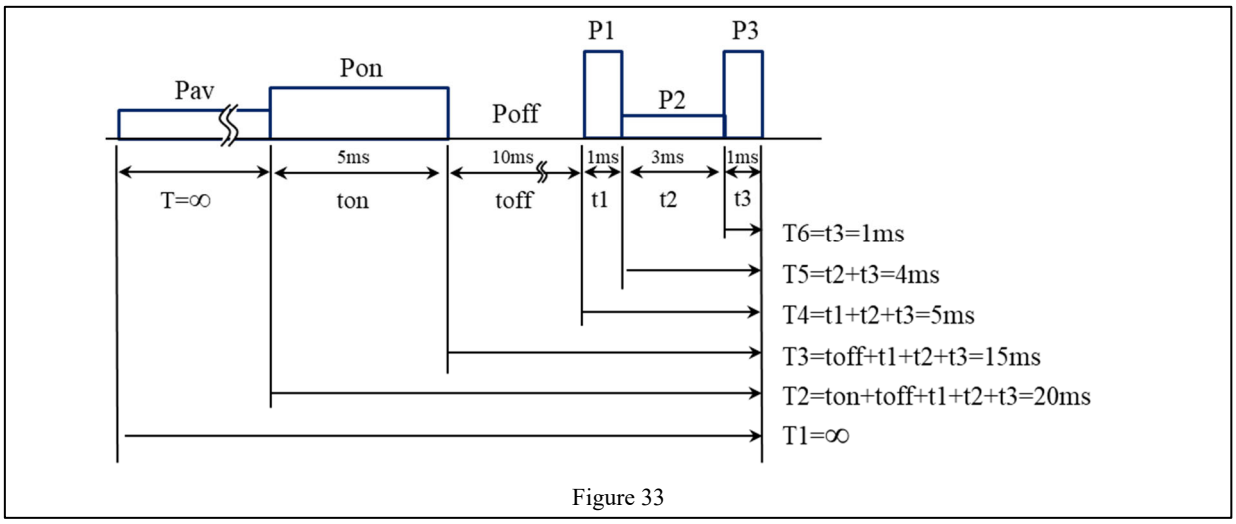


Figure 33

Calculate the average loss Pon (P1~ P3) during the operating period.

Pon =(P1・t1+P2・t2+P3・t3)/T4 =(25W・1ms+10W・3ms+25W・1ms)/5ms
=16W

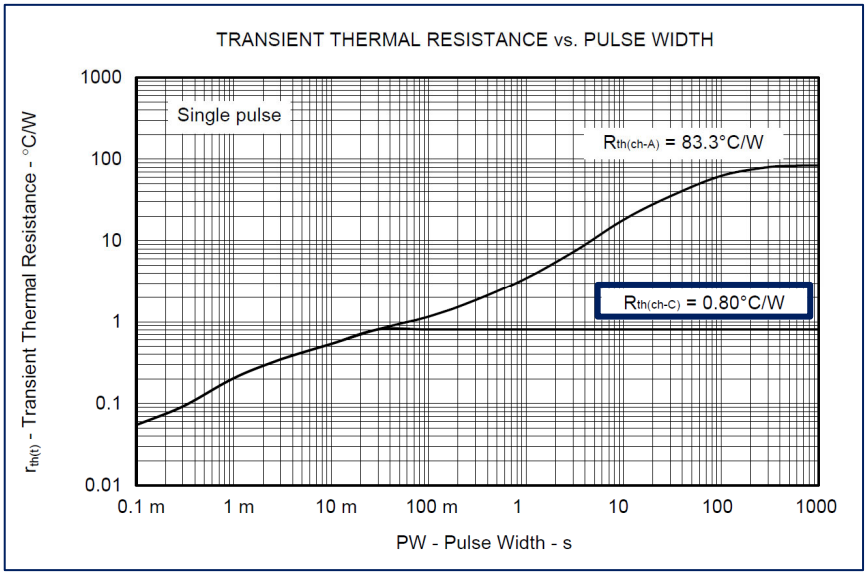
Calculate the average loss Pav (P1 ~ P3 and Poff) for the entire period.

Pav=(Pon・T4)/T3 =(16W・5ms)/15ms
=5.3W

The calculation of channel temperature rise ΔTch is as follows.

ΔTch=Pav・Rth(T1)+(Pon-Pav)・rth(T2)+(Poff-Pon)・rth(T3)+(P1-Poff)・rth(T4)
+(P2-P1)・rth(T5)+(P3-P2)・rth(T6) …Fomula-1

Here, the thermal resistance value required for the calculation is read from the curve of 1 shot in the thermal resistance graph. (Figure 34)



Thermal resistance (reading value)
Rth(T1)=Rth(ch-C)=0.8℃/W
rth(T2)=rth(20.0ms)=0.70℃/W
rth(T3)=rth(15.0ms)=0.62℃/W
rth(T4)=rth(5.0ms)=0.42℃/W
rth(T5)=rth(4.0ms)=0.38℃/W
rth(T6)=rth(1.0ms)=0.20℃/W

Figure 34. Transient Thermal Resistance vs. Pulse Width

⊿Tch is calculated by the following formula from the loss and thermal resistance obtained above.

ΔTch=Pav・Rth(T1)+(Pon-Pav)・rth(T2)+(Poff-Pon)・rth(T3)+(P1-Poff)・rth(T4)
+(P2-P1)・rth(T5)+(P3-P2)・rth(T6)
=5.3W・0.8℃/W+(16W-5.3W)・0.70℃/W+(0-16W)・0.62℃/W+(25W-0)・0.42℃/W
+(10W-25W)・0.38℃/W+(25W-10W)・0.2℃/W
=4.2℃＋7.5℃-9.9℃+10.5℃—5.7℃+3.0℃
=9.6℃

The channel temperature Tch is calculated by the case temperature Tc = 60℃ and the channel temperature rise ΔTch.

Tch=Tc＋ΔTch
=60℃+9.6℃
≒70℃

In addition, the calculation formula (Equation-1) is a notation summarized by thermal resistance, but in other materials, it may be written by a notation (Equation-2) summarized by electric power as shown below.

Similar calculation results can be obtained by using either of these two formulas.

（The conversion result from Equation-1 to Equation-2 is described for reference.）

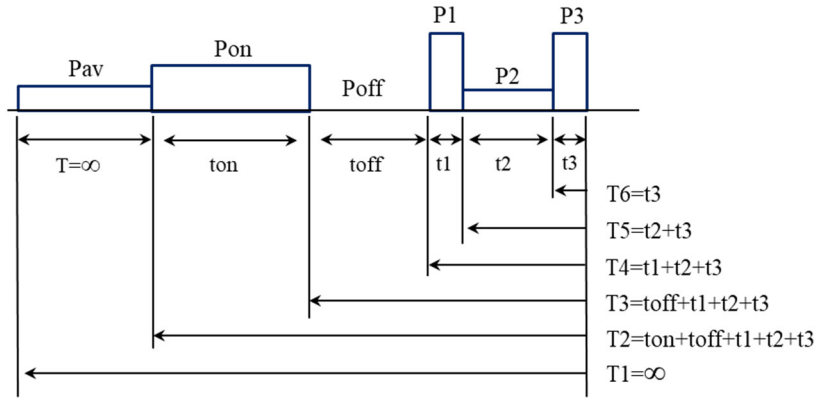


Figure 35

ΔTch=Pav・{Rth(T1)-rth(T2)}+Pon・{rth(T2)-rth(T3)}+Poff・{rth(T3)-rth(T4)}
+P1・{rth(T4)-rth(T5)}+P2・{rth(T5)-rth(T6)}+P3・rth(T6) …Fomula-2

[Conversion result from Fomula-1 to Fomula-2]

$$\Delta Tch = Pav \cdot Rth(T1) + (Pon-Pav) \cdot rth(T2) + (Poff-Pon) \cdot rth(T3) + (P1-Poff) \cdot rth(T4) + (P2-P1) \cdot rth(T5) + (P3-P2) \cdot rth(T6) \ldots \text{Fomula-1}$$

$$= Pav \cdot Rth(T1) + Pon \cdot rth(T2) - Pav \cdot rth(T2) + Poff \cdot rth(T3) - Pon \cdot rth(T3) + P1 \cdot rth(T4) - Poff \cdot rth(T4) + P2 \cdot rth(T5) - P1 \cdot rth(T5) + P3 \cdot rth(T6) - P2 \cdot rth(T6)$$

$$= Pav \cdot Rth(T1) - Pav \cdot rth(T2) + Pon \cdot rth(T2) - Pon \cdot rth(T3) + Poff \cdot rth(T3) - Poff \cdot rth(T4) + P1 \cdot rth(T4) - P1 \cdot rth(T5) + P2 \cdot rth(T5) - P2 \cdot rth(T6) + P3 \cdot rth(T6)$$

$$= Pav \cdot \{Rth(T1) - rth(T2)\} + Pon \cdot \{rth(T2) - rth(T3)\} + Poff \cdot \{rth(T3) - rth(T4)\} + P1 \cdot \{rth(T4) - rth(T5)\} + P2 \cdot \{rth(T5) - rth(T6)\} + P3 \cdot rth(T6) \ldots \text{Fomula-2}$$

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