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M16C/64 Group

Power Control Example Using Wait Mode

1. Abstract

This example shows the procedure for entering wait mode after turning the main clock off. In the sample program, the device returns from wait mode every second and after incrementing the 1-second counter, goes to wait mode again. When an INTO interrupt is generated, the device returns from wait mode and then enters high-speed mode (main clock working).

2. Introduction

The application example described in this document applies to the following MCU:

• MCU: M16C/64 group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.



3. Specification

The peripheral functions used in the sample program are listed below. Also, a power control state transition diagram is shown in Figure 1.

- Timer B2 timer mode
- $\overline{\text{INT0}}$ interrupt

A flag named "F_WIT" is used in the setup procedure. This flag is used to determine whether wait mode is to be exited.

If F_WIT = 1 in the main program, wait mode is entered; if F_WIT = 0, wait mode is not entered.

- (1) A 32.768 kHz resonator is connected to XCIN and it is used as the count source for timer B2. Every time the timer counts 1 second, a timer B2 interrupt is generated. The device returns from wait mode by this timer B2 interrupt and after counting clock pulses, goes to wait mode again. In the sample program, a RAM labeled "WATCH_CNT" is used as memory to count clock pulses.
- (2) When an INT0 interrupt request is generated, wait mode is exited. In an INT0 interrupt handler, the F_WIT flag is cleared by writing 0.

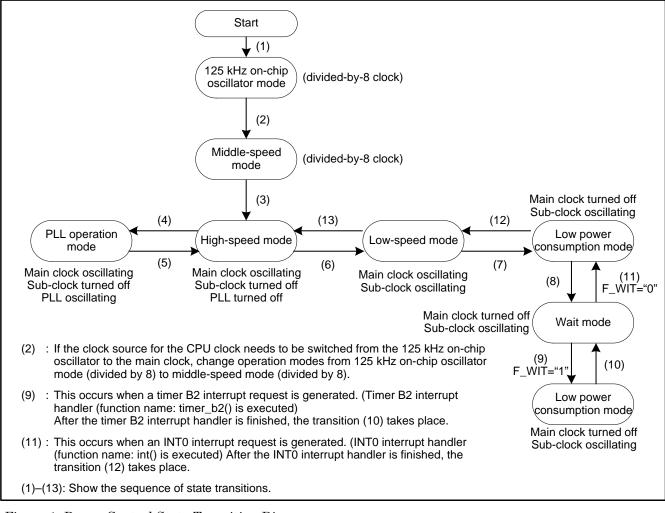


Figure 1. Power Control State Transition Diagram



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4. Operation

- (1) The clock source for the CPU clock is switched from the main clock to a sub-clock, thereby entering low-speed mode.
- (2) The main clock is turned off to enter low power consumption mode. After that, wait mode is entered by a WAIT instruction. At this time, timer B2 and INTO interrupts are enabled.
- (3) When a timer B2 interrupt request (interrupt interval of 1 second) is generated, control returns from wait mode and the CPU clock is turned back on again. At the same time, clock pulses are counted in a timer B2 interrupt handler, and then wait mode is entered again. (F_WIT flag = 1)
- (4) When an INTO interrupt request is generated, control returns from wait mode and the CPU clock is turned back on again. At the same time, the F_WIT flag is cleared (wait mode exited) by writing 0 in an INTO interrupt handler.
- (5) The main clock is started oscillating to enter low-speed mode. After that, the clock source for the CPU clock is switched from a sub-clock to the main clock, thereby entering high-speed mode.

| | | (| | | le entered | -::: | | | nting and to the | | | | |
|----------------------|---------------|-----------|-------------------------|-----------------|---------------------------|------------|-----------------|-------------|------------------|-------------|------------|---------------|---------|
| | | | : (| 2) XIN tu | | | • | | ption mode to | wait moc | ie | | |
| | | | | | (3 | B) Timer E | 32 interrupt re | quest ger | nerated | 4) INT0 in | terrupt re | quest ger | nerated |
| | | | | | | | | | (| | • | llating. Tr | |
| | | | | | | | | | | (0) | | ow-speed | |
| | | | : | ÷ | | | | | | | | peed moo | |
| XIN Oscillating | | | Turned off | | | | | | | Oscillating | | | |
| _ | | | | | | | | | | | | | |
| PLL | Oscillating | | | - | | | Turned off | | | | | | |
| r | T 1 | | | | | | | | | | | · - · | 1 |
| | Turned off | | : | : | | Os | scillating | | | | : | Turned off | |
| CPU clock | | | | <u>:</u> CIN | T | XCIN | | XCIN | T | | | VIN | 1 |
| source | PLL | XIN | | JIN E | Turned off | | Turned off | XCIN | Turned off | | | XIN | J |
| Operation | PLL | High | Low | Low | Wait mode | Low | Wait mode | Low | Wait mode | Low | Low | High |] |
| mode | | speed | speed | power Note 2 | : | Note 2 | | Note 2 | | Note 2 | speed | speed | J |
| Timer B2 overflow | | | | | İ | ٦ | ĺ | | | | | | |
| Timer B2 | | | | | | | | | | | | | - |
| interrupt | | | | | | | | | | | | | |
| handling - | | | | | | | | | | | | | - |
| —— "H" - | | | | | | | | | | | | | |
| INTO " | | | | | | | | | | | | | _ |
| - | | | | | | | | | | | | | |
| | | | t clock in bit to 0 (cl | | | k source | for the CPU cl | lock, follo | w the steps be | elow. | | | |
| | | | | | oscillation stal | hilizes | | | | | | | |
| | | | | | selected for t | | m clock). | | | | | | |
| , | | | | | | | for the system | n clock). | | | | | |
| | Set the | e CM07 I | oit to 0 (m | ain clock | , PLL clock or | 125 kHz | on-chip oscill | ator selec | cted for the sys | stem cloc | k). | | |
| | | | | | ode (CM07 bit | = 1 (sub- | clock selected | d) and CM | /105 bit = 1 (ma | ain clock | turned off | i)), registe | r |
| | | | as follows | | • • • • | | | | | | | | |
| | | | ain clock o | | -8 mode) ability HIGH) | | | | | | | | |
| • | CIVITS D | m = 1 (X) | | unve cap | | | | | | | | | |

Figure 2. Operation Timing Diagram of Wait Mode Based Power Control



5. How to Set Up

The following shows how to set up the registers to accomplish the operation described in 4, "Operation." For details about each register, see the hardware manual of the M16C/64 group.

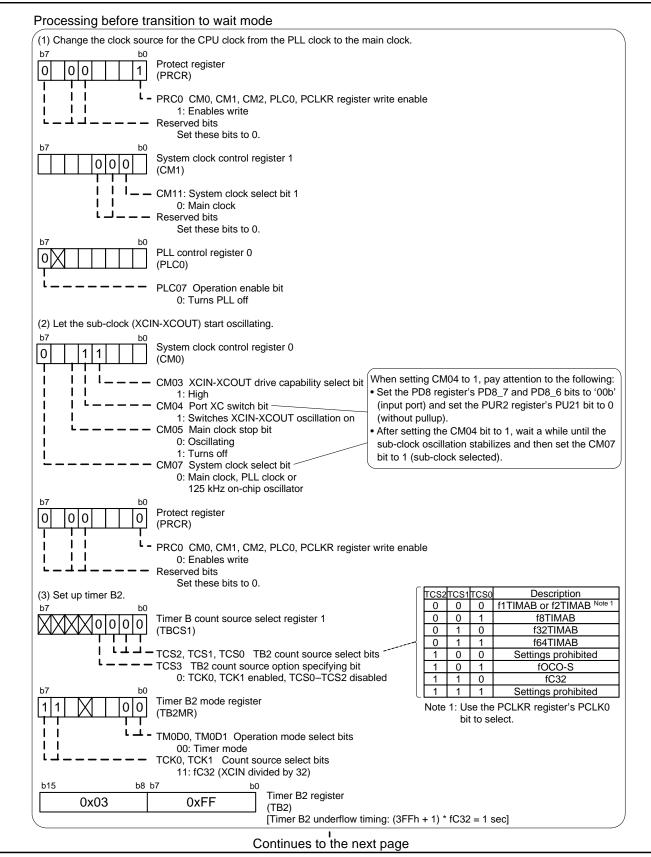


Figure 3. Procedure for Setting Up the Registers Associated with Wait Mode Based Power Control (1)



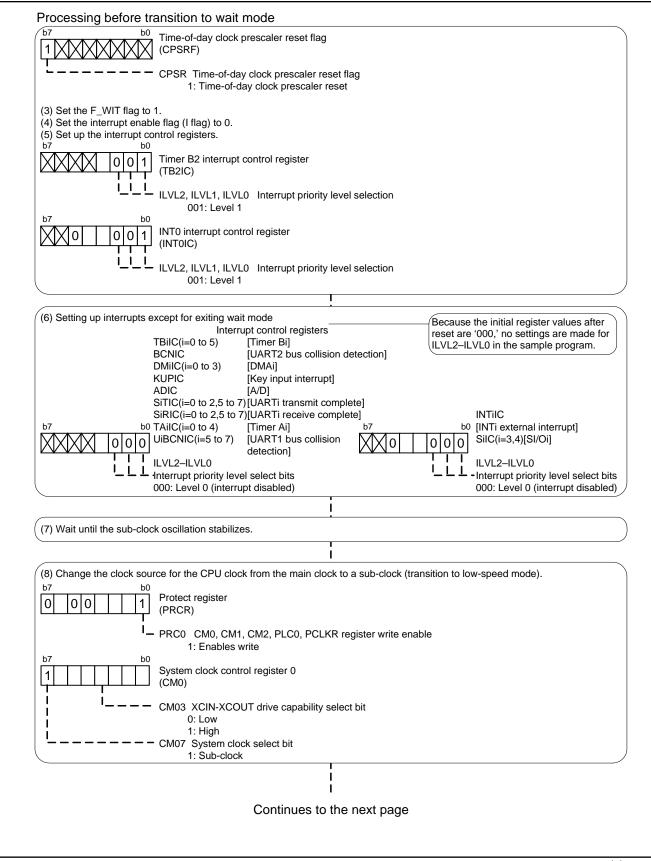


Figure 4. Procedure for Setting Up the Registers Associated with Wait Mode Based Power Control (2)



| ~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~ | ansition to wait mode | n mode) | | | |
|---|--|---|---|--|--|
| (9) Let the main clock stop b7 b0 | o oscillating (transition to low power consumption | i mode). | | | |
| | System clock control register 0 (CM0) | (If the CM07 bit = 1 (su | b-clock selected) and | | |
| i | CM05 Main clock stop bit 1: Turns off | CM05 bit = 1 (main clo settings are fixed as fo | ck turned off), register llows: | | |
| b7 b0 0 0 0 0 | Protect register (PRCR) | CM06 bit = 1 (main clock divide-by-8 mode) CM15 bit = 1 (XIN-XOUT drive capability HIGH | | | |
| ٤ ـ | PRC0 CM0, CM1, CM2, PLC0, PCLKR registe 0: Disables write | er write enable | | | |
| (10) Timer B2 starts count | ing. | | | | |
| b7 b0 Count start flag (TBSR) | | | | | |
| ' | TB2S Timer B2 count start flag 1: Count starts | | | | |
| (11) Set the interrupt enab | ble flag (I flag) to 1. | | | | |
| | (12) WAIT instruction | - n | | | |
| | (Insert at least 4 NOP instructions after | | INT0 interrupt reques | | |
| Processing after retu | | | TB2 interrupt reques | | |
| wait mode | <u>Return from wait r</u> (CPU clock turned back | | generated | | |
| | | | | | |
| (13) Main clock starts osc | illating (transition to low-speed mode). | ht ili a sama at same | en fra er ovalt er ala ia a T | | |
| b7 b0 | | | rn from wait mode is a TE WIT = 1), perform step | | |
| | Protect register (PRCR) PRC0 CM0, CM1, CM2, PLC0, PCLKR register 1: Enables write | (12), "WAIT instructer write enable | ction," again. | | |
| b7 b0 | System clock control register 0 | | | | |
| | (ĆM0) | | | | |
| · | CM05 Main clock stop bit 0: Oscillating | | | | |
| | | | | | |
| (14) Wait until the main cl | ock oscillation stabilizes. | | | | |
| | | | | | |
| b7 b0 | urce for the CPU clock from a sub-clock to the ma | ain clock (transition to high-s | peed mode). | | |
| 0 | System clock control register 0 (CM0) | | | | |
| h7 40 | CM07 System clock select bit 0: Main clock | | | | |
| ь7 ь0 | System clock control register 0 | | | | |
| | (CM0) CM06 Main clock divide ratio select bit 0: Not divided | | | | |
| ь7 ь0 | System clock control register 0 | | | | |
| | (CM0) •CM04 Port XC switch bit | | bit to 0 causes the sub- | | |
| b7 b0 | 0: Switches Xin-Xout oscillation off | clock (XCIN) stop | oscillating. | | |
| | Protect register | | | | |
| | (PRCR) PRC0 CM0, CM1, CM2, PLC0, PCLKR registe 0: Disables write | er write enable | | | |
| | | kt page | | | |

Figure 5. Procedure for Setting Up the Registers Associated with Wait Mode Based Power Control (3)



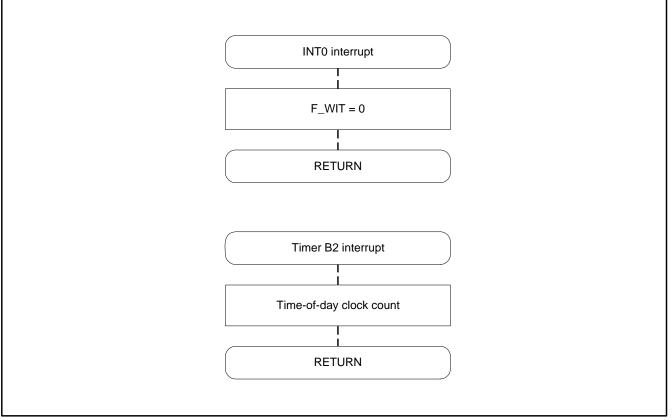


Figure 6. Procedure for Setting Up the Registers Associated with Wait Mode Based Power Control (4)



6. Sample Programming Code

A sample program can be downloaded from the Renesas Technology website. To download, click "Application Notes" in the left-hand side menu of the M16C Family page.

7. Reference Documents

Hardware manual

M16C/64 Group Hardware Manual (Get the latest version from the Renesas Technology website.)

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| 1.00 | Mar 23,2009 | - | First Edition issued | | |
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