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April 1st, 2010
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M16C/64 Group

Operation of Timer A (pulse width modulation mode, 8-bit PWM mode)

1. Abstract

In pulse width modulation mode, choose functions from those listed in Table 1. Operations of the circled items are described below.

2. Introduction

This application note is applied to the M16C/64 group microcomputers.

This program can be operated under the condition of M16C family products with the same SFR (Special Function Register) as M16C/64 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation.

3. Chosen functions

Table 1. Chosen functions

Item	Set-up	
Count source	O	Internal count source (f1TIMAB/f2TIMAB/f8TIMAB/f32TIMAB/f64TIMAB/foco-s/fc32)
PWM mode		16-bit PWM
	O	8-bit PWM
Count start condition	O	External trigger input (falling edge of input signal to the TAiIN pin)
		External trigger input (rising edge of input signal to the TAiIN pin)
		Timer overflow (TB2/TAj/TAk overflow)
Output polar control	O	Output waveform “H” active
		Output waveform “L” active (output reversed)

Note: j = i – 1, but j = 4 when i = 0; k = i + 1, but k = 0 when i = 4.

4. Operation

(1) If the TAiIN pin input level changes from “H” to “L” with the count start flag set to “1”, the counter performs a down count on the count source. Also, the TAiOUT pin outputs an “H” level.

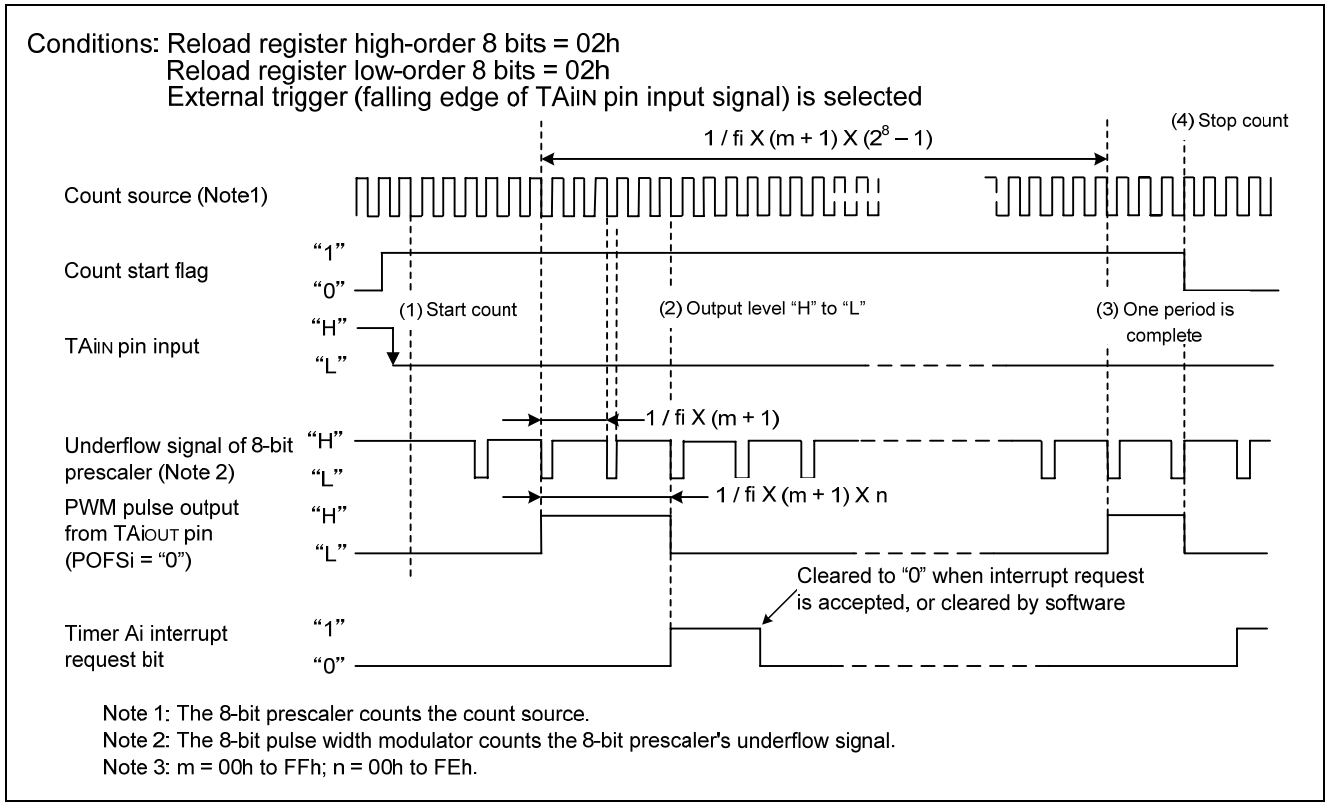
(2) The TAiOUT pin output level changes from “H” to “L” when a set time period elapses. At this time, the timer Ai interrupt request bit goes to “1”.

(3) The counter reloads the content of the reload register every time PWM pulses are output for one cycle, and continues counting.

(4) Setting the count start flag to “0” causes the counter to stop and to hold its value. Also, the TAiOUT pin outputs an “L” level.

Note:
• The period of PWM pulses becomes (m + 1) X (2^8 – 1) / fi, and the “H” level pulse width becomes n X (m + 1) / fi. If “00h” is set in the eight higher-order bits of the timer Ai register, the pulse width modulator does not work, and the TAiOUT pin outputs “L” level, therefore the timer Ai interrupt request is not generated.
(fi : frequency of the count source f1TIMAB/f2TIMAB/f8TIMAB/f32TIMAB/f64TIMAB/foco-s/fc32; m : values set to timer Ai register's low-order address n : values set to timer Ai register's high-order address)
• When a trigger is generated, the TAiOUT pin outputs “L” level of same amplitude as “H” level of the set PWM pulse, after which it starts PWM pulse output.

Figure 1 shows the operation timing.



Note 1: The 8-bit prescaler counts the count source.
Note 2: The 8-bit pulse width modulator counts the 8-bit prescaler's underflow signal.
Note 3: m = 00h to FFh; n = 00h to FEh.

Figure 1. Operation timing of pulse width modulation mode, with 8-bit PWM mode selected

5. Set-up procedure

Table 2 shows Timer A count source, Figure 2 shows block diagram of Timer A count source in timer mode.

Table 2. Count Source Selection of Timer A

TACSj register (Note 1)				TAiMR register (Note)		Count source	Count source period
TCS3/ TCS7	TCS2/ TCS6	TCS1/ TCS5	TCS0/ TCS4	TCK1	TCK0		f(PLL):24MHz f(XCIN):32.768kHz
0	-	-	-	0	0	f1TIMAB/f2TIMAB (Note 2)	41.7ns or 83.3ns
0	-	-	-	0	1	f8TIMAB	333.3ns
0	-	-	-	1	0	f32TIMAB	1333.3ns
0	-	-	-	1	1	fc32	976.56µs
1	0	0	0	-	-	f1TIMAB/f2TIMAB (Note 2)	41.7ns or 83.3ns
1	0	0	1	-	-	f8TIMAB	333.3ns
1	0	1	0	-	-	f32TIMAB	1333.3ns
1	0	1	1	-	-	f64TIMAB	2666.7ns
1	1	0	1	-	-	foco-s	About 8µs
1	1	1	0	-	-	fc32	976.56µs

Note 1: TCS3~TCS0 bits of TACS0 register correspond to Timer A0 count source selection, TCS7~TCS4 bits of TACS0 register correspond to Timer A1 count source selection, TCS3~TCS0 bits of TACS1 register correspond to Timer A2 count source selection, TCS7~TCS4 bits of TACS1 register correspond to Timer A3 count source selection, and TCS3~TCS0 bits of TACS2 register correspond to Timer A4 count source selection.
Note 2: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.

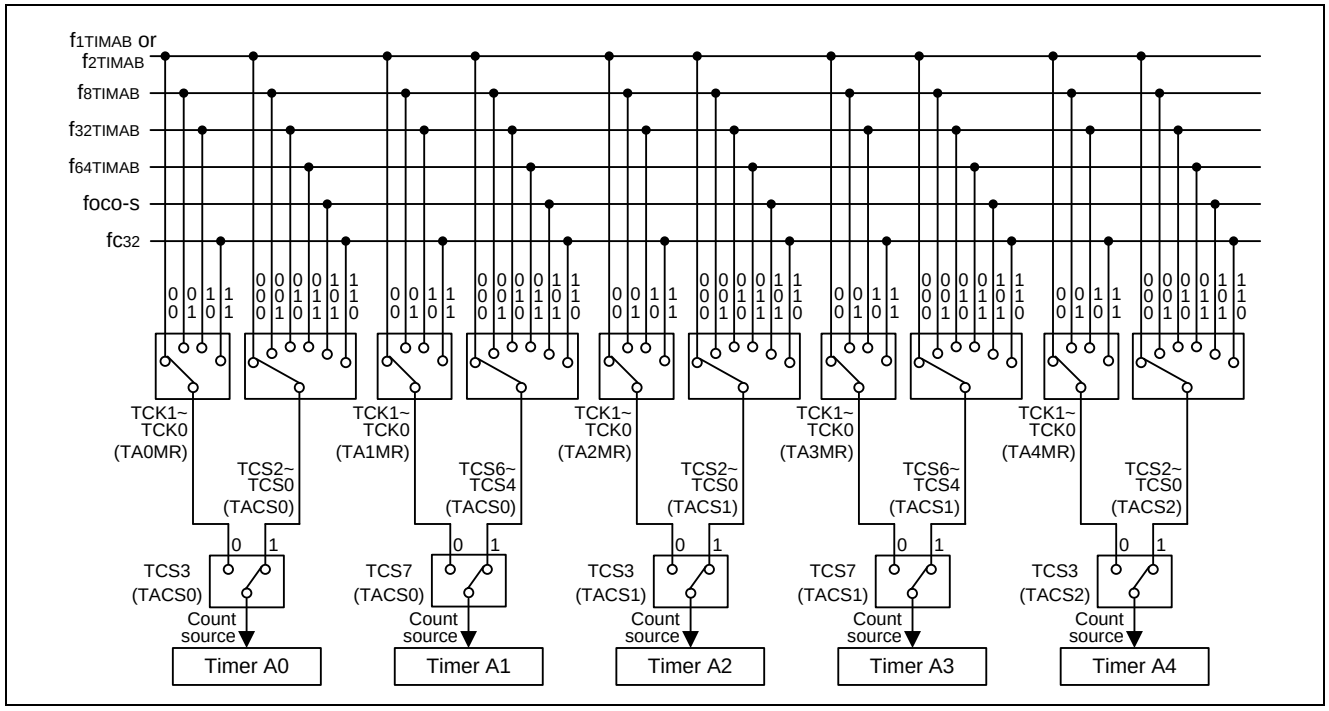
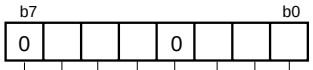


Figure 2. Count source of Timer A

Selecting timer count source

TACS0 register can select Timer A0 and Timer A1 count source, TACS1 can select Timer A2 and Timer A3 count source, and TACS2 can select Timer A4 count suorce.



Timer A count source select register 0 [Address 01D0h] TACS0
Timer A count source select register 1 [Address 01D1h] TACS1

TAi count source select bit (Note1)

b2 b1 b0
0 0 0 : f_{1TIMAB} or f_{2TIMAB} (Note2)
0 0 1 : f_{8TIMAB}
0 1 0 : $f_{32TIMAB}$
0 1 1 : $f_{64TIMSB}$
1 0 0 : Do not set
1 0 1 : foco-s
1 1 0 : f_{C32}
1 1 1 : Do not set

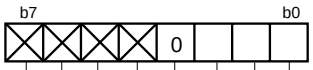
TAi count source option specified bit (Note1)
0 : TCK0, TCK1 enabled, TCS0 to TCS2 disabled

TAj count source select bit (Note1)

b2 b1 b0
0 0 0 : f_{1TIMAB} or f_{2TIMAB} (Note2)
0 0 1 : f_{8TIMAB}
0 1 0 : $f_{32TIMAB}$
0 1 1 : $f_{64TIMSB}$
1 0 0 : Do not set
1 0 1 : foco-s
1 1 0 : f_{C32}
1 1 1 : Do not set

TAj count source option specified bit (Note1)
0 : TCK0, TCK1 enabled, TCS4 to TCS6 disabled

TACS0 register: i = 0, j = 1, TACS1 register: i = 2, j = 3
Note 1: About the count source period, please refer to Table 2.
Note 2: When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is f_{1TIMAB}. When the PCLK0 bit is “0”, the selected clock source is f_{2TIMAB}.



Timer A count source select register 2 [Address 01D2h] TACS2

TA4 count source select bit (Note1)

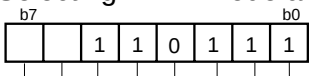
b2 b1 b0
0 0 0 : f_{1TIMAB} or f_{2TIMAB} (Note2)
0 0 1 : f_{8TIMAB}
0 1 0 : $f_{32TIMAB}$
0 1 1 : $f_{64TIMSB}$
1 0 0 : Do not set
1 0 1 : foco-s
1 1 0 : f_{C32}
1 1 1 : Do not set

TA4 count source option specified bit (Note1)
0 : TCK0, TCK1 enabled, TCS0 to TCS2 disabled

No register bits. If necessary, set to 0. Read as undefined value.

Note 1: About the count source period, please refer to Table 2.
Note 2: When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is f_{1TIMAB}. When the PCLK0 bit is “0”, the selected clock source is f_{2TIMAB}.

Selecting PWM mode and functions



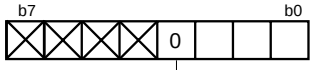
Timer Ai mode register (i=0 to 4) [Address 0336h to 033Ah]
TAiMR (i=0 to 4)

Selection of PWM mode
1 (Must always be "1" in PWM mode)
External trigger select bit
0 : Falling edge of input signal to TAiIN pin (Note 1)
Trigger select bit
1 : Selected by event/trigger select register
16/8-bit PWM mode select bit
1 : Functions as a 8-bit pulse width modulator
Count source select bit (Note 2)
b7 b6
0 0 : f_{1TIMAB} or f_{2TIMAB} (Note 3)
0 1 : f_{8TIMAB}
1 0 : $f_{32TIMAB}$
1 1 : fc_{32}

Note 1: Valid when bits TAiTGH and TAiTGL bit in the ONSF register or TRGSR register are set to 00b (TAi_{IN} pin input). Please set the port direction bit for the TAi_{IN} pin to 0 (input mode).
Note 2: Valid when the TCS3 bit or TCS7 bit in registers TACS0 to TACS2 is set to 0 (TCK0, TCK1 enabled). About the count source period, please refer to Table 2.
Note 3: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f_{1TIMAB}. When the PCLK0 bit is "0", the selected clock source is f_{2TIMAB}.

Clearing timer Ai interrupt request bit

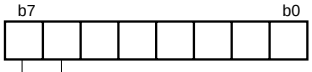
Refer to 'Precaution for Timer A (pulse width modulation mode)'



Timer Ai interrupt control register [Address 0055h to 0059h]
TAiIC (i=0 to 4)

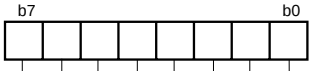
Interrupt request bit

Setting event/trigger select bit



One-shot start flag [Address 0322h]
ONSF

Timer A0 event/trigger select bit
b7 b6
0 0 : Input on $TA0_{IN}$ is selected (Note1)

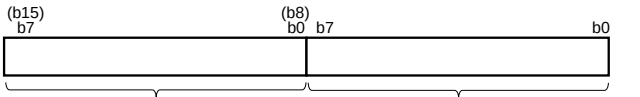


Trigger select register [Address 0323h]
TRGSR

Timer A1 event/trigger select bit
b1 b0
0 0 : Input on $TA1_{IN}$ is selected (Note 1)
Timer A2 event/trigger select bit
b3 b2
0 0 : Input on $TA2_{IN}$ is selected (Note 1)
Timer A3 event/trigger select bit
b5 b4
0 0 : Input on $TA3_{IN}$ is selected (Note 1)
Timer A4 event/trigger select bit
b7 b6
0 0 : Input on $TA4_{IN}$ is selected (Note 1)

Note 1: Set the port direction bits for the pins $TA0_{IN}$ to $TA4_{IN}$ to 0 (input mode).

Setting PWM pulse's period and "H" level width

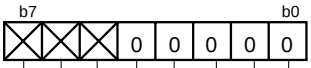


Timer A0 register [Address 0327h, 0326h] TA0
Timer A1 register [Address 0329h, 0328h] TA1
Timer A2 register [Address 032Bh, 032Ah] TA2
Timer A3 register [Address 032Dh, 032Ch] TA3
Timer A4 register [Address 032Fh, 032Eh] TA4

Can be set to 00h to FFh: m

Can be set to 00h to FEh: n

Selecting waveform output function



Timer A waveform output function select register [Address 01D5h]
TAPOFS

TA0OUT output polar control bit
0 : Output waveform "H" active

TA1OUT output polar control bit
0 : Output waveform "H" active

TA2OUT output polar control bit
0 : Output waveform "H" active

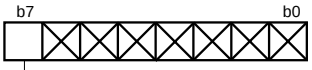
TA3OUT output polar control bit
0 : Output waveform "H" active

TA4OUT output polar control bit
0 : Output waveform "H" active

No register bits. If necessary, set to 0. Read as undefined value

Setting clock prescaler reset flag

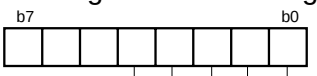
(This function is effective when f_{C32} is selected as the count source. Reset the prescaler for generating f_{C32} by dividing the X_{CIN} by 32.)



Count prescaler reset flag [Address 0015h]
CPSRF

Clock prescaler reset flag
0 : No effect
1 : Prescaler is reset (When read, the value is "0")

Setting count starts flag



Count start flag [Address 0320h]
TABSR

Timer A0 count start flag

Timer A1 count start flag

Timer A2 count start flag

Timer A3 count start flag

Timer A4 count start flag

Start count

6. Reference

Hardware manual

M16C/64 Group Hardware Manual

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