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M32C/84 Group

Operation of Timer B (pulse width measurement mode)

1. Abstract

In pulse period/pulse width measurement mode, choose functions from those listed in Table 1. Operations of the circled items are described below. Figure 1 shows the operation timing, and Figure 2 shows the set-up procedure. A reference program is an example when using the Timer B0 interrupt based on the setting procedure of Figure 2.

2. Introduction

This application note is applied to the M32C/84 group Microcomputers.

This program can be operated under the condition of M16C family products with the same SFR(Special Function Register) as M32C/84 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation



Choosed functions

Table 1. Choosed functions

Item	Set-up		
Count source	0	Internal count source (f1 / f8 / f2n / fc32)	
Measurement		Pulse period measurement (interval between measurement pulse falling edge to falling edge)	
mode		Pulse period measurement (interval between measurement pulse rising edge to rising edge)	
	o	Pulse width measurement (interval between measurement pulse falling edge to rising edge, and between rising edge to falling edge)	

4. Operation

- (1) Setting the count start flag to "1" causes the counter to start counting the count source.
- (2) If an effective edge of a pulse to be measured is input, the value of the counter goes to "0000h", and measurement is started. In this instance, an indeterminate value is transferred to the reload register. The timer Bi interrupt request does not generate.
- (3) If an effective edge of a pulse to be measured is input again, the value of the counter is transferred to the reload register, and the timer Bi interrupt request bit goes to "1". Then the value of the counter becomes "0000h", and measurement is started again.

Note

- The timer Bi interrupt request bit goes to "1" when an effective edge of a pulse to be measured is input or timer Bi is overflows. The factor of interrupt request can be determined by use of the timer Bi overflow flag within the interrupt routine.
- The value of the counter at the beginning of a count is indeterminate. Therefore, the timer Bi overflow flag may go to "1" and timer Bi interrupt request may be generated during the interval between a count start and an effective edge input.
- The timer Bi overflow flag is indeterminate after reset. The timer Bi overflow flag goes to "0" if timer Bi mode register is written to when the count start flag is "1". This flag cannot be set to "1" by software.
- Set TBilN pin's function select register A to I/O port and port direction register to "0".

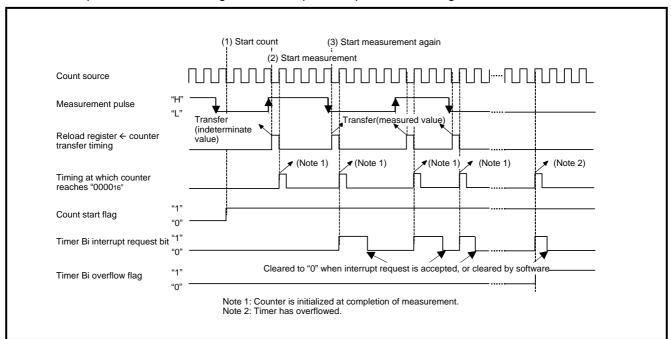


Figure 1. Operation timing of pulse width measurement mode



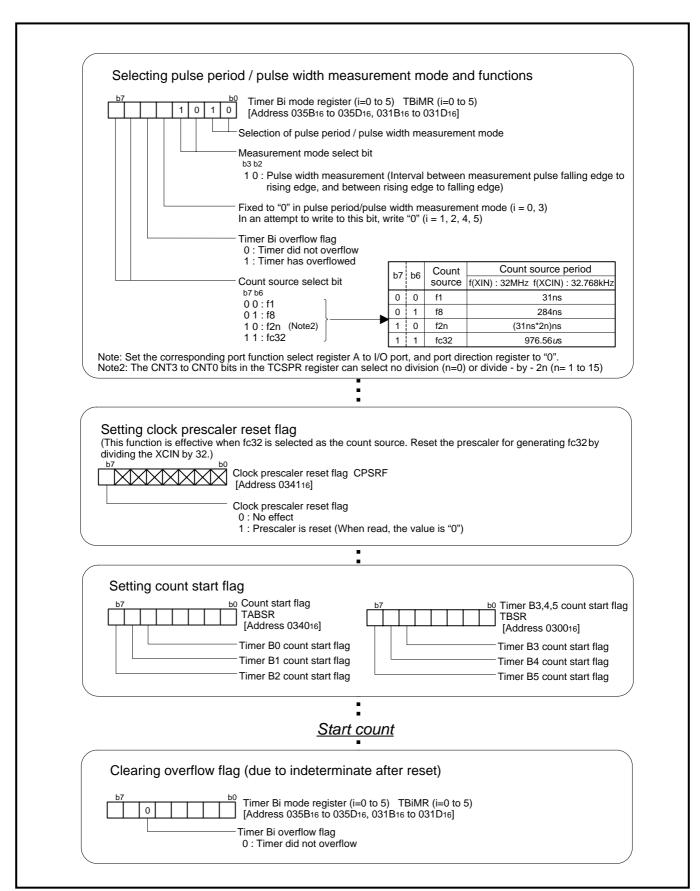


Figure 2. Set-up procedure of pulse width measurement mode



5. The example of reference program

```
M32C/84 Program Collection
   FILE NAME: rjj05b0716_src.a30
   CPU
              : M32C/84 Group
   FUNCTION: Operation of Timer B (pulse width measurement)
   HISTORY : 2005.1.31 Ver 1.00
   Copyright(C)2005, Renesas Technology Corp.
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   All rights reserved.
      .LIST
                                        ;Stops outputting lines to the assembler list file
      .INCLUDE sfr32c84.inc
                                        ;Reads the file that defined SFR
      .LIST
                                        ;Starts outputting lines to the assembler list file
                  on
       Symbol definition
   **************************
RAM TOP
                               000400h
                                                ;Start address of RAM
                       .equ
RAM_END
                               002affh
                                                :End address of RAM
                       .equ
ROM_TOP
                               0fe0000h
                                                ;Start address of ROM
                       .equ
VECT TOP
                       .equ
                               0fffe00h
                                                ;Start address of vect top
FIXED_VECT_TOP
                       .equ
                               0ffffdch
                                                ;Start address of fixed_vect_top
       Program area
       Start up
        .SECTION
                                                ;Declares section name and section type
                     PROGRAM, CODE
        .ORG
                     ROM_TOP
                                                ;Declares start address
START:
      ldc
                       #RAM_END+1,isp
                                                ;Sets interrupt stack pointer
      mov.b
                       #03h, prcr
                                                ;Removes protect
                       #0000000b, pm0
                                                ;Single-chip mode
      mov.b
                       #0000000b, pm1
      mov.b
```



```
#00001000b, cm0
                                               ;Xcin-Xcout High
      mov.b
                      #0010000b, cm1
      mov.b
      mov.b
                      #00010010b, mcd
                                               ;No division mode
      mov.b
                      #00h, prcr
                                               ;Protects all registers
                      #VECT_TOP,intb
      ldc
                                               ;Sets interrupt table register
       Main program
      mov.b
                      #0000000b,tcspr
                                               ;Count source prescaler register
                            ++++----;No division
      mov.b
                      #1000000b,tcspr
                        +----;Divider start
      mov.b
                       #01001010b,tb0mr
                                               ;Timer B0 mode register
                        |||||++----;Pulse period/pulsewidgh measurement mode
                        | | | | ++-----; Pulse width measurement (measurement between
                                               ;a falling edge and the next rising edge of measured
                                               ;pulse and between a rising edge and the next
                        \Pi\Pi\Pi
                                               ;falling edge)
                        \Pi\Pi\Pi
                        | | | +-----;Set to"0"in pulse period and pulse widge
                                               ;measurement mode
                        | | +-----; Timer has not overflowed
                        ++----;Count source(f8)
      mov.b
                      #04H, prcr
                                               ;Removes protect
      bclr
                      pd9_0
                                               ;(Note)Set the corresponding port direction register to "0"
      bclr
                      ps3_0
                                               ;Port P9_0 is I/O port
                                               ;Protects all registers
      mov.b
                      #00h,prcr
                      #0000011b,tb0ic
                                               ;Interrupt control register
      mov.b
                            |+++----;Interrupt priority level select bit
                                               ;(011:Level 3, interrupt disabled)
                               -----;Interrupt request bit (0:interrupt not requested)
      mov.b
                      #00100000b,tabsr
                                               ;Count start flag
                          +----;Starts counting
      fset
                                               ;Set interrupt enable flag
      mov.b
                      #01001010b,tb0mr
                                               ;Timer B0 mode register
                            -----;Timer did not overflowed
MAIN:
      jmp
                      MAIN
       Interrupt program
TB0 INT:
              ;/ TB0_INT interrupt routine /
```



reit							
; :=======	=======================================						
; Dummy interrupt processing program							
;=====================================	=======================================						
reit							
;							
.*************************************	**************************************	*******************					
, Setting of var	iable vector table *******	******					
,							
.SECTION	VECT,ROMDATA						
.ORG	VECT_TOP + (8*4)						
; .lword	DUMMY	;DMA0 interrupt vector					
.lword	DUMMY	;DMA1 interrupt vector					
.lword	DUMMY	;DMA2 interrupt vector					
.lword	DUMMY	;DMA3 interrupt vector					
.lword	DUMMY	;TA0 interrupt vector					
.lword	DUMMY	;TA1 interrupt vector					
.lword	DUMMY	;TA2 interrupt vector					
.lword	DUMMY	;TA3 interrupt vector					
.lword	DUMMY	;TA4 interrupt vector					
.lword	DUMMY	;UART0 transmit/NACK interrupt vector					
.lword	DUMMY	;UART0 receive/ACK interrupt vector					
.lword	DUMMY	;UART1 transmit/NACK interrupt vector					
.lword	DUMMY	;UART1 receive/ACK interrupt vector					
.lword	TB0_INT	;TB0 interrupt vector					
.lword	DUMMY	;TB1 interrupt vector					
.lword	DUMMY	;TB2 interrupt vector					
.lword	DUMMY	;TB3 interrupt vector					
.lword	DUMMY	;TB4 interrupt vector					
.lword	DUMMY	;INT5 interrupt vector					
.lword	DUMMY	;INT4 interrupt vector					
.lword	DUMMY	;INT3 interrupt vector					
.lword	DUMMY	;INT2 interrupt vector					
.lword	DUMMY	;INT1 interrupt vector					
.lword	DUMMY	;INT0 interrupt vector					
.lword	DUMMY	;TB5 interrupt vector					
.lword	DUMMY	;UART2 transmit/NACK interrupt vector					
.lword	DUMMY	;UART2 receive/ACK interrupt vector					
.lword	DUMMY	;UART3 transmit/NACK interrupt vector					
.lword	DUMMY	;UART3 receive/ACK interrupt vector					
.lword	DUMMY	;UART4 transmit/NACK interrupt vector					
.lword	DUMMY	;UART4 receive/ACK interrupt vector					
.lword	DUMMY	;Bus collision detection,start/stop					



		;condition detection (UART2) interrupt vector
.lword	DUMMY	;Bus collision detection,start/stop
		;condition detection (UART3) interrupt vector
.lword	DUMMY	;Bus collision detection,start/stop
		;condition detection (UART4) interrupt vector
.lword	DUMMY	;A-D interrupt vector
.lword	DUMMY	;KEY interrupt vector
.lword	DUMMY	;IntelligentI/O interrupt vector0
.lword	DUMMY	;IntelligentI/O interrupt vector1
.lword	DUMMY	;IntelligentI/O interrupt vector2
.lword	DUMMY	;IntelligentI/O interrupt vector3
.lword	DUMMY	;IntelligentI/O interrupt vector4
.lword	DUMMY	;IntelligentI/O interrupt vector8
.lword	DUMMY	;IntelligentI/O interrupt vector9,CAN0
.lword	DUMMY	;IntelligentI/O interrupt vector10,CAN1
.lword	DUMMY	;CAN2
;		
.**************	**********	*********
; Setting of fixed		************
; Setting of fixed		
; Setting of fixed	d vector	
; Setting of fixed	d vector	
; Setting of fixed;	d vector ************************************	
Setting of fixed	d vector F_VECT,ROMDATA	
Setting of fixed	d vector F_VECT,ROMDATA	
Setting of fixed; SECTION ORG	d vector F_VECT,ROMDATA FIXED_VECT_TOP	*************
; Setting of fixed; ;******;; ; .SECTION .ORG ;	d vector F_VECT,ROMDATA FIXED_VECT_TOP DUMMY	;Undefined instruction interrupt vector
Setting of fixed SECTION ORG Ilword	d vector F_VECT,ROMDATA FIXED_VECT_TOP DUMMY DUMMY	;Undefined instruction interrupt vector ;Overflow interrupt vector
Setting of fixed SECTION ORG Liword Liword Liword	F_VECT,ROMDATA FIXED_VECT_TOP DUMMY DUMMY DUMMY	;Undefined instruction interrupt vector ;Overflow interrupt vector ;BRK instruction interrupt vector
Setting of fixed SECTION ORG Ilword Ilword Ilword Ilword	d vector F_VECT,ROMDATA FIXED_VECT_TOP DUMMY DUMMY DUMMY DUMMY DUMMY	;Undefined instruction interrupt vector ;Overflow interrupt vector ;BRK instruction interrupt vector
Setting of fixed SECTION ORG Iword Iword Iword Iword Iword	F_VECT,ROMDATA FIXED_VECT_TOP DUMMY DUMMY DUMMY DUMMY DUMMY DUMMY DUMMY DUMMY	;Undefined instruction interrupt vector ;Overflow interrupt vector ;BRK instruction interrupt vector ;Address match interrupt vector ;
Setting of fixed SECTION ORG Iword Iword Iword Iword Iword Iword Iword Iword	F_VECT,ROMDATA FIXED_VECT_TOP DUMMY	;Undefined instruction interrupt vector ;Overflow interrupt vector ;BRK instruction interrupt vector ;Address match interrupt vector ;
Setting of fixed SECTION ORG Iword Iword Iword Iword Iword Iword Iword Iword	F_VECT,ROMDATA FIXED_VECT_TOP DUMMY	;Undefined instruction interrupt vector ;Overflow interrupt vector ;BRK instruction interrupt vector ;Address match interrupt vector ; ;Watchdog timer interrupt vector ;
; Setting of fixed; ; *****************; .SECTION .ORG ; .lword	F_VECT,ROMDATA FIXED_VECT_TOP DUMMY	;Undefined instruction interrupt vector ;Overflow interrupt vector ;BRK instruction interrupt vector ;Address match interrupt vector ; ;Watchdog timer interrupt vector ; ;NMI interrupt vector



6. Referense

Hardware manual
M32C/84 group (Tentative version) Hardware Manual Rev.0.50
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7. Web-site and contact for support

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