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M32C/84 Group

Operation of Key-Input Interrupt

1. Abstract

The following is an operation of key-input interrupt. Figure 1 shows an example of a circuit that uses the key-input interrupt, Figure 2 shows an example of operation of key-input interrupt, and Figure 3 shows the setting procedure of key-input interrupt.

2. Introduction

This application note is applied to the M32C/84 group Microcomputers.

This program can be operated under the condition of M16C family products with the same SFR(Special Function Register) as M32C/84 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation

3. Specifications

Use the following peripheral functions:

- Key-input interrupts
- Stop mode
- Pull-up function

(1) Use P10_0 through P10_3 for the scan output pins of a key matrix. Use the input pins (KI0 through KI3) of the key-input interrupt function for the key-input reading pins. The pull-up function is also used.
(2) If a key-input interrupt request occurs, clear the stop mode and read a key.

4. Operation

(1) Set the direction register of the ports to be changed to key-input interrupt pins to input, and set the pull-up function.
(2) Setting the key-input interrupt control register and setting the interrupt enable flag makes the interrupt-enabled state ready.
(3) If a falling edge is input to either KI0 through KI3, the key-input interrupt request bit goes to “1”.

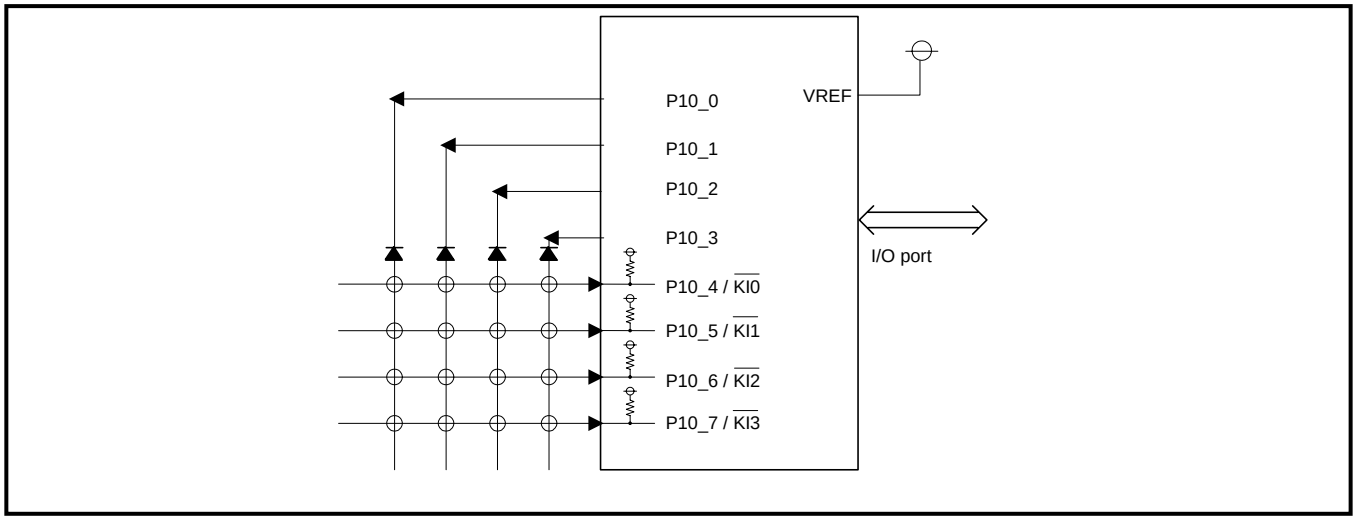

Figure 1. Example of circuit using the key-input interrupt

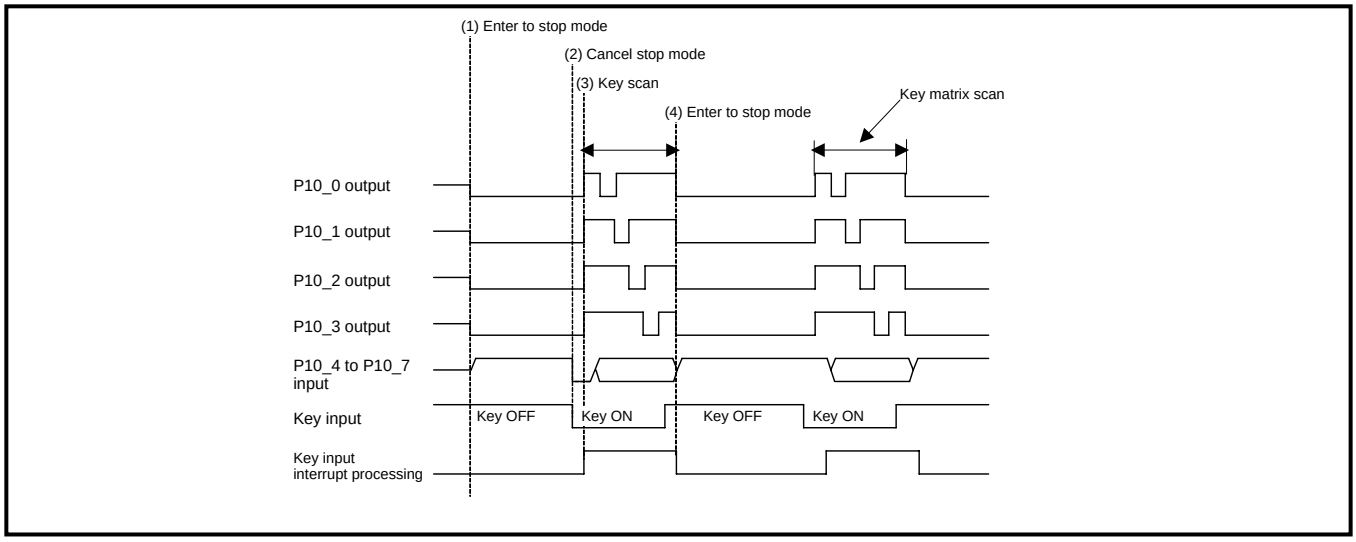

Figure 2. Example of operation of key-input interrupt

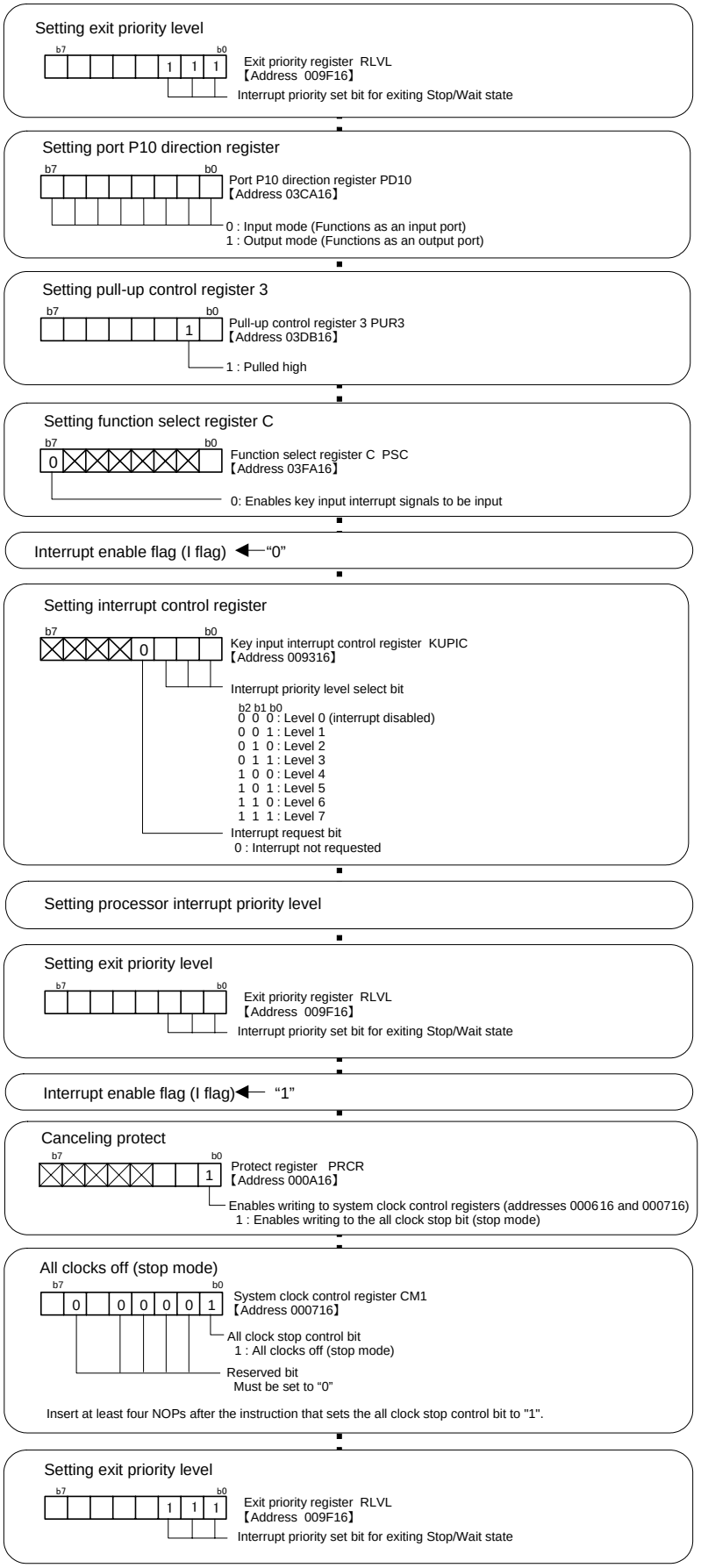

Figure 3. Set-up procedure of key-input interrupt

5. The example of reference program

```
;***************************************************************************
;
;    M32C/84 Program Collection
;
;    FILE NAME : rjj05b0766_src.a30
;    CPU       : M32C/84 Group
;    FUNCTION  : Operation of Key-Input Interrupt
;    HISTORY   : 2005.4.7    Ver 1.00
;
;    Copyright(C)2005, Renesas Technology Corp.
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;    All rights reserved.
;
;***************************************************************************
;***************************************************************************
;         Include
;***************************************************************************
;
        .LIST       off                 ;Stops outputting lines to the assembler list file
        .INCLUDE    sfr32c84.inc        ;Reads the file that defined SFR
        .LIST       on                  ;Starts outputting lines to the assembler list file
;
;***************************************************************************
;         Symbol definition
;***************************************************************************
RAM_TOP             .equ    000400h         ;Start address of RAM
RAM_END             .equ    002affh         ;End address of RAM
ROM_TOP             .equ    0fe0000h        ;Start address of ROM
VECT_TOP            .equ    0fffe00h        ;Start address of vect_top
FIXED_VECT_TOP      .equ    0ffffdch        ;Start address of fixed_vect_top
;***************************************************************************
;         Program area
;***************************************************************************
;=========================================================================
;         Start up
;=========================================================================
        .SECTION    PROGRAM, CODE       ;Declares section name and section type
        .ORG        ROM_TOP             ;Declares start address
START:
        ldc         #RAM_END+1,isp      ;Sets interrupt stack pointer
        mov.b       #03h, prcr          ;Removes protect
        mov.b       #00000000b, pm0     ;Single-chip mode
        mov.b       #00000000b, pm1     ;
        mov.b       #00001000b, cm0     ;Xcin-Xcout High
        mov.b       #00100000b, cm1     ;
```

```
        mov.b       #00010010b, mcd     ;No division mode
        mov.b       #00h, prcr          ;Protects all registers
        ldc         #VECT_TOP,intb      ;Sets interrupt table register
;
;=============================================================================
;         Main program
;=============================================================================
INIT:
        mov.b       #00000111b,rlvl     ;M16C-97-0303(Japanese) countermeasure
;                           | | |       ;M16C-97-0307(Engish) countermeasure
;                           | | |       ;Exit priority register
;                           +++---------;Interrupt priority set bit for exiting stop/wait state
                                        ;(111:Level 7, interrupt disabled)
MAIN:
;
        mov.b       #00h,p10            ;"L"level
        mov.b       #00001111b,pd10     ;Setting port direction register
;                     | | | |++++-------;Output mode
;                     ++++--------------;Input mode
        mov.b       #00000010b,pur3     ;Setting pull-up control register 3
;                         +-------------;Pulled high
                                        ;(p10_4 - p10_7)
        mov.b       #00000000b,psc      ;Setting function select register C
;                     +-----------------;Enable key input interrupt signals to be input
        fclr        i
        mov.b       #00000101b,kupic    ;Interrupt control register
;                       |+++-----------;Interrupt priority level select bit
;                       |               ;(101:Level 5, interrupt disabled)
;                       +-------------;Interrupt request bit (0:Interrupt not requested)
        ldipl       #3                  ;Intterrupt permission level: 0
        mov.b       #00000011b,rlvl     ;Exit priority register
;                           +++---------;Interrupt priority set bit for exiting stop/wait state
                                        ;(011:Level 3, interrupt disabled)
        fset        i                   ;Set Interrupt enable flag
;
STOP:
;
        mov.b       #00000001b,prcr     ;Removes protect
        bset        cm10                ;Stop mode
        mov.b       #00000000b,prcr     ;Protects all registers
        jmp.b       MAIN_A              ;TN-16C-124A/JA(Japanese) countermeasure
;                                       ;TN-16C-124A/EA(English) countermeasure
MAIN_A:
;
        nop
        nop
        nop
```

```
        nop
;
MAIN_B:
;
        jmp             MAIN_B
;
;=============================================================================
;         Interrupt program
;=============================================================================
KEY_INT:
;
        mov.b           #00000111b,rlvl         ;Exit priority register
;                               +++-------------;Interrupt priority set bit for exiting stop/wait state
;                                               ;(111:Level 7, interrupt disabled)
        reit
;=============================================================================
;         Dummy interrupt processing program
;=============================================================================
DUMMY:
                reit
;
;*****************************************************************************
;         Setting of variable vector table
;*****************************************************************************
        .SECTION        VECT,ROMDATA
        .ORG            VECT_TOP + (8*4)
;
        .lword                  DUMMY           ;DMA0 interrupt vector
        .lword                  DUMMY           ;DMA1 interrupt vector
        .lword                  DUMMY           ;DMA2 interrupt vector
        .lword                  DUMMY           ;DMA3 interrupt vector
        .lword                  DUMMY           ;TA0 interrupt vector
        .lword                  DUMMY           ;TA1 interrupt vector
        .lword                  DUMMY           ;TA2 interrupt vector
        .lword                  DUMMY           ;TA3 interrupt vector
        .lword                  DUMMY           ;TA4 interrupt vector
        .lword                  DUMMY           ;UART0 transmit/NACK interrupt vector
        .lword                  DUMMY           ;UART0 receive/ACK interrupt vector
        .lword                  DUMMY           ;UART1 transmit/NACK interrupt vector
        .lword                  DUMMY           ;UART1 receive/ACK interrupt vector
        .lword                  DUMMY           ;TB0 interrupt vector
        .lword                  DUMMY           ;TB1 interrupt vector
        .lword                  DUMMY           ;TB2 interrupt vector
        .lword                  DUMMY           ;TB3 interrupt vector
        .lword                  DUMMY           ;TB4 interrupt vector
        .lword                  DUMMY           ;INT5 interrupt vector
        .lword                  DUMMY           ;INT4 interrupt vector
```

```
        .lword                  DUMMY           ;INT3 interrupt vector
        .lword                  DUMMY           ;INT2 interrupt vector
        .lword                  DUMMY           ;INT1 interrupt vector
        .lword                  DUMMY           ;INT0 interrupt vector
        .lword                  DUMMY           ;TB5 interrupt vector
        .lword                  DUMMY           ;UART2 transmit/NACK interrupt vector
        .lword                  DUMMY           ;UART2 receive/ACK interrupt vector
        .lword                  DUMMY           ;UART3 transmit/NACK interrupt vector
        .lword                  DUMMY           ;UART3 receive/ACK interrupt vector
        .lword                  DUMMY           ;UART4 transmit/NACK interrupt vector
        .lword                  DUMMY           ;UART4 receive/ACK interrupt vector
        .lword                  DUMMY           ;Bus collision detection,start/stop
                                                ;condition detection (UART2) interrupt vector
        .lword                  DUMMY           ;Bus collision detection,start/stop
                                                ;condition detection (UART3) interrupt vector
        .lword                  DUMMY           ;Bus collision detection,start/stop
                                                ;condition detection (UART4) interrupt vector
        .lword                  DUMMY           ;A-D interrupt vector
        .lword                  KEY_INT         ;KEY interrupt vector
        .lword                  DUMMY           ;IntelligentI/O interrupt vector0
        .lword                  DUMMY           ;IntelligentI/O interrupt vector1
        .lword                  DUMMY           ;IntelligentI/O interrupt vector2
        .lword                  DUMMY           ;IntelligentI/O interrupt vector3
        .lword                  DUMMY           ;IntelligentI/O interrupt vector4
        .lword                  DUMMY           ;IntelligentI/O interrupt vector8
        .lword                  DUMMY           ;IntelligentI/O interrupt vector9,CAN0
        .lword                  DUMMY           ;IntelligentI/O interrupt vector10,CAN1
        .lword                  DUMMY           ;CAN2
;
;*****************************************************************************
;           Setting of fixed vector
;*****************************************************************************
;
        .SECTION        F_VECT,ROMDATA
        .ORG            FIXED_VECT_TOP
;
        .lword                  DUMMY           ;Undefined instruction interrupt vector
        .lword                  DUMMY           ;Overflow (INTO instruction) interrupt vector
        .lword                  DUMMY           ;BRK instruction interrupt vector
        .lword                  DUMMY           ;Address match interrupt vector
        .lword                  DUMMY           ;
        .lword                  DUMMY           ;Watchdog timer interrupt vector
        .lword                  DUMMY           ;
        .lword                  DUMMY           ;NMI interrupt vector
        .lword                  START           ;Sets start vector
;
        .end
```

6. Referense

Hardware manual

M32C/84 group Hardware Manual

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Revision

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		Page	Point
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