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M16C/65 Group

Operation of DMAC (repeated transfer mode)

1. Abstract

In repeat transfer mode, choose functions from the items shown in Table 1. Operations of the circled items are described below.

2. Introduction

This application note is applied to the M16C/65 group microcomputers.

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Chosen functions

Table 1. Chosen functions

Item	Set-up	
Transfer space		Fixed address from an arbitrary 1 M bytes space
	O	Arbitrary 1 M bytes space from a fixed address
		Fixed address from fixed address
Unit of transfer		8 bits
	O	16 bits
Repeat transfer mode		Single transfer
	O	Repeat transfer
Source address direction	O	Fixed
		Forward
Destination address direction		Fixed
	O	Forward

4. Operations

(1) When software trigger is selected, setting software DMA request bit to “1” generates a DMA transfer request signal.

(2) If DMAC is active, data transfer starts, and the contents of the address indicated by the DMAi source pointer are transferred to the address indicated by the DMAi forward-direction address pointer. When data transfer starts directly after DMAC becomes active, the value of the DMAi transfer counter reload register is reloaded to the DMAi transfer counter, and the value of the DMAi destination pointer is reloaded to the DMAi forward-direction address pointer. Each time a DMA transfer request signal is generated, 2 byte of data is transferred. The DMAi transfer counter is down counted, and the DMAi forward-direction address pointer is up counted.

(3) Though DMAi transfer counter is underflowed, DMA enable bit is still “1”. The DMA interrupt request bit changes to “1” simultaneously.

(4) After DMAi transfer counter is underflowed, when the next DMA request is generated, DMA transfer is repeated from (1).

Figure 1 shows an example of operation

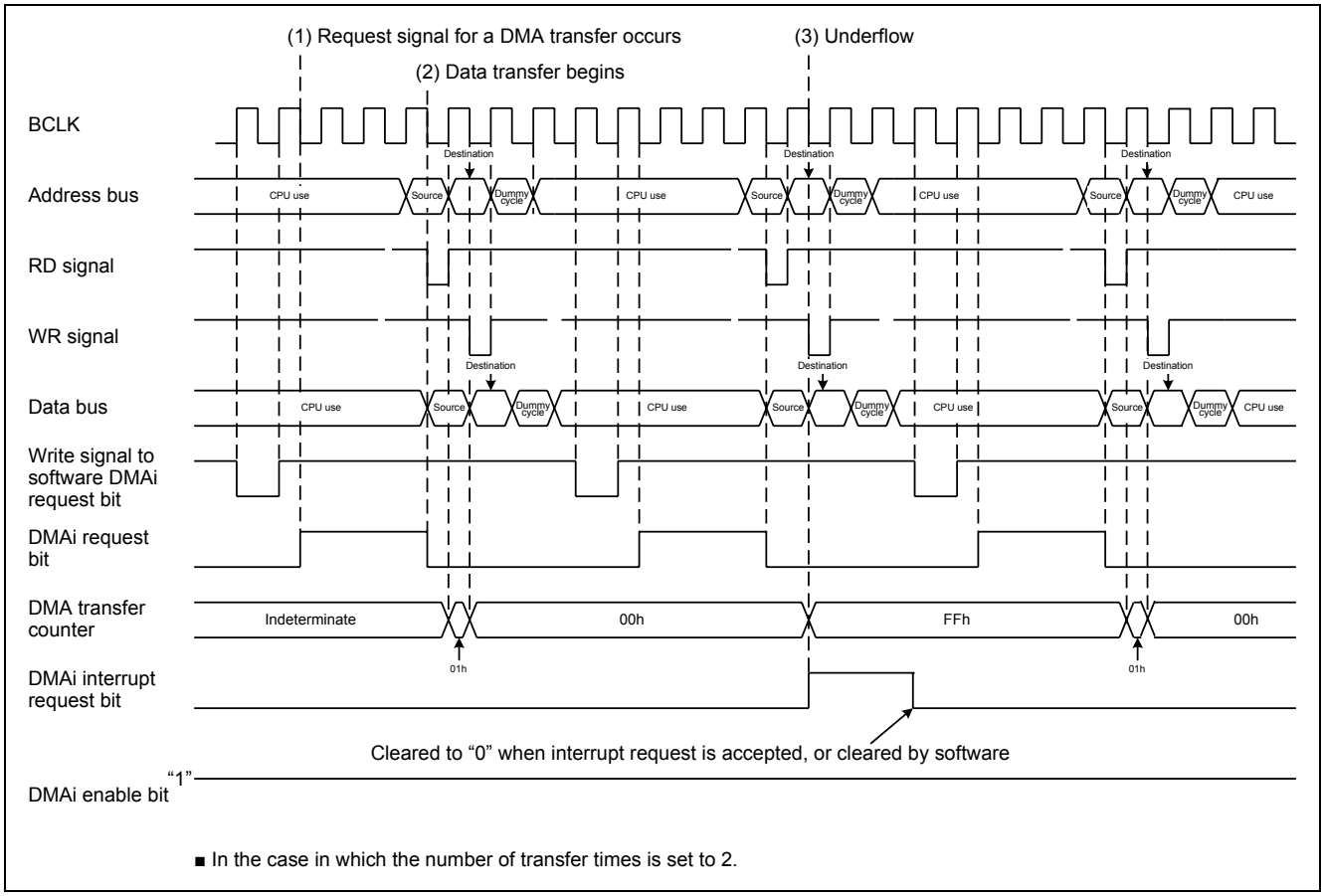
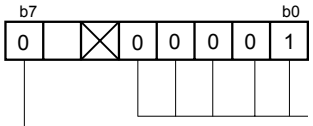


Figure 1. Example of operation of repeated transfer mode

5. Set-up procedure

Setting DMAi request cause select register

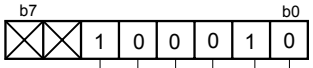


DMA0 request cause select register [Address 0398h] DM0SL
DMA1 request cause select register [Address 039Ah] DM1SL
DMA2 request cause select register [Address 0390h] DM2SL
DMA3 request cause select register [Address 0392h] DM3SL

DMA request cause select bit
b4 b3 b2 b1 b0
0 0 0 0 1 : Software trigger

Software DMA request bit
Set to "0"

Setting DMAi control register



DMA0 control register [Address 018Ch] DM0CON
DMA1 control register [Address 019Ch] DM1CON
DMA2 control register [Address 01ACh] DM2CON
DMA3 control register [Address 01BCh] DM3CON

Transfer unit bit select bit
0 : 16 bits

Repeat transfer mode select bit
1 : Repeat transfer

DMA request bit
0 : DMA not requested

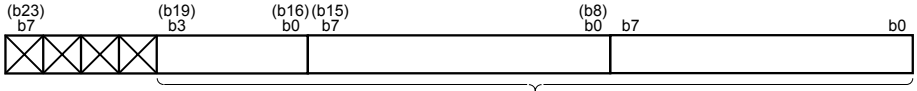
DMA enable bit
0 : Disabled

Source address direction select bit
0 : Fixed (Bit 4 and bit 5 cannot be set to "1" simultaneously)

Destination address direction select bit
1 : Forward (Bit 4 and bit 5 cannot be set to "1" simultaneously)

Setting DMAi source pointer

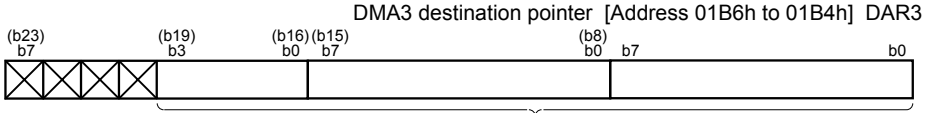
DMA0 source pointer [Address 0182h to 0180h] SAR0
DMA1 source pointer [Address 0192h to 0190h] SAR1
DMA2 source pointer [Address 01A2h to 01A0h] SAR2
DMA3 source pointer [Address 01B2h to 01B0h] SAR3



Source pointer
Stores the source address

Setting DMAi destination pointer

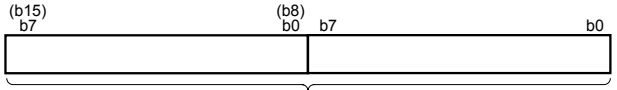
DMA0 destination pointer [Address 0186h to 0184h] DAR0
DMA1 destination pointer [Address 0196h to 0194h] DAR1
DMA2 destination pointer [Address 01A6h to 01A4h] DAR2
DMA3 destination pointer [Address 01B6h to 01B4h] DAR3



Destination pointer
Stores the destination address

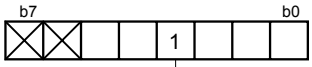
Setting DMAi transfer counter

DMA0 transfer counter [Address 0189h to 0188h] TCR0
DMA1 transfer counter [Address 0199h to 0198h] TCR1
DMA2 transfer counter [Address 01A9h to 01A8h] TCR2
DMA3 transfer counter [Address 01B9h to 01B8h] TCR3



Transfer counter
Set a value one less than the transfer count

Setting DMAi control register



DMA0 control register [Address 018Ch] DM0CON
DMA1 control register [Address 019Ch] DM1CON
DMA2 control register [Address 01ACh] DM2CON
DMA3 control register [Address 01BCh] DM3CON

DMA enable bit
1 : Enabled

Note: Clear DMA request bit simultaneously again.

When software DMA request bit = “1”

Start DMA transmission

6. Reference

Hardware manual

M16C/65 Group Hardware Manual
(Use the most recent version of the document on the Renesas Technology Web site.)

Technical news/Technical update

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