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## M16C/64 Group

### Operation of DMAC (one-shot transfer mode)

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#### 1. Abstract

In one-shot transfer mode, choose functions from the items shown in Table 1. Operations of the circled items are described below.

#### 2. Introduction

This application note is applied to the M16C/64 group microcomputers.

This program can be operated under the condition of M16C family products with the same SFR (Special Function Register) as M16C/64 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation.

### 3. Chosen functions

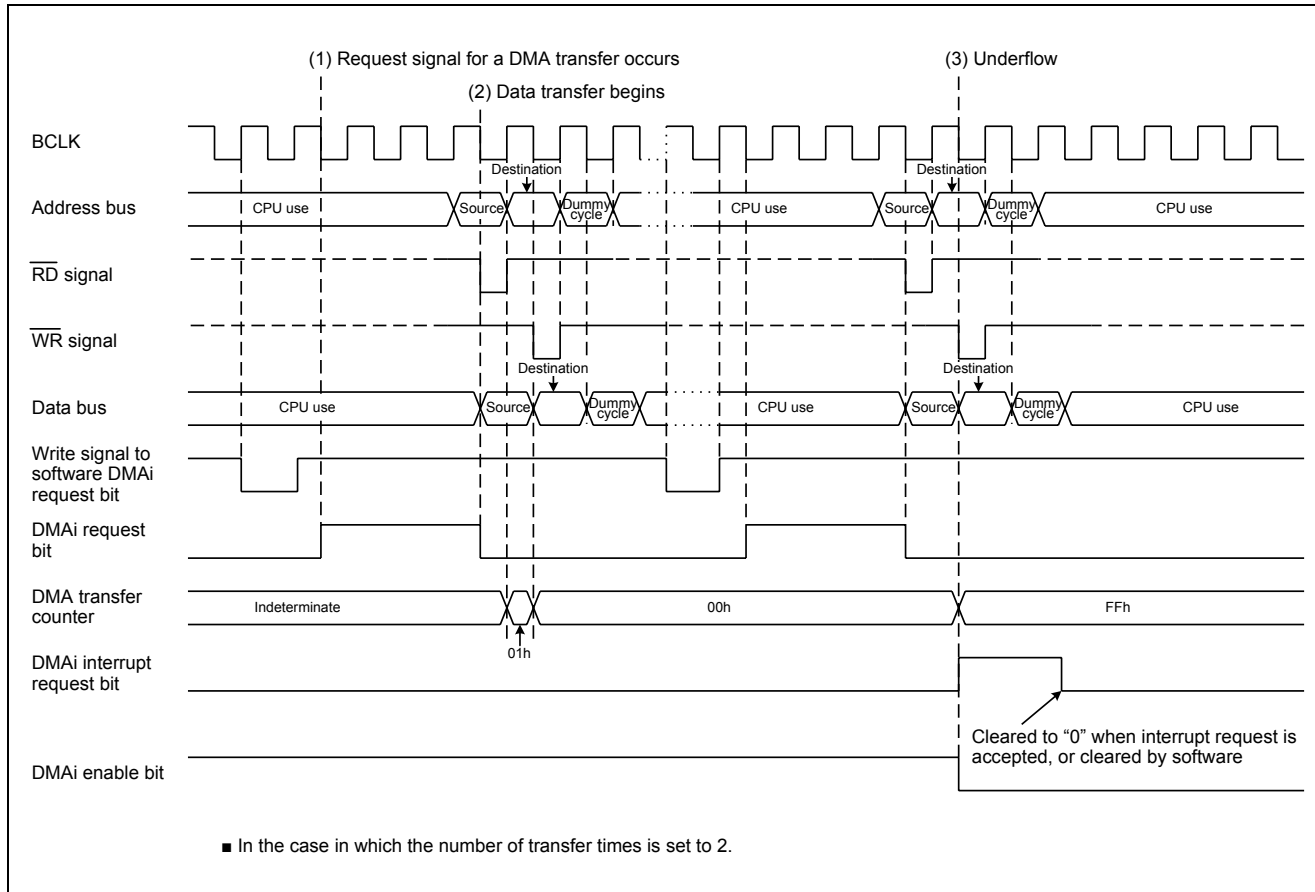
**Table 1. Chosen functions**

Item	Set-up	
Transfer space	O	Fixed address from an arbitrary 1 M bytes space
		Arbitrary 1 M bytes space from a fixed address
		Fixed address from fixed address
Unit of transfer	O	8 bits
		16 bits

### 4. Operation

- (1) When software trigger is selected, setting software DMA request bit to “1” generates a DMA transfer request signal.
- (2) If DMAC is active, data transfer starts, and the contents of the address indicated by the DMAi forward-direction address pointer are transferred to the address indicated by the DMAi destination pointer. When data transfer starts directly after DMAC becomes active, the value of the DMAi transfer counter reload register is reloaded to the DMAi transfer counter, and the value of the DMAi source pointer is reloaded by the DMAi forward-direction address pointer. Each time a DMA transfer request signal is generated, 1 byte of data is transferred. The DMAi transfer counter is down counted, and the DMAi forward-direction address pointer is up counted.
- (3) If the DMA transfer counter underflows, the DMA enable bit changes to “0” and DMA transfer is completed. The DMA interrupt request bit changes to “1” simultaneously.

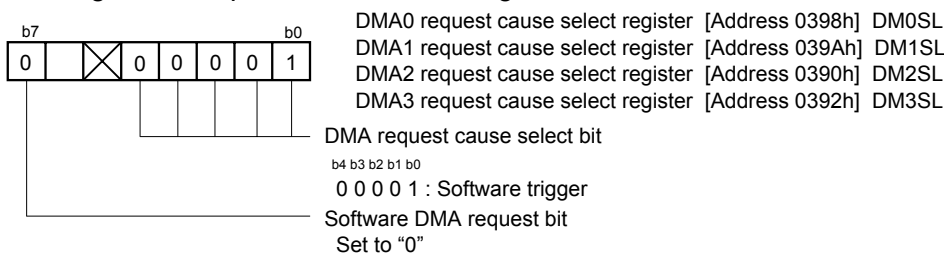
Figure 1 shows an example of operation



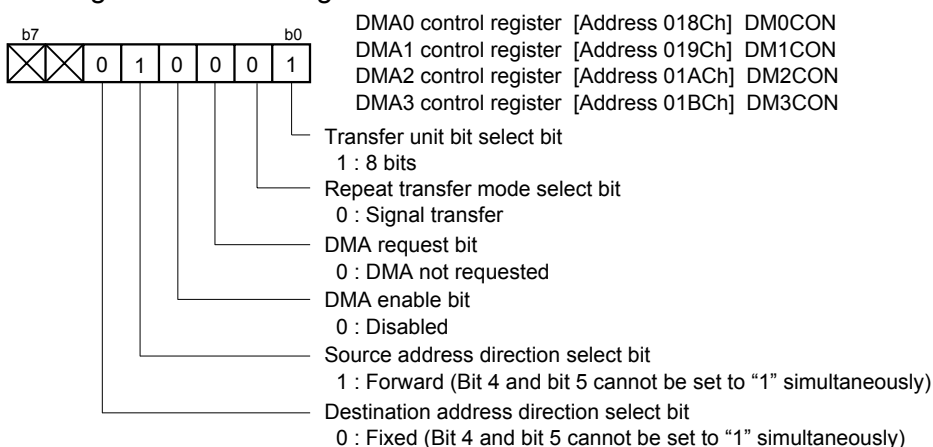
**Figure 1. Example of operation of one-shot transfer mode**

### 5. Set-up procedure

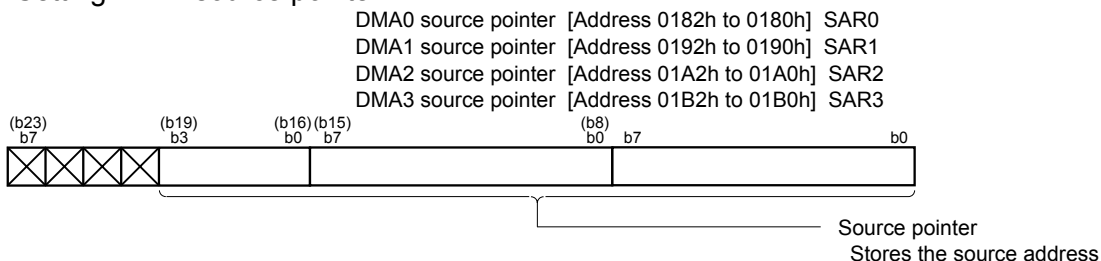
#### Setting DMAi request cause select register



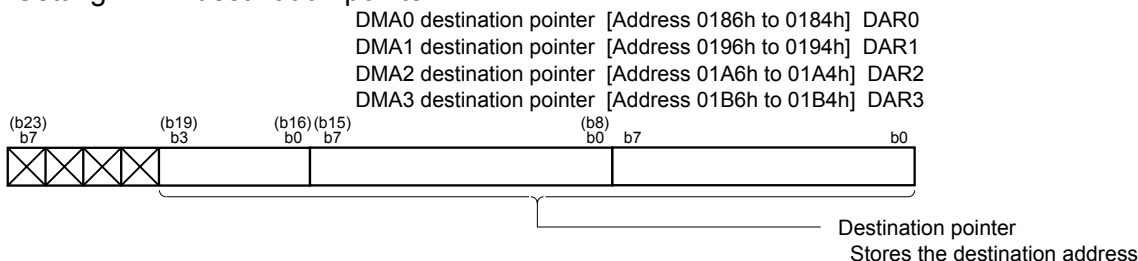
#### Setting DMAi control register



#### Setting DMAi source pointer

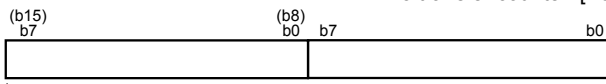


#### Setting DMAi destination pointer



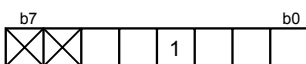
### Setting DMAi transfer counter

DMA0 transfer counter [Address 0189h to 0188h] TCR0  
 DMA1 transfer counter [Address 0199h to 0198h] TCR1  
 DMA2 transfer counter [Address 01A9h to 01A8h] TCR2  
 DMA3 transfer counter [Address 01B9h to 01B8h] TCR3



Transfer counter  
 Set a value one less than the transfer count

### Setting DMAi control register



DMA0 control register [Address 018Ch] DM0CON  
 DMA1 control register [Address 019Ch] DM1CON  
 DMA2 control register [Address 01ACh] DM2CON  
 DMA3 control register [Address 01BCh] DM3CON

DMA enable bit  
 1 : Enabled

Note: Clear DMA request bit simultaneously again.

When software DMA request bit = "1"

Start DMA transmission

## 6. Reference

### Hardware manual

M16C/64 Group Hardware Manual

(Use the most recent version of the document on the Renesas Technology Web site.)

### Technical news/Technical update

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## Revision

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		Page	Point
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