M16C/63, 64A, 65, 65C, 6C, 5LD, 5L, and 5M Groups

Serial Interface Special Mode 2
Slave Communication

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1. Abstract

This document describes an example of slave reception using serial interface special mode 2.

2. Introduction

The application example described in this document applies to the following microcomputers (MCUs):

- MCUs: M16C/63 Group, M16C/64A Group, M16C/65 Group, M16C/65C Group, M16C/6C Group, M16C/5LD Group, M16C/5L Group, M16C/5M Group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above groups. Check the user's manuals for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Operation Confirmation Conditions

Table 3.1 lists the Operation Confirmation Conditions.

Table 3.1 Operation Confirmation Conditions

Item	Contents
MCU used	M16C/65 Group
Operating frequency	• Main clock: 8 MHz • CPU clock: 32 MHz (PLL clock divided by 2 and multiply-by-8)
Operating voltage	5.0 V (operation enabled from 2.7 to 5.5 V)
Integrated development environment	Renesas Electronics High-performance Embedded Workshop Version 4.07
C complier	Renesas Electronics M16C Series, R8C Family C Compiler Package V.5.45 Release 01
	Compile options -c -finfo -dir "$(CONFIGDIR)" The default settings of the integrated development environment are used.

4. Hardware

4.1 Pins Used

Table 4.1 lists the Pins Used and Their Functions.

Table 4.1 Pins Used and Their Functions

Pin Name	I/O	Function
P8_2 / $\overline{\text{INT0}}$	Input	Port to control data reception
P7_2 / CLK2	Input	Transmit/receive clock input
P7_1 / RXD2	Input	Serial data input
P7_0 / TXD2	Output	Serial data output

4.2 Circuit Diagram

Figure 4.1 shows a Master and Slave Connection Example.

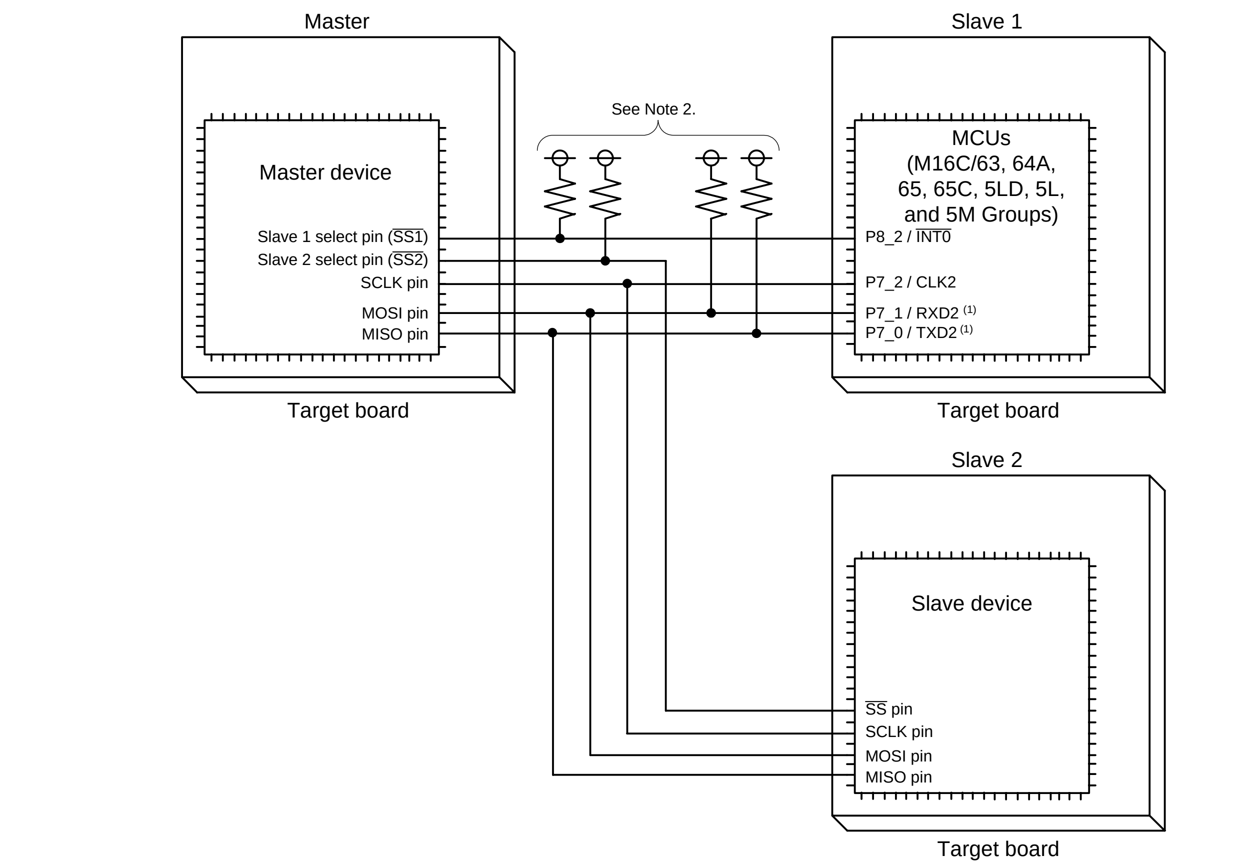


Figure 4.1 Master and Slave Connection Example

5. Software

5.1 Specifications

The sample code performs slave reception of 1-byte data.
When the falling edge is input to the $\overline{\text{INT0}}$ pin, the transmission and reception of UART2 is enabled. After 1-byte data is received, the received data is stored to relocatable variables in the UART2 received interrupt. When the rising edge is input to the $\overline{\text{INT0}}$ pin, the transmission and reception of UART2 and the serial interface are disabled.
Table 5.1 lists the Sample Code Specifications.

Table 5.1 Sample Code Specifications

Item	Slave (Without Clock Delay)	Slave (With Clock Delay)
Communication mode	Special mode 2 (external clock)	
Clock phase	The CKPH bit in the U2SMR3 register is 0 (no clock delay).	The CKPH bit in the U2SMR3 register is 1 (with clock delay).
	The CKPOL bit in the U2C0 register is 0 (transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge).	
Data format	Character length: 8 bits	
Bit order	LSB first	
Transmit/receive control	P8_2 pin ($\overline{\text{INT0}}$ pin)	
Interrupts	• UART2 reception interrupt (priority level: 2) • INT0 interrupt (priority level: 1)	

5.2 Notes

When the following conditions apply, execute the countermeasure listed in “5.3 Operation”.

- When the CKPOL bit in the UiC0 register is 0, and CKPH bit in the UiSMR3 register is 1 (i = 0 to 2 and 5 to 7).
- When the CKPOL bit is 1, and CKPH bit is 0.

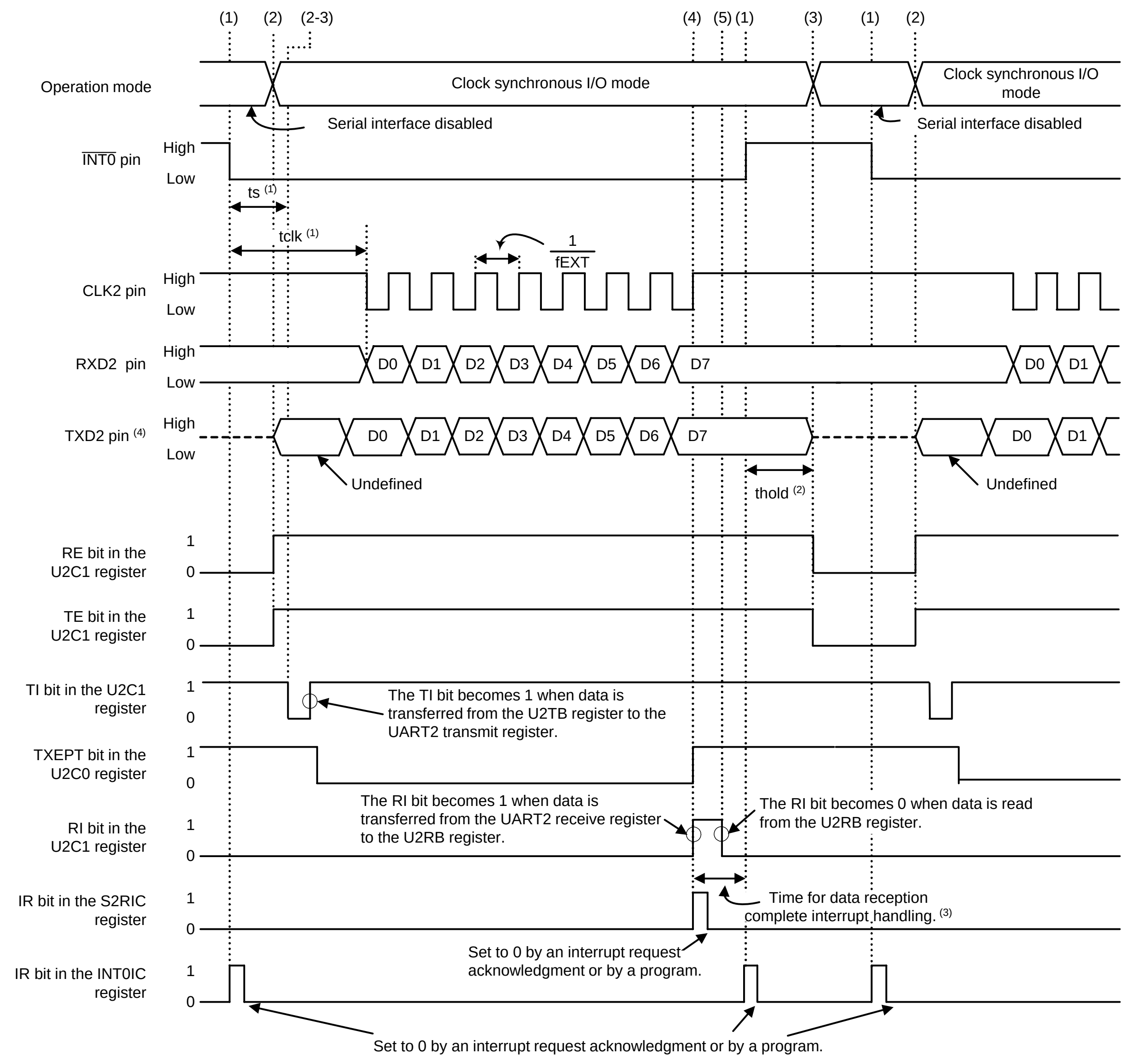
When the CKPOL bit is 0 and the CKPH bit is 1 (with clock delay), the CLKi pin is low while the communication path is idle (when the CKPOL bit is 1 and CKPH bit is 0, the CLKi pin is high).

5.3 Operation With No Clock Delay

Figure 5.1 shows an Example of Slave Transmission/Reception Using Special Mode 2 With No Clock Delay, and Table 5.2 lists the Measurement Values Using the Sample Code.

(1) The $\overline{\text{INT0}}$ interrupt ($\overline{\text{SS}}$ input) is generated.
(2) When the $\overline{\text{INT0}}$ pin is low:
(2-1) The U2MR register is set to 09h (clock synchronous serial I/O mode, external clock). (The TXD pin becomes output hereat.)
(2-2) The U2Cl register is set to 05h (transmission and reception enabled).
(2-3) Data is written to the U2TB register. (1)
(3) When the $\overline{\text{INT0}}$ pin is high:
(3-1) The U2C1 register is set to 00h (transmission and reception disabled).
(3-2) The U2MR register is set to 00h (serial interface disabled). (2) (The TXD pin is released hereat.)
(4) When the received data is transferred to the U2RB register, the RI bit in the U2C1 register becomes 1 and a reception interrupt is generated.
(5) Data is read from the U2RB register in the reception interrupt.

Notes:
1. Until process (2-3) is done, do not input the transmit/receive clock to the CLK2 pin.
2. Until the serial interface is disabled, the TXD2 pin retains the last data.



fEXT: External clock frequency

The above diagram applies under the following conditions:
- The CKPOL bit in the U2C0 register is 0 (transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge).
- The CKPH bit in the U2SMR3 register is 0 (no clock delay).

Notes:
1. Set to tclk > ts. Do not input the transmit/receive clock to the CLK2 pin during tclk.
2. The TXD2 pin retains the last data during thold.
3. After the data reception completed interrupt handling and data transmission completed interrupt handling are done, control the master to drive the INT0 pin high.
4. Set to the port direction register corresponding to the TXD2 pin to constantly be in input mode.

Figure 5.1 Example of Slave Transmission/Reception Using Special Mode 2 With No Clock Delay

Table 5.2 Measured Values Using the Sample Code (1)

Item	Measured Value	Cycle
ts	Approximately 4.6 µs	Approximately 147 cycles
thold	Approximately 4.4 µs	Approximately 141 cycles
Time for data reception complete interrupt handling	Approximately 2.6 µs	Approximately 83 cycles

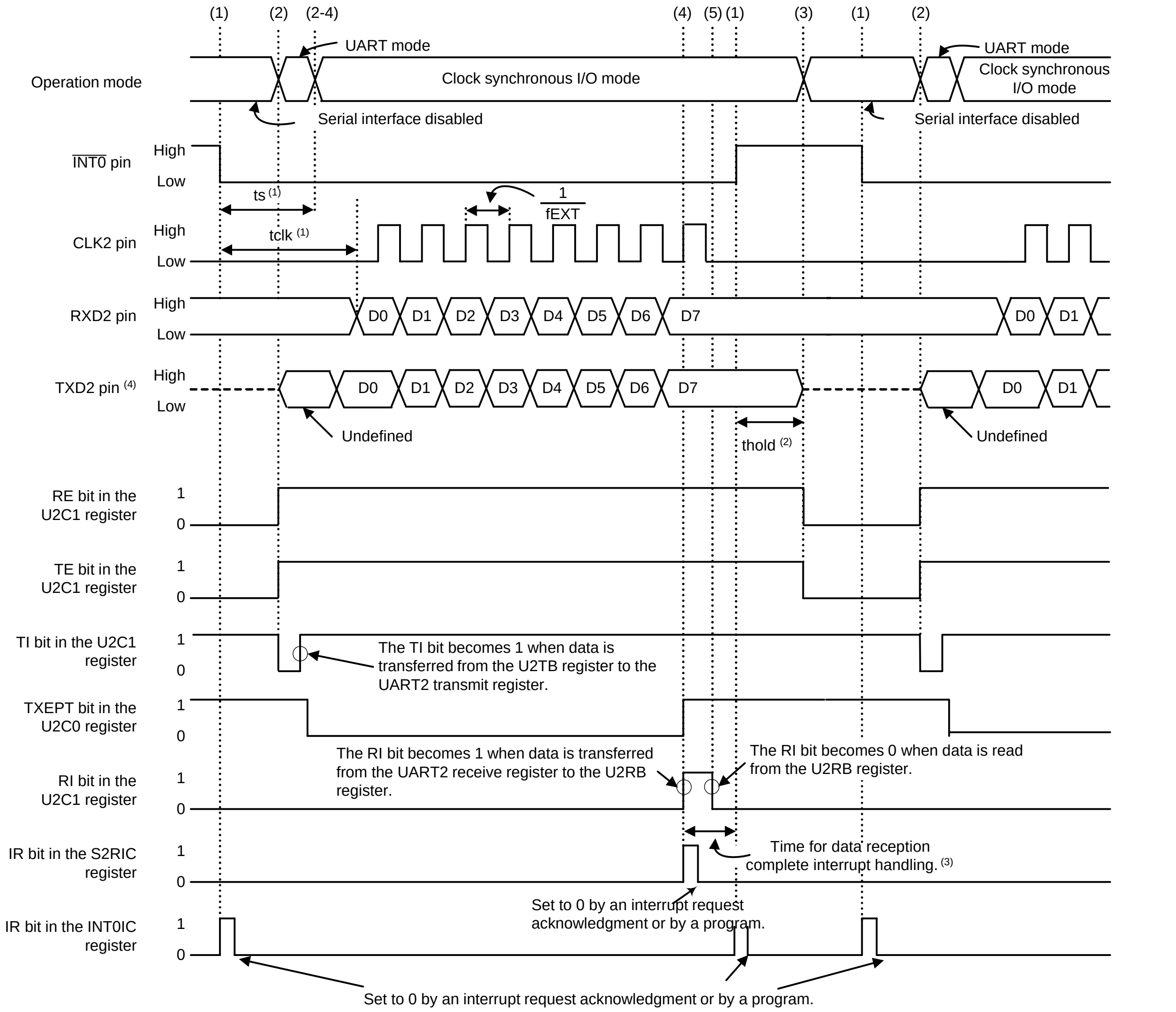
Note:
1. The conditions for measuring the values are the same as “3. Operation Confirmation Conditions”. The measured values and number of cycles are modified depending on the compiler option settings and interrupt generation timing.

5.4 Operation With Clock Delay

Figure 5.2 shows an Example of Slave Transmission/Reception Using Special Mode 2 With a Clock Delay, and Table 5.3 lists the Measured Values Using the Sample Code.

(1) The $\overline{\text{INT0}}$ interrupt ($\overline{\text{SS}}$ input) is generated.
(2) When the $\overline{\text{INT0}}$ pin is low:
(2-1) The U2MR register is set to 0Dh (UART mode, external clock). [1] (The TXD pin becomes output hereat.)
(2-2) The U2Cl register is set to 05h (transmission and reception enabled).
(2-3) Data is written to the U2TB register. [1]
(2-4) The U2MR register is set to 09h (clock synchronous serial I/O mode). [2]
(3) When the $\overline{\text{INT0}}$ pin is high.
(3-1) The U2C1 register is set to 00h (transmission and reception disabled).
(3-2) The U2MR register is set to 00h (serial interface disabled). [3] (The TXD pin is released hereat.)
(4) When the received data is transferred to the U2RB register, the RI bit in the U2C1 register becomes 1 and the reception interrupt occurs.
(5) Data is read from the U2RB register in the reception interrupt handling.

Notes:
1. UART mode is set due to the countermeasure in “5.3 Operation With No Clock Delay”.
2. Until process (2-4) is done, do not input the transmit/receive clock to the CLK2 pin.
3. Until the serial interface is disabled, the TXD2 pin retains the last data.



fEXT: External clock frequency

The above diagram applies under the following conditions:
- The CKPOL bit in the U2C0 register is 0 (transmit data is output at the falling edge of transmit/receive clock and receive data is input at the rising edge).
- The CKPH bit in the U2SMR3 register is 1 (with clock delay).

Notes:
1. Set to tclk > ts. Do not input the transmit/receive clock to the CLK2 pin during tclk.
2. The TXD2 pin retains the last data during thold.
3. After the data reception completed interrupt handling and data transmission completed interrupt handling are done, control the master to drive the INT0 pin high.
4. Set to the port direction register corresponding to the TXD2 pin to constantly be in input mode.

Figure 5.2 Example of Slave Transmission/Reception Using Special Mode 2 With a Clock Delay

Table 5.3 Measured Values Using the Sample Code (1)

Item	Measured Value	Cycle
ts	Approximately 4.8 µs	Approximately 153 cycles
thold	Approximately 4.4 µs	Approximately 141 cycles
Time for data reception complete interrupt handling	Approximately 2.6 µs	Approximately 83 cycles

Note:
1. The conditions for measuring the values are the same as “3. Operation Confirmation Conditions”. The measured values and number of cycles are modified depending on the compiler option settings and interrupt generation timing.

5.5 Constants

Table 5.4 lists the Constants Used in the Sample Code.

Table 5.4 Constants Used in the Sample Code

Constant Name	Setting Value	Content
OVR_ERROR_MASK	1000h	Confirms an overrun error.
OVR_ERROR	1000h	Overrun error
HIGH	1	Determines a rising edge.
LOW	0	Determines a falling edge.
DUMMY_DATA	55h	Dummy data for transmission.
SUCCESS	00h	Success
ERROR	FFh	Error

5.6 Variables

Table 5.5 lists the Variables.

Table 5.5 Variables

Style	Variable Name	Content	Function Used
unsigned char	rcv_data	Stores received data.	uart2_receive()
unsigned char	u2_overrun	Stores an overrun error result.	main() _uart2_receive()

5.7 Function Tables

Declaration	void mcu_init(void)		
Outline	CPU clock setting		
Argument	Argument name		Meaning
	None		-
Variable (global)	Variable name		Contents
	None		-
Returned value	Type	Value	Meaning
	None	-	-
Function	Set the PLL clock as the CPU clock. Set the main clock as the CPU clock when using the M16C/63 Group.		

Declaration	void peripheral_init(void)		
Outline	Peripheral initial setting		
Argument	Argument name		Meaning
	None		-
Variable (global)	Variable name		Contents
	None		-
Returned value	Type	Value	Meaning
	None	-	-
Function	Perform initial setting of UART2. Set the NCH bit in the U2C0 register to 1 (pins TXD2/SDA2 and SCL2 are N-channel open drain output) when using the M16C/50 Series. Configure the $\overline{\text{INT0}}$ interrupt.		

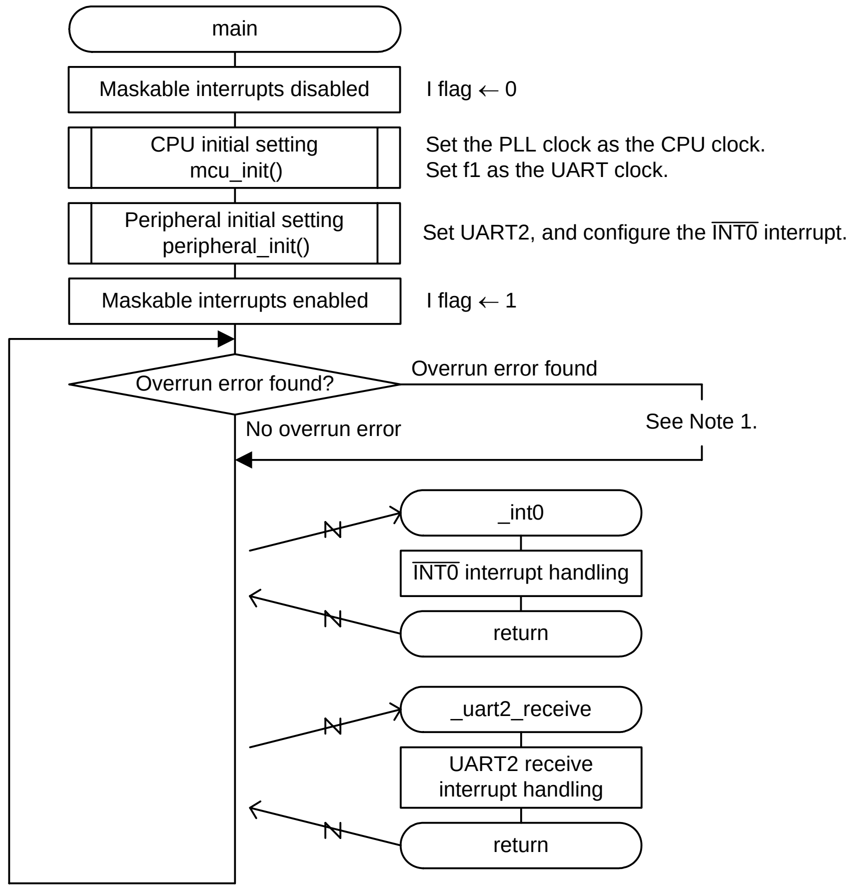
Declaration	void _int0(void)		
Outline	$\overline{\text{INT0}}$ interrupt handling		
Argument	Argument name		Meaning
	None		-
Variable (global)	Variable name		Contents
	None		-
Returned value	Type	Value	Meaning
	None	-	-
Function	At the beginning of the $\overline{\text{INT0}}$ interrupt handling, sample the input level three times. When a falling edge is input, start the UART2 transmission/reception. When a rising edge is input, disable the serial interface.		

Declaration	void _uart2_receive(void)		
Outline	UART2 receive interrupt handling		
Argument	Argument name		Meaning
	None		-
Variable (global)	Variable name		Contents
	rcv_data		Store received data.
	u2_overrun		Store overrun error result.
Returned value	Type	Value	Meaning
	None	-	-
Function	Check to see if an overrun error has been generated, and store the received data to the variables.		

5.8 Flowcharts

5.8.1 Main Function

Figure 5.3 shows the Main Function.

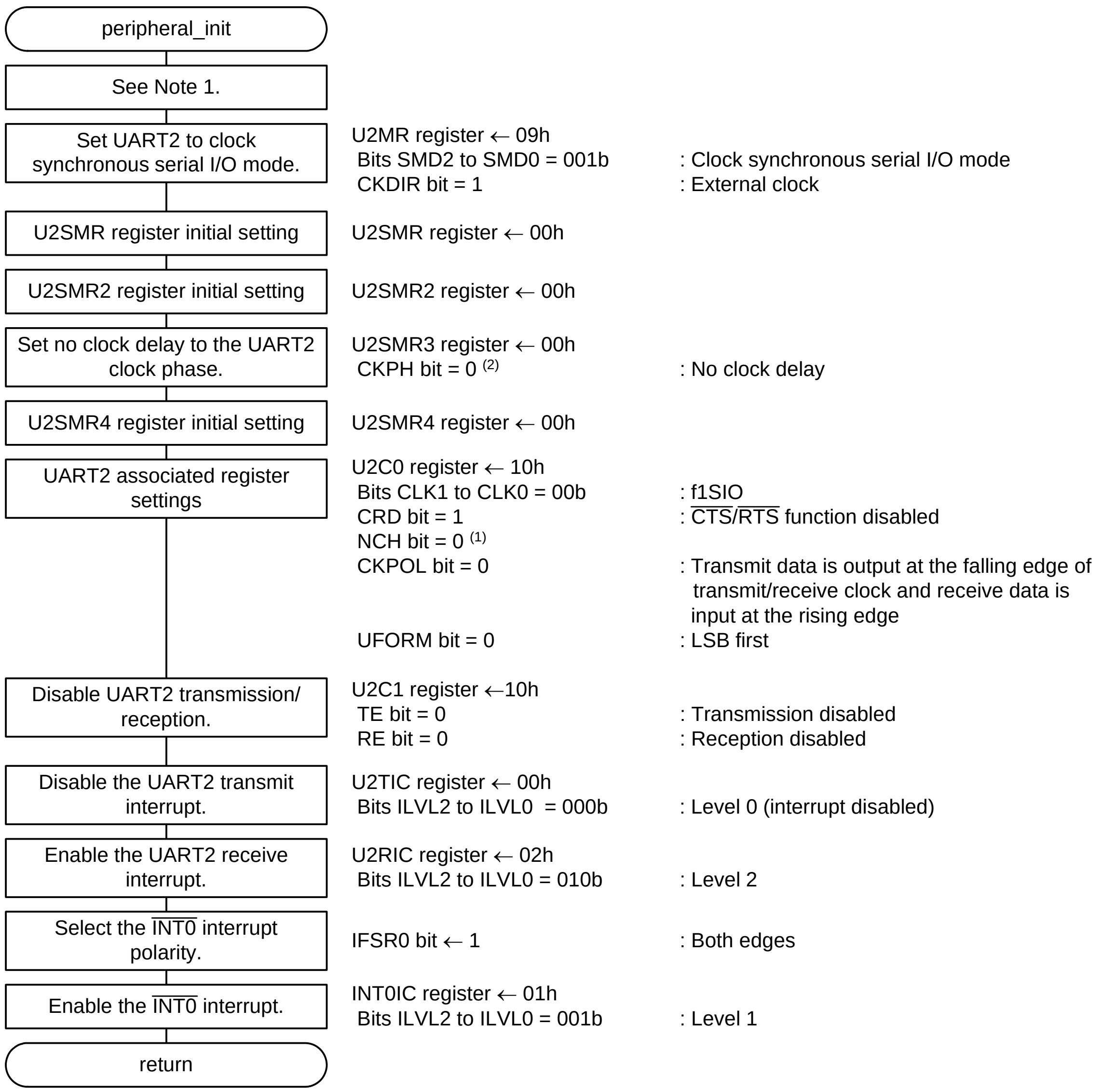


Note:
1. The sample code does not include any processing for when errors occur. Add processing is necessary.

Figure 5.3 Main Function

5.8.2 Peripheral Initial Setting

These settings set UART2 and configure the INT0 interrupt.
Figure 5.4 shows the Peripheral Initial Setting.



Notes:
1. Ports P7_0 and P7_1 in the M16C/50 Series are not N-channel open drain outputs.
   Set the NCH bit in the U2C0 register to 1 (pins TDX2/SDA2 and SCL2 are N-channel open drain output) when the M16C/50 Series is used.
2. Set the CKPH bit to 1 when using a clock delay.

Figure 5.4 Peripheral Initial Setting

5.8.3 $\overline{\text{INT0}}$ Interrupt Function

When a falling edge is input, UART2 transmission/reception enabled is set. When a rising edge is input, the serial interface is disabled.

Figure 5.5 shows the $\overline{\text{INT0}}$ Interrupt Function With No Clock Delay, and Figure 5.6 shows the $\overline{\text{INT0}}$ Interrupt Function With Clock Delay.

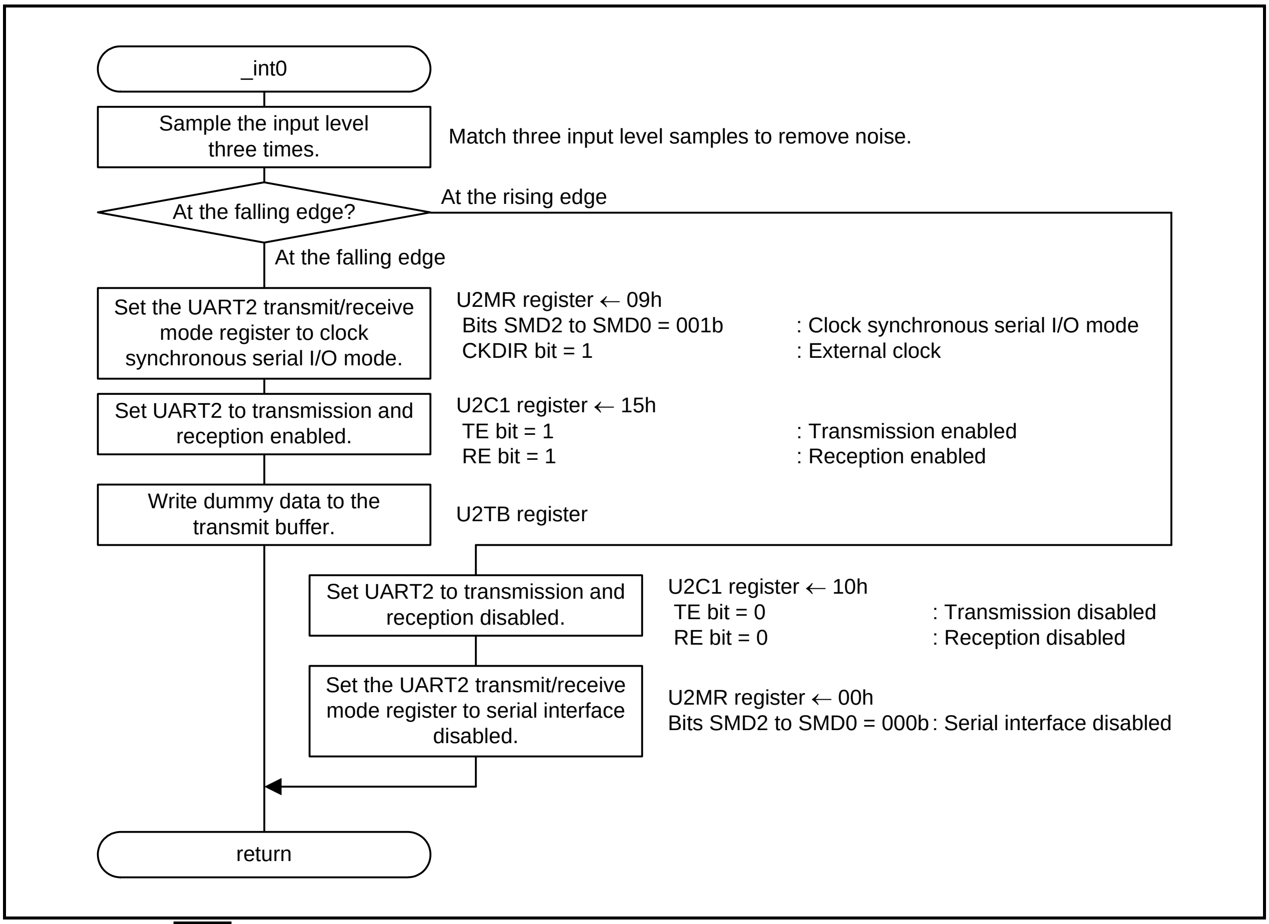
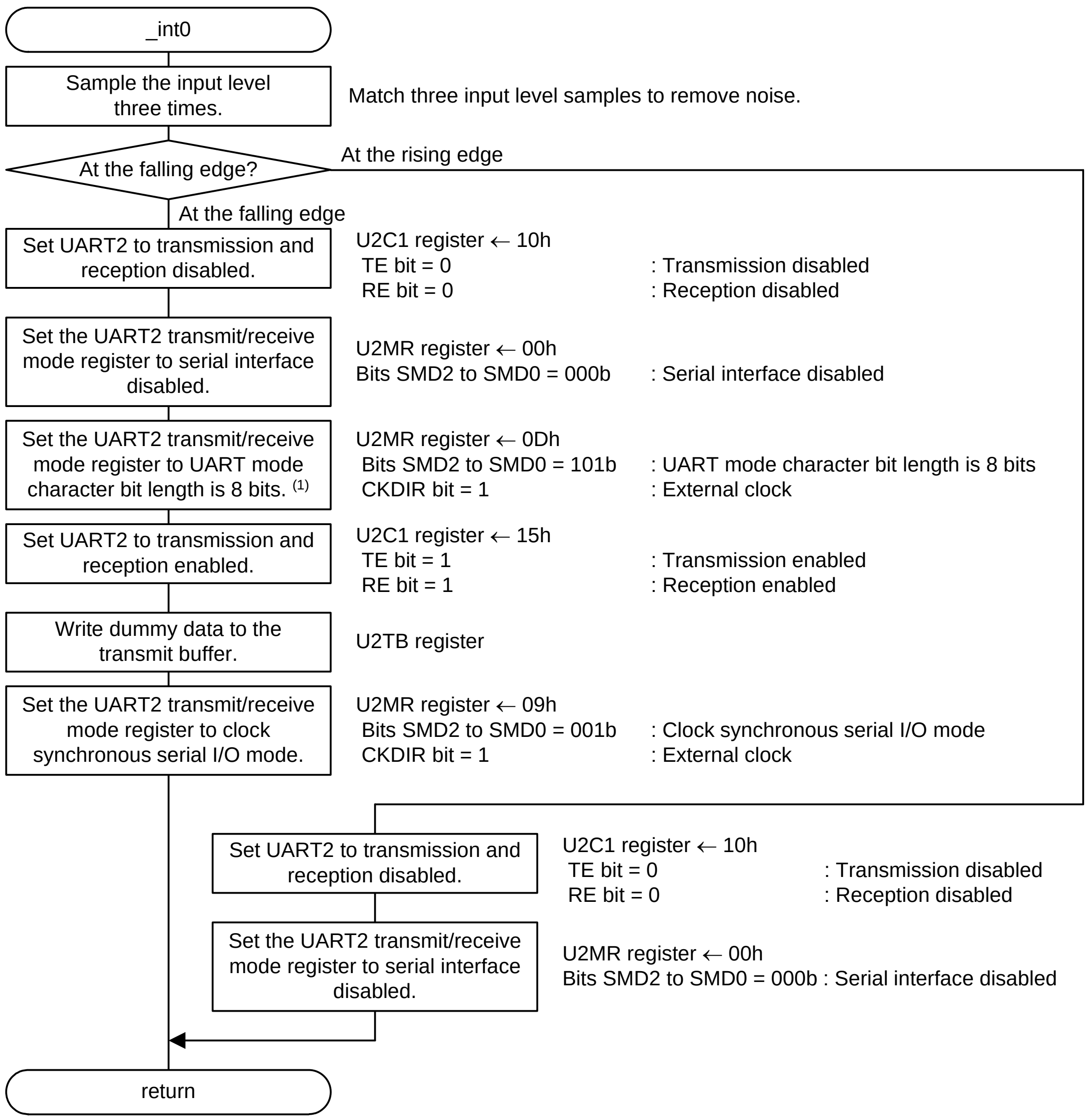


Figure 5.5 $\overline{\text{INT0}}$ Interrupt Function With No Clock Delay



Note:
1. Transmission and reception start conditions are not satisfied because the CLK2 pin becomes low when the CKPOL bit in the U2C0 register is 0, and the CKPH bit in the U2SMR3 register is 1. Therefore, the UART mode setting is added here.

Figure 5.6 INT0 Interrupt Function With Clock Delay

5.8.4 UART2 Reception Interrupt Function

This function checks whether an overrun error has occurred or not, and stores the received data to the variable. Figure 5.7 shows the UART2 Reception Interrupt Function.

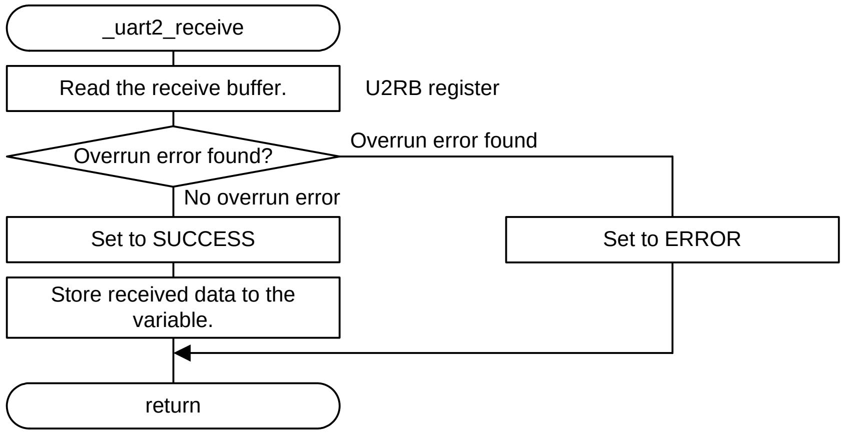


Figure 5.7 UART2 Reception Interrupt Function

6. Sample Program

A sample program can be downloaded from the Renesas Electronics website.

7. Reference Documents

M16C/65 User's Manual: Hardware Rev.1.10
The latest version can be downloaded from the Renesas Electronics website.

Technical Update/Technical News
The latest information can be downloaded from the Renesas Electronics website.

Website and Support

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http://www.renesas.com/

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Revision History	M16C/63, 64A, 65, 65C, 6C, 5LD, 5L, and 5M Groups Serial Interface Special Mode 2

Rev.	Date	Description	
		Page	Summary
1.00	Dec. 28, 2010	—	First edition issued

General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this manual, refer to the relevant sections of the manual. If the descriptions under General Precautions in the Handling of MPU/MCU Products and in the body of the manual differ from each other, the description in the body of the manual takes precedence.

1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.
2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.
3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.
4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.
5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different part numbers may differ because of the differences in internal memory capacity and layout pattern. When changing to products of different part numbers, implement a system-evaluation test for each of the products.

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