RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five, RZ/A3UL, RZ/G3S, RZ/A3M Lifetime Guideline

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Information

This guide helps PCB design engineers to estimate product lifetimes for the target devices based on the criteria used in the qualification process. The product lifetimes described here are estimates and do not represent a guaranteed lifetime for a product. The target devices consist of several processors that deliver a wide range of processing and multimedia capabilities across various qualification levels. This document is intended to provide users with guidance on how to interpret the different target devices qualification levels in terms of the target operating frequency of the device, the maximum supported junction temperature(Tj) of the processor, and how it relates to the lifetime of the device.

Target Device

- RZ/G2L PBGA 15.0/21.0sq
- RZ/G2LC PBGA 13.0sq
- RZ/V2L PBGA 13.0sq
- RZ/G2UL PBGA 15.0/21.0sq
- RZ/Five PBGA 13.0/11.0sq
- RZ/A3UL PBGA 13.0sq
- RZ/G3S PBGA 14.0sq
- RZ/A3M PBGA 17.0sq

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1. Device Qualification Level and available Power-on Hours

Device qualification level defines a number of Power-on Hours (PoH) available to the target devices under a given set of the conditions. For example,

- Operating voltage of the target device
- The maximum operating frequency
  - The Tj of the target device depends on its operating frequency. Therefore, users must ensure that their device is appropriately thermally managed such that the maximum Tj is not exceeded.

NOTE

All data provided within this document are estimates for PoH that are based on extensive qualification experience and testing with the target devices. These statistically derived estimates should not be viewed as a limit on an individual device lifetime, nor should they be construed as a guarantee by Renesas as to the actual lifetime of the device. Sales and warranty terms and conditions still apply.

Figure 1.1 shows the estimates of the PoH as a function of Tj. PoH can be read directly from the curves below to determine the necessary trade-offs to Tj at the maximum operating frequency of the device.

Table 1.1 provides the number of PoH at the maximum Tj.

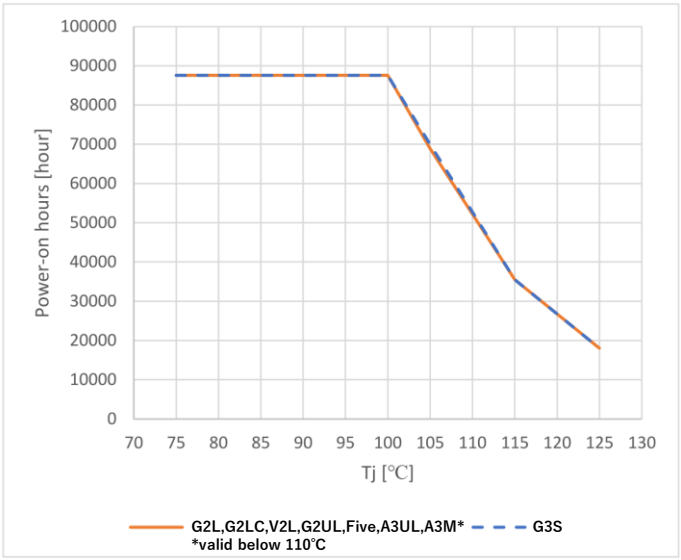

Figure 1.1 Lifetime Estimation vs Tj

Table 1.1 Lifetime Estimation at the maximum Tj

Target Device	PoH [Hrs]	SOC operating voltage [V]	Tj [°C]
RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five, RZ/A3UL	18042	1.1	125
RZ/G3S	18042	0.9	125
RZ/A3M	18042	1.1	110

2. Conclusion

Selecting the optimal operating performance point and thermal envelope is paramount to meet the application lifetime targets. The operating Tj of the processor can greatly improve the lifetime of the device. Lowering the operating Tj in the application is the most effective means to increase the lifetime of the device without affecting the performance of the device. This can be accomplished by increasing the thermal dissipation capacity in the application. In cases where the thermal properties cannot be altered, a lower operating voltage can be used to increase the lifetime of the device. Lowering the voltage may result in lowered performance; the operating frequency may have to be adjusted lower to match the voltage as specified in the datasheet. The data and examples provided in this application note help users determine the estimated lifetime for their particular application.

REVISION HISTORY	RZ/G2L, RZ/G2LC, RZ/G2UL, RZ/V2L, RZ/Five, RZ/A3UL, RZ/G3S, RZ/A3M Lifetime Guideline

Rev.	Date	Description	
		Page	Summary
1.00	Oct. 05, 2021	—	First edition issued
1.01	Dec. 01, 2021	All	RZ/G2UL is added.
1.02	June 20, 2022	All	RZ/Five is added.
1.03	June 24, 2022	All	RZ/A3UL is added.
1.04	Nov. 20, 2023	All	RZ/G3S is added.
1.05	Apr. 10, 2025	All	RZ/A3M is added.

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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