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April 1st, 2010
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SH7080 Group

I²C2 Single-Master Transmission (Writing to I²C-Bus EEPROM)

Introduction

This application note describes the transmitting operation by the I²C bus interface 2 module (I²C2) in single-master mode. Please use this application note as a guide in designing user programs.

Although the programs given in this application note have been verified for correct operation, we strongly recommend that the user confirm correct operation before applying the programs in the actual application.

Target Device

SH7085

Contents

1. Specifications

- The SH7085's I²C bus interface 2 module (I²C2) is used to write 10 bytes of data to a two-wire serial EEPROM (HN58X2416; 16k bits; 2k words × 8 bits).
- The connection is made in single-master configuration, in which the SH7085 is the master device.
- The device code of the connected EEPROM is B'1010.
- Data is written to addresses H'0000 to H'0009 in the EEPROM.
- While the acknowledge bit (ACK) from the EEPROM is 0, data are transmitted continuously (data transmission is halted when ACK = 1 is received).
- The frequency of the I²C bus data transfer clock is 400 kHz.

Figure 1 shows an example of connection between the SH7085 and EEPROM, and table 1 shows the SH7085's I²C2 settings. Table 2 shows the device address word of the EEPROM used in the sample task.

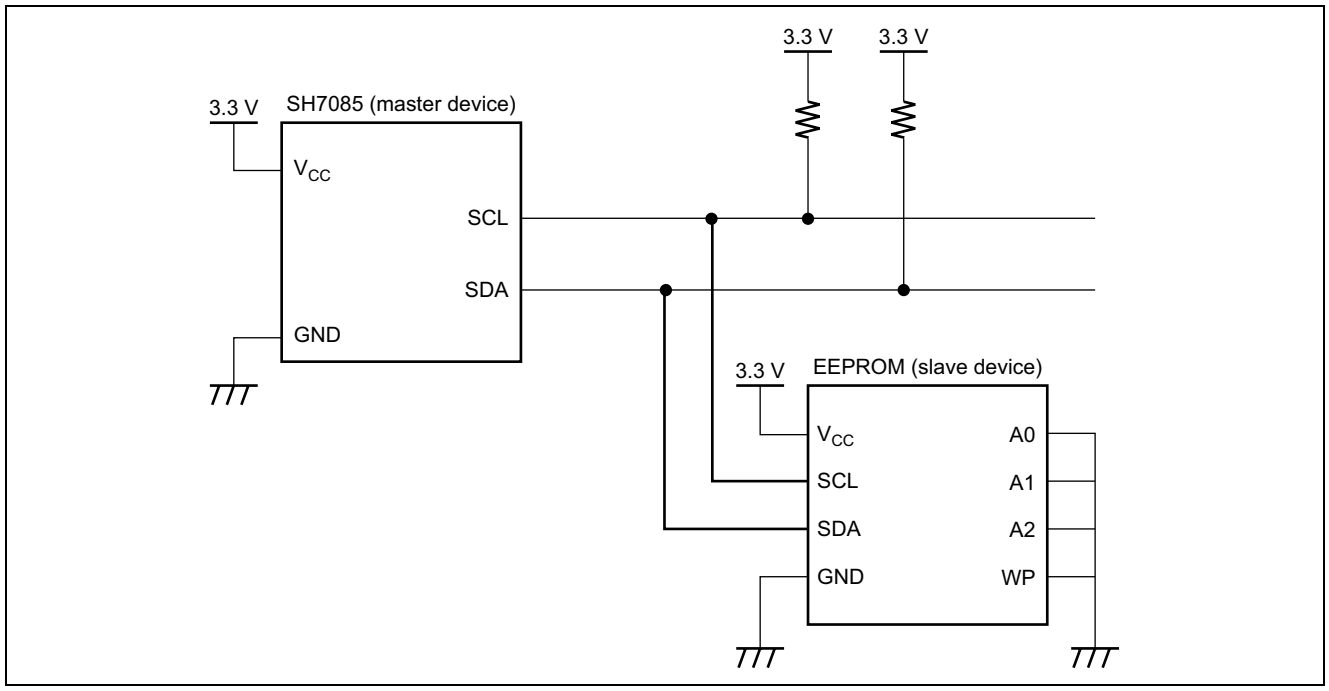


Figure 1 Example of Connection between SH7085 and EEPROM

Table 1 I²C2 Settings of SH7085

Item	Setting
Operating mode	Master transmission mode
Transfer clock	400 kHz (Pϕ = 40 MHz)
Data bit length	9 bits (including the ACK bit)
Wait cycles inserted between data and ACK	None
Interrupt	None
ACK determination	Data transmission is halted when ACK = 1 is received.

Table 2 Device Address Word of EEPROM

Device Code				Device Address Code			R/W Code
1	0	1	0	a10	a9	a8	R = 1, W = 0

Note: a10 to a8 are the upper 3 bits of the EEPROM address.

2. Conditions for Application

Operating frequency:	Internal clock:	80 MHz
	Bus clock:	40 MHz
	Peripheral clock:	40 MHz
	MTU2 clock:	40 MHz
	MTU2S clock:	80 MHz
C compiler:	Version 7.1.04 from Renesas Technology Corp.	

3. Summary of MCU Functions Used

In this sample task, data are written to the EEPROM via the I²C bus (Inter IC bus).

3.1 I²C Bus Interface 2 (I²C2)

The I²C bus interface 2 (I²C2) conforms to the I²C bus interface specifications set up by Philips, and provides a subset of the I²C functions. Figure 2 shows a block diagram of the I²C2 module.

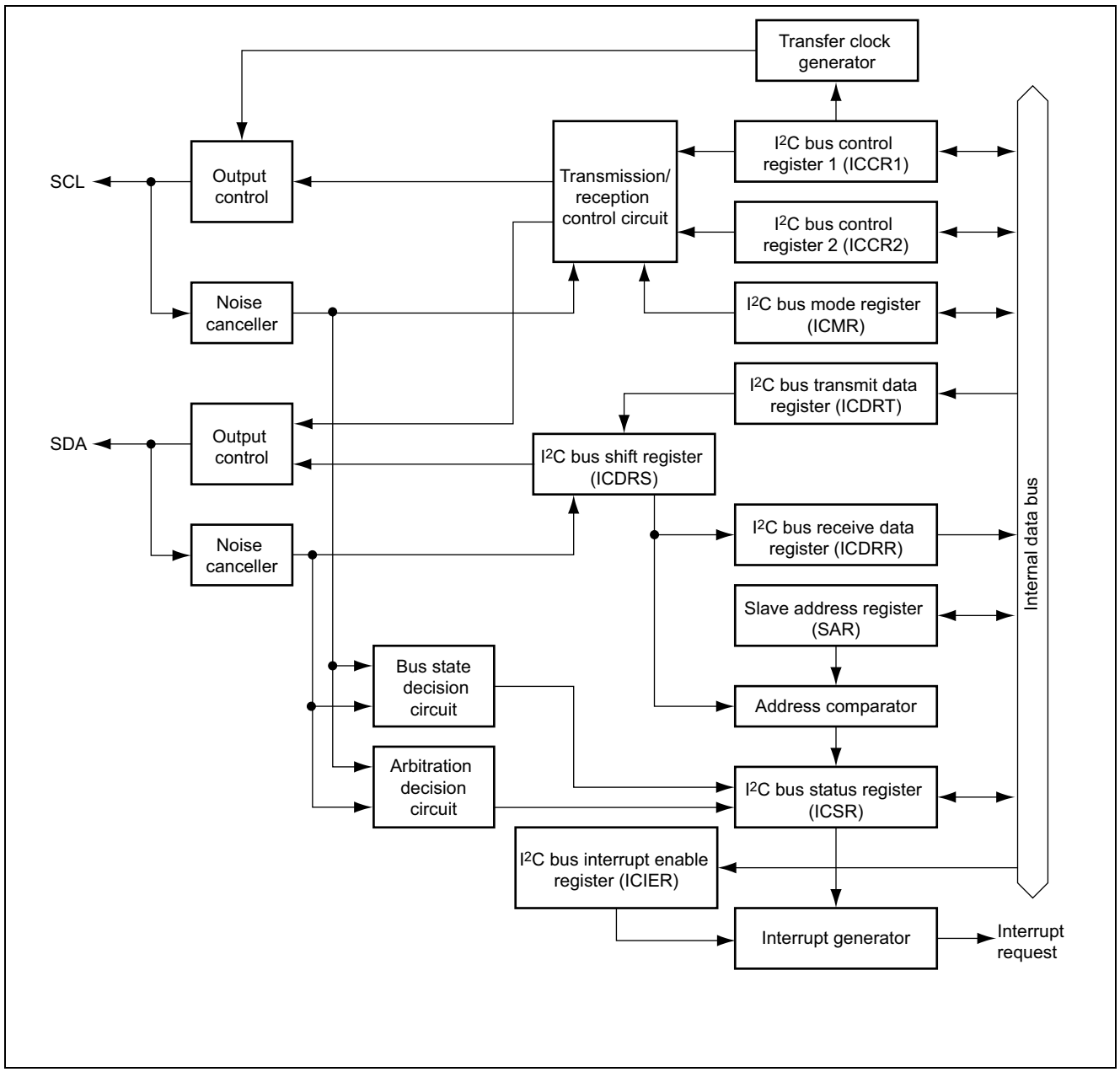


Figure 2 Block Diagram of I²C2 Module

- The I²C bus control register 1 (ICCR1) sets I²C2 operations.
- The I²C bus control register 2 (ICCR2) generates start and stop conditions, drives the SDA pin, monitors the SCL pin, and controls resetting of the I2C bus control circuitry.
- The I²C bus mode register (ICMR) selects MSB- or LSB-first transfer, controls the wait states in master mode, and selects the number of bits to be transferred.
- The I²C bus interrupt enable register (ICIER) enables interrupts, selects the use of the acknowledge bit, sets the acknowledge bit for transmission, and checks the received acknowledge bit.
- The I²C bus status register (ICSR) consists of various interrupt request and status flags.
- The I²C slave address register (SAR) selects a format and sets the slave address.
- The I²C bus transmit data register (ICDRT) holds data for transmission.
- The I²C bus receive data register (ICDRR) holds the received data.
- The I²C bus shift register (ICDRS) is used to transmit/receive data; this register cannot be accessed by the CPU.

4. Operation

In this sample task, data are written to the EEPROM.

Figure 3 shows the contents of communication when data are written to the EEPROM.

After a start condition is generated, the device address word is transmitted with the R/W code set to 0 (meaning write operation); the lower byte of the write start address of the EEPROM is transmitted next, followed by data to be written in sequence.

While the acknowledge (ACK) from the EEPROM is 0, the next data is transmitted continuously. Finally, a stop condition is generated.

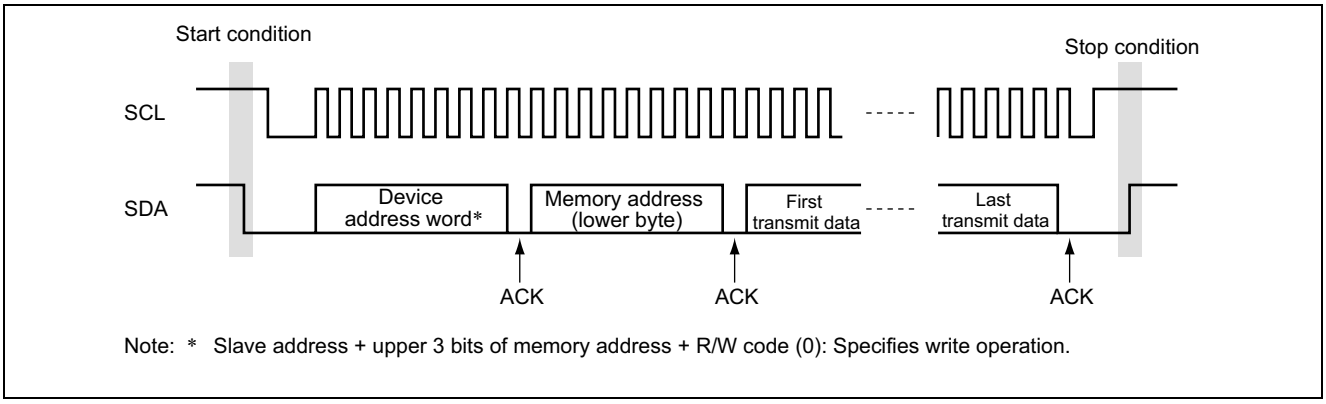
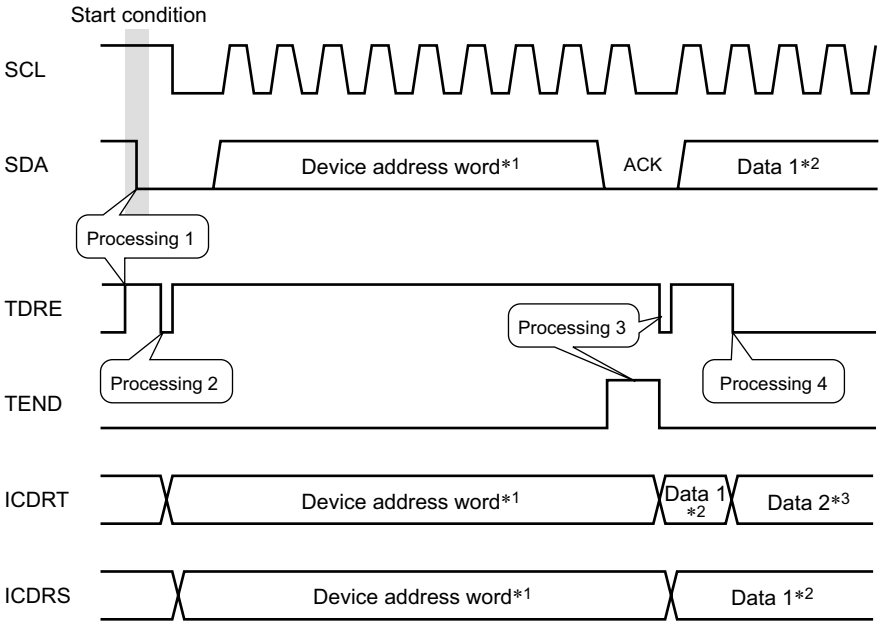


Figure 3 Contents of Communication When Data are Written to EEPROM

Figure 4 shows the operation when writing to EEPROM is started, and figure 5 shows the ending operation. The software and hardware processing in figures 4 and 5 are described in tables 3 and 4, respectively.



Notes: 1. Slave address + upper 3 bits of memory address + R/W code (0): Specifies write operation.
2. Lower byte of the EEPROM write start address
3. First byte of the data for writing

Figure 4 Operation when EEPROM Writing Starts

Table 3 Software and Hardware Processing when EEPROM Writing Starts

	Software Processing	Hardware Processing
Processing 1	Set BBSY to 1 and SCP to 0 in the ICCR2 register.	• Generate a start condition. • Set the TDRE bit in the ICSR register to 1.
Processing 2	Write the device address word data to the ICDRT register.	• Clear the TDRE bit in the ICSR register to 0. • Transfer the transmit data in the ICDRT register to the ICDRS register, and output the data from the SDA pin. • Set the TDRE bit in the ICSR register to 1.
Processing 3	• Confirm that TEND in the ICSR register is 1. • Check the received acknowledge bit through the ACKBR bit in the ICIER register. • Write the lower byte of the write start address of the EEPROM to the ICDRT register.	• Set the TEND bit in the ICSR register to 1 after the last bit of the transmit data is output. • Clear the TDRE and TEND bits in the ICSR register to 0 after writing to the ICDRT register has ended. • Transfer the transmit data in the ICDRT register to the ICDRS register, and output the data from the SDA pin. • Set the TDRE bit in the ICSR register to 1 after the transmit data in the ICDRT register has been transferred to the ICDRS register.
Processing 4	• Confirm that TDRE in the ICSR register is 1. • Write the first byte of the transmit data to the ICDRT register.	Clear the TDRE bit in the ICSR register to 0 after writing to the ICDRT register has ended.

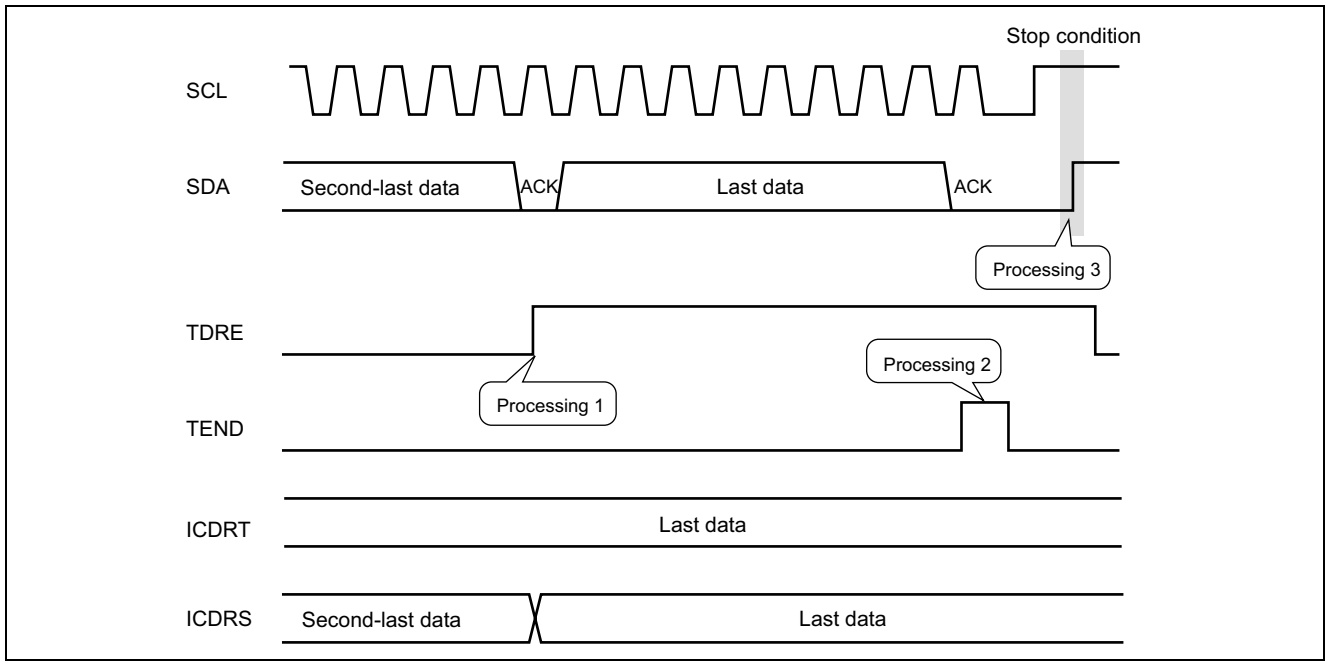


Figure 5 Operation when EEPROM Writing Ends

Table 4 Software and Hardware Processing when EEPROM Writing Ends

	Software Processing	Hardware Processing
Processing 1	—	• Transfer the transmit data in the ICDRT register to the ICDRS register, and output the data from the SDA pin. • Set the TDRE bit in the ICSR register to 1.
Processing 2	• Confirm that TEND in the ICSR register is 1. • Clear the TEND bit in the ICSR register to 0. • Clear the STOP bit in the ICSR register to 0.	—
Processing 3	• Clear BBSY and SCP in the ICCR2 register to 0. • Confirm that STOP in the ICSR register is 1. • Clear MST and TRS in the ICCR1 register to 0 (slave reception mode). • Clear the TDRE bit in the ICSR register to 0.	• Generate a stop condition. • Set the STOP bit in the ICSR register to 1.

5. Description of Software

5.1 Modules

Table 5 describes the modules used in the sample application.

Table 5 Description of Modules

Module Name	Label Name	Description
Main function	main()	Sets the write start address of the EEPROM and data for writing, and calls the data write function.
I²C2 initialization function	init_iic()	Cancels module standby mode, and configures the PFC and I²C2.
Data write function	write_EEPROM()	Generates a start condition, writes data to the EEPROM, and generates a stop condition.
EEPROM address transmission function	set_addr_EEPROM()	Generates a start condition and a slave address, and sets the EEPROM address.

5.2 Variables

Table 6 lists the variables used in the sample application.

Table 6 Description of Variables

Label Name of Variable	Function	Used In
write_data[0:9]	Array for storing write data	Main function
address	Write start address of the EEPROM	Main function
addr	Copy of write start address of the EEPROM	Data write function EEPROM address transmission function
*w_data	Pointer variable to the array for storing write data	Data write function
num	Number of transmit data bytes	Data write function
ack	Acknowledge determination flag	Data write function

5.3 Register Settings

The register settings used in the sample application are described below. Note that the set values are specifically used in the sample task and that they are different from the initial values.

5.3.1 Settings for the Clock Pulse Generator (CPG)

- Frequency Control Register (FRQCR)
  - Setting value: H'0241
  - Function: Specifies the frequency division ratios.

Bit	Bit Name	Value	Description
15	—	0	Reserved
14 to 12	IFC[2] to IFC[0]	000	Frequency division ratio for internal clock (Iϕ) 000: ×1 (80 MHz when input clock is 10 MHz)
11 to 9	BFC[2] to BFC[0]	001	Frequency division ratio for bus clock (Bϕ) 001: ×1/2 (40 MHz when input clock is 10 MHz)
8 to 6	PFC[2] to PFC[0]	001	Frequency division ratio for peripheral clock (Pϕ) 001: ×1/2 (40 MHz when input clock is 10 MHz)
5 to 3	MIFC[2] to MIFC[0]	000	Frequency division ratio for MTU2S clock (MIϕ) 000: ×1 (80 MHz when input clock is 10 MHz)
2 to 0	MPFC[2] to MPFC[0]	001	Frequency division ratio for MTU2 clock (MPϕ) 001: ×1/2 (40 MHz when input clock is 10 MHz)

5.3.2 Settings for Power-Down Modes

- Standby Control Register 3 (STBCR3)
  - Setting value: H'7F
  - Function: Controls the operation of individual modules in power-down modes.

Bit	Bit Name	Value	Description
7	MSTP15	0	0: The I²C2 runs.
6	MSTP14	1	1: Stops supply of the clock signal to the SCIF.
5	MSTP13	1	1: Stops supply of the clock signal to SCI_2.
4	MSTP12	1	1: Stops supply of the clock signal to SCI_1.
3	MSTP11	1	1: Stops supply of the clock signal to SCI_0.
2	MSTP10	1	1: Stops supply of the clock signal to the SSU.
1 and 0	—	11	Reserved

5.3.3 Settings for I²C Bus Interface 2 (I²C2)

- I²C Bus Control Register 1 (ICCR1)
  - Setting value: H'B5
  - Function: Selects the operating mode and transfer clock of the I²C2.

Bit	Bit Name	Value	Description
7	ICE	1	1: Enables transfer operation (the SCL/SDA buses are driven).
6	RCVD	0	0: Performs the next reception when ICDRR is read.
5	MST	1	MST: Master/Slave Select
4	TRS	1	TRS: Transmit/Receive Select 11: Master transmission mode.
3 to 0	CKS[3] to CKS[0]	0101	Transfer Clock Select 0101: Sets the transfer rate to 400 kHz (Pϕ = 40 MHz).

- I²C Bus Control Register 2 (ICCR2)
  - Setting value: H'7D
  - Function: Generates start and stop conditions, drives the SDA pin, monitors the SCL pin, and controls resetting of the I²C bus control circuitry.

Bit	Bit Name	Value	Description
7	BBSY	0*	Indicates whether the I²C bus is occupied or released, and generates start and stop conditions. 0: I²C bus is released.
6	SCP	1*	Controls generation of start and stop conditions.
5	SDAO	1	1: The output on the SDA pin is high (when read). Changes the output on the SDA pin to Hi-Z (when written).
4	SDAOP	1	SDAO Write Protect Write 0 to this bit when writing to SDAO.
3	SCLO	1	1: The output on the SCL pin is high (read-only bit).
2	—	1	Reserved
1	IICRST	0	I²C Control Unit Reset Resets the control circuitry of the I²C when 1 is written.
0	—	1	Reserved

Note: * To generate a start condition, write b'10 to BBSY and SCP.
To generate a stop condition, write b'00 to BBSY and SCP.

- I²C Bus Mode Register (ICMR)
  - Setting value: H'38
  - Function: Selects MSB- or LSB-first transfer, controls the wait states in master mode, and selects the number of bits to be transferred.

Bit	Bit Name	Value	Description
7	MLS	0*[1]	0: MSB-first
6	WAIT	0*[2]	0: Data and acknowledge bit are transferred continuously.
5 and 4	—	11	Reserved
3	BCWP	1	BC Write Protect Write 0 to this bit when writing to the BC[2] to BC[0] bits.
2 to 0	BC[2] to BC[0]	000	000: 9 bits (data and acknowledge bit) are transferred.

Notes: 1. This bit must be set to 0 (MSB-first) when the I²C bus format is used.
2. This bit must be set to 0.

- I²C Bus Interrupt Enable Register (ICIER)
  - Setting value: H'04
  - Function: Enables or disables interrupt sources and controls the acknowledge bit.

Bit	Bit Name	Value	Description
7	TIE	0	0: Disables the transmit data empty interrupt request (IITXI).
6	TEIE	0	0: Disables the transmit end interrupt request (IITEI).
5	RIE	0	0: Disables the receive data full interrupt request (IIRXI).
4	NAKIE	0	0: Disables the NACK receive interrupt request (IINAKI).
3	STIE	0	0: Disables the stop condition detection interrupt request (IISTPI).
2	ACKE	1	1: Halts data transfer when the received acknowledge bit is 1.
1	ACKBR	0	Holds the acknowledge data in transmission mode (read-only bit).
0	ACKBT	0	0: Transmits ACK = 0 in reception mode.

- I²C Bus Status Register (ICSR)
  - Setting value: H'00
  - Function: Provides various interrupt request and status flags.

Bit	Bit Name	Value	Description
7	TDRE	0	Transmit data register empty flag
6	TEND	0	Transmit end flag
5	RDRF	0	Receive data register full flag
4	NACKF	0	No acknowledge detection flag
3	STOP	0	Stop condition detection flag
2	AL/OVE	0	Arbitration lost flag/overrun error flag
1	AAS	0	Slave address recognition flag
0	ADZ	0	General call address recognition flag

- I²C Bus Transmit Data Register (ICDRT)
  - Setting value: H'FF (initial value)
  - Function: Holds data for transmission.
- I²C Bus Receive Data Register (ICDRR)
  - Setting value: H'FF
  - Function: Holds the received data. (Read only)

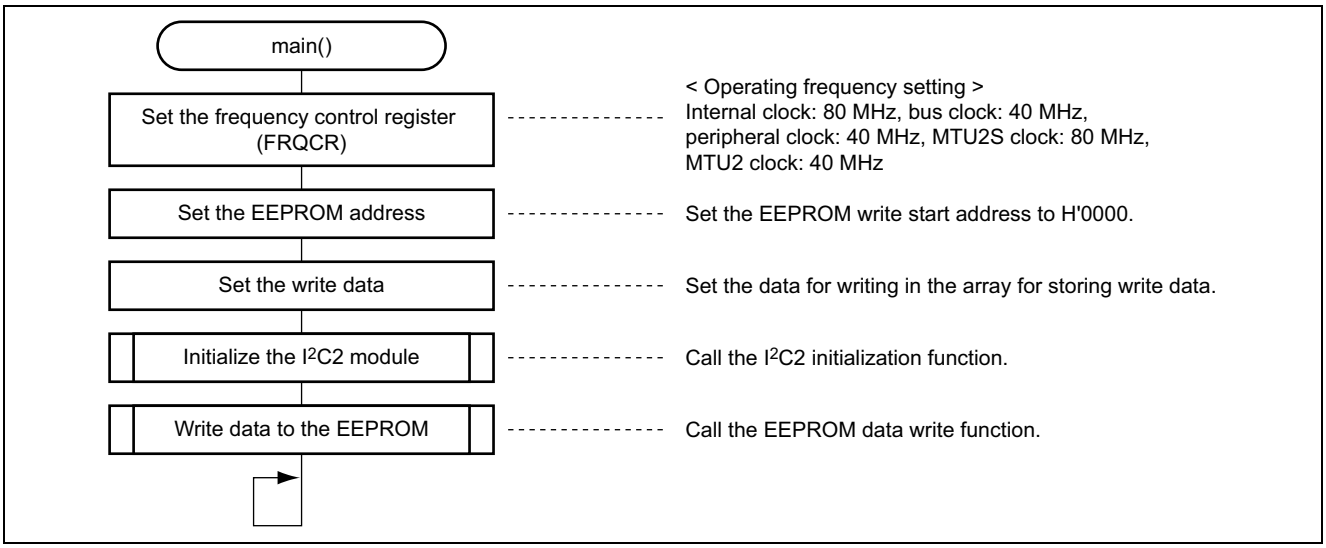
5.3.4 Settings for the Pin Function Controller (PFC)

- Port B Control Register L1 (PBCRL1)
  - Setting value: H'4400
  - Function: Selects the functions of the multiplexed pins on port B (PB3 to PB0).

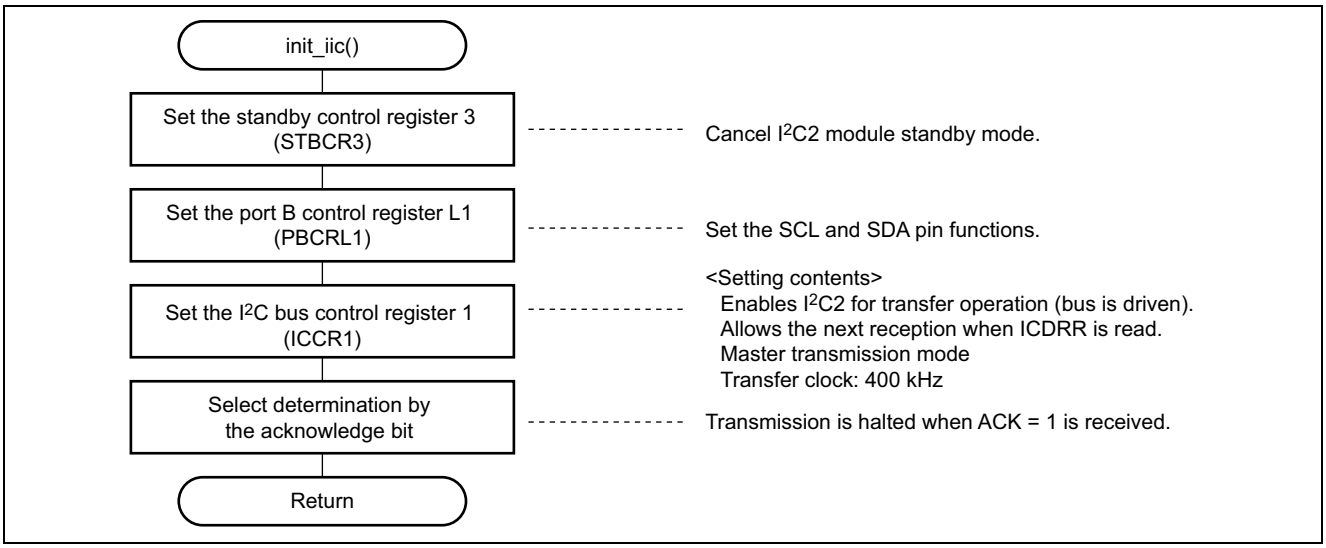
Bit	Bit Name	Value	Description
15	—	0	Reserved
14 to 12	PB3MD[2] to PB3MD[0]	100	PB3 mode 100: SDA I/O (I²C2)
11	—	0	Reserved
10 to 8	PB2MD[2] to PB2MD[0]	100	PB2 mode 100: SCL I/O (I²C2)
7	—	0	Reserved
6 to 4	PB1MD[2] to PB1MD[0]	000	PB1 mode 000: PB1 I/O (port)
3	—	0	Reserved
2 to 0	PB0MD[2] to PB0MD[0]	000	PB0 mode 000: PB1 I/O (port)

6. Flowcharts

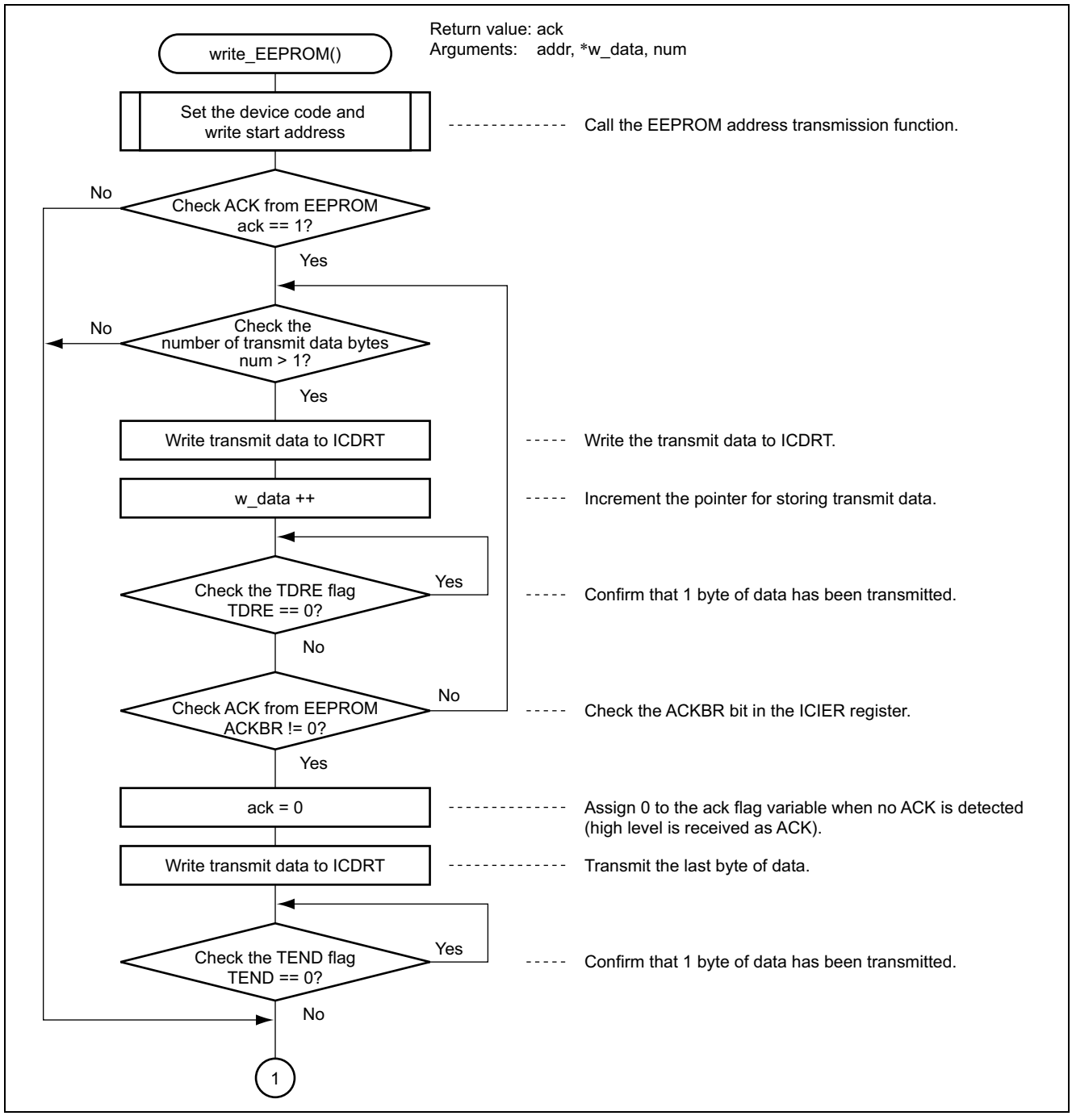
6.1 Main Function

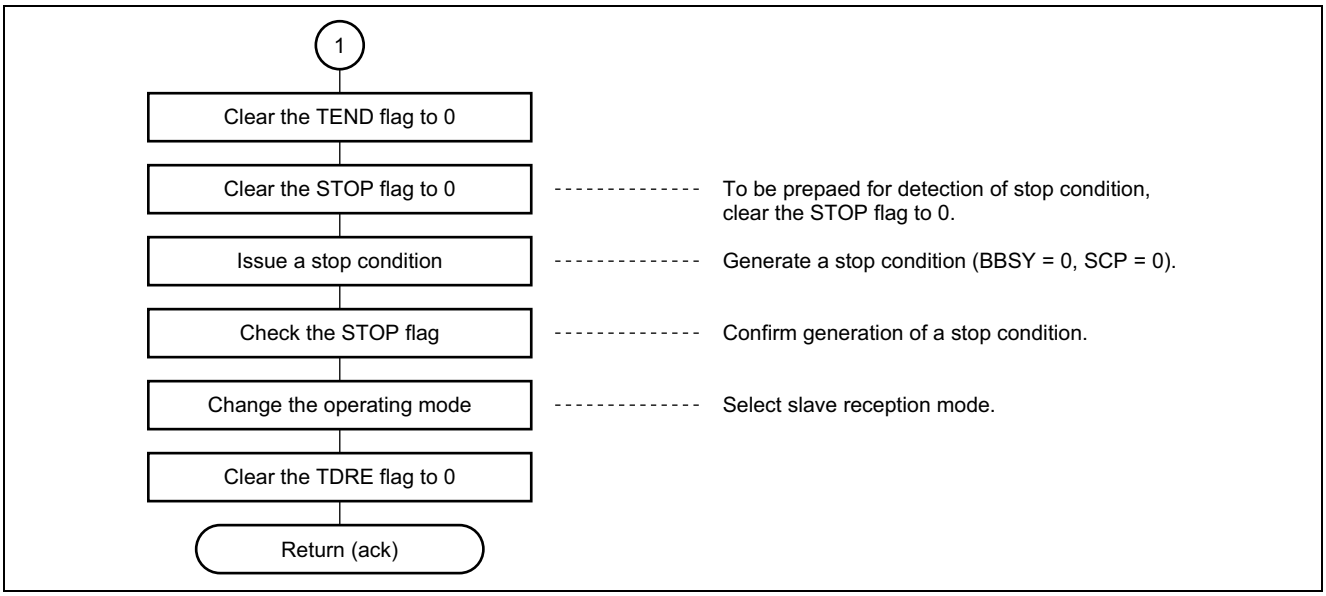


6.2 I²C2 Initialization Function

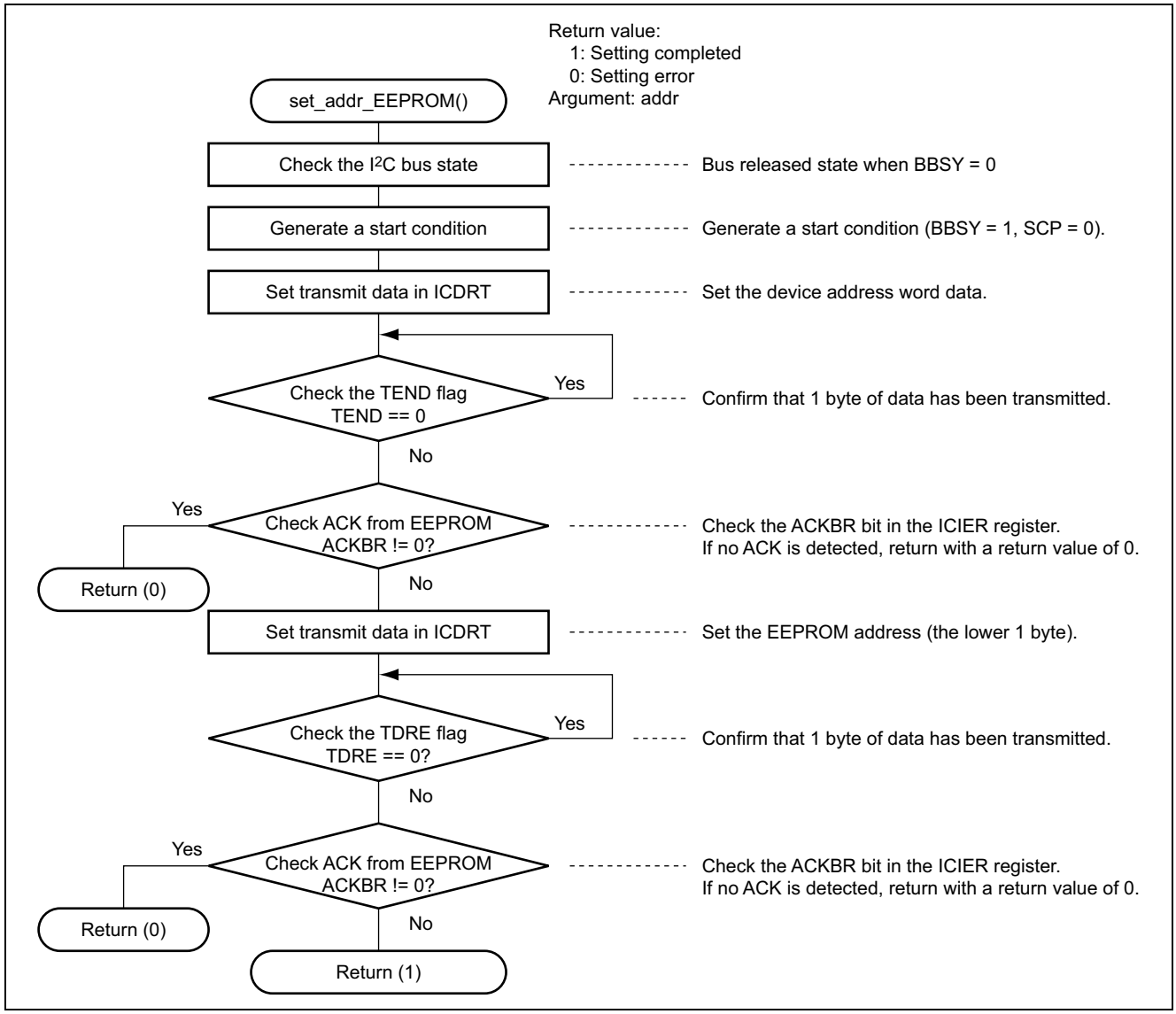


6.3 Data Write Function




1
Clear the TEND flag to 0
Clear the STOP flag to 0
To be prepaed for detection of stop condition, clear the STOP flag to 0.
Issue a stop condition
Generate a stop condition (BBSY = 0, SCP = 0).
Check the STOP flag
Confirm generation of a stop condition.
Change the operating mode
Select slave reception mode.
Clear the TDRE flag to 0
Return (ack)

6.3.1 EEPROM Address Transmission Function



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Rev.	Date	Description	
		Page	Summary
1.00	Sep.14.05	—	First edition issued

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