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H8/38076R

LED Flashing Operation Using Interval Function of Watchdog Timer

Introduction

The interval function of the watchdog timer is used to flash an LED on and off.

Target Device

H8/38076R

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1. Specifications

- The interval timer mode of the watchdog timer is used to flash an LED on and off.
- The system clock is used as the clock source of the watchdog timer.
- An internal interrupt is generated when timer counter WD (TCWD) of the watchdog timer overflows.
- The LED connected to the P93 output pin of port 9 flashes each time an internal interrupt is generated.
- A sample connection diagram is shown in figure 1.

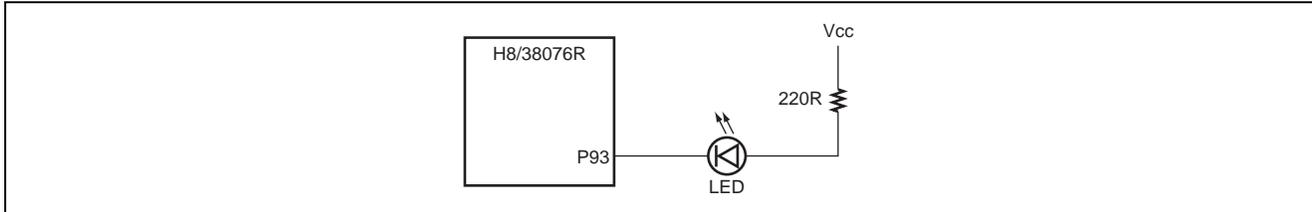


Figure 1 LED Flashing Operation Using Interval Function of Watchdog Timer

2. Description of Functions

2.1 Functions Used

In this sample task the watchdog timer operates as an interval timer. A block diagram of the watchdog timer is shown in figure 2. The watchdog timer function is described below.

1. Watchdog Timer Function

This LSI incorporates the watchdog timer (WDT). The WDT is an 8-bit timer that can generate an internal reset if a system becomes uncontrolled and prevents the CPU from writing to the timer counter, allowing it to overflow. When this watchdog timer function is not needed, the WDT can be used as an interval timer. In interval timer operation, an interval timer interrupt is generated each time the counter overflows.

- **Timer control/status register WD1 (TCSRWD1)**
TCSRWD1 performs TCSRWD1 and TCWD write control. TCSRWD1 also controls the watchdog timer operation and indicates the operating state. TCSRWD1 must be rewritten by using the MOV instruction. Bit manipulation instructions cannot be used to change its setting values. In this sample task TCSRWD1 controls the enabling/disabling of write operations to various registers, depending on conditions, and controls the start of count-up operation by the counter.
- **Timer control/status register WD2 (TCSRWD2)**
TCSRWD2 performs TCSRWD2 write control, mode switching, and interrupt control. TCSRWD2 must be rewritten by using the MOV instruction. Bit manipulation instructions cannot be used to change its setting values. In this sample task the watchdog timer operates as an interval timer, and overflow interrupts are enabled.
- **Timer counter WD (TCWD)**
Timer counter WD is an 8-bit readable/writable up-counter. When TCWD overflows from H'FF to H'00, OVF in TCSRWD2 is set to 1. The initial value of TCWD is H'00. In this sample task it is set to H'12.
- **Timer mode register WD (TMWD)**
TMWD selects the input clock. In this sample task the system clock is selected as the input clock and $\phi/8,192$ is used as the division setting.

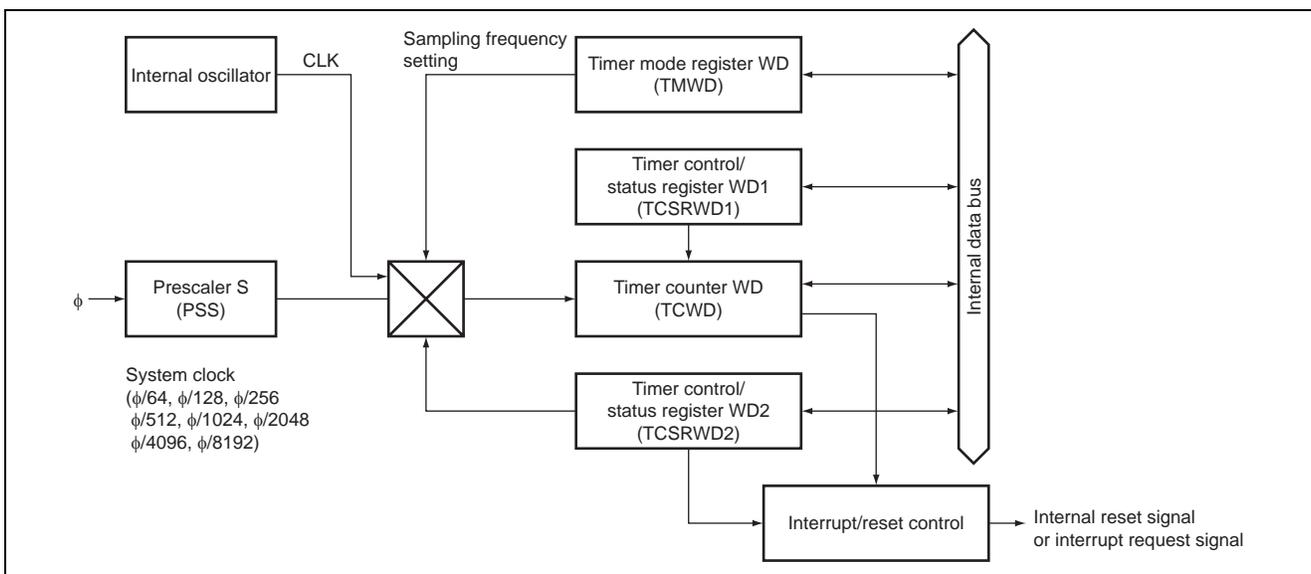


Figure 2 Block Diagram of Watchdog Timer

2. Interval Timer Operation

This section describes operation in the interval timer mode. To use the watchdog timer as an interval timer, set the WT/IT bit in TCSRWD2 to 1. (Two write accesses are required to write to the WT/IT bit.) If 0 is written to the B2WI bit and 1 to the WDON bit simultaneously when the TCSRWE bit in TCSRWD1 is set to 1, TCWD starts counting up. (Two write accesses to TCSRWD1 are required to operate the watchdog timer.)

When the watchdog timer is operating as an interval timer, an interval timer interrupt request is generated each time TCNT overflows. In this way it is possible to generate an interval timer interrupt at fixed intervals. An example of how to calculate the overflow period of TCWD is shown below. In this sample task the LED flash interval is set at approximately 200 ms.

<p>System clock ϕ: 10 MHz Division: $\phi/8192$ TCWD set value: H'0C</p> $\text{TCWD overflow period} = \frac{1}{\text{System clock } \phi/8192} \times (256 - \text{TCWD set value})$ $= 0.8192 \text{ ms} \times (256 - 12)$ $= 199.9 \text{ ms}$
--

3. Interrupts

During interval timer operation an interval timer interrupt is generated each time an overflow occurs. An interval timer interrupt is requested whenever the OVF flag is set to 1 while the IEOVF bit in TCSRWD2 is set to 1. The OVF flag must be cleared to 0 in the interrupt handling routine.

4. Usage Note

- Switching between the watchdog timer mode and the interval timer mode

If the mode is switched between the watchdog timer mode and the interval timer mode while WDT is operating, errors could occur. Always halt the WDT (by clearing the WDON bit to 0) before switching the timer mode.

5. Port 9

Port 9 is a general I/O port with pins that function as both external interrupt input pins and PWM output pins.

- Port data register 9 (PDR9)

PDR9 is an 8-bit register that stores data for pins P93 to P90 of port 9. If port 9 is read, the values of PDR9 are read directly, regardless of the actual pin states.

- Port control register 9 (PCR9)

PCR9 selects inputs/outputs in bit units for pins to be used as I/O ports of port 9. Setting a PCR9 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the corresponding pin an input pin. The settings in PCR9 and in PDR9 are valid when the corresponding pins are set as I/O ports of port 9. PCR9 is a write-only register. These bits are always read as 1.

- Port mode register 9 (PMR9)

PMR9 controls the selection of functions for port 9 pins.

2.2 Assignment of Functions

Table 1 shows the assignment of functions in this sample task. The watchdog timer is operated using functions assigned as shown in table 1.

Table 1 Assignment of Functions

Elements	Description
TCSRWD1	Starts the WDT, controls enabling of writing initial and reset values to TCWD
TCSRWD2	Sets the watchdog timer mode
TCWD	Writes initial and reset values for up-counter and overflow interval
TMWD	Selects the input clock
PDR9	Stores output data for P93
PCR9	Sets P93 as an output pin
P93	Connected to an external LED. Flashes when timer overflow interrupts are generated

3. Principles of Operation

The principles of operation of this sample task are illustrated in figure 3. Internal timer operation is performed using the hardware and software processing shown in figure 3.

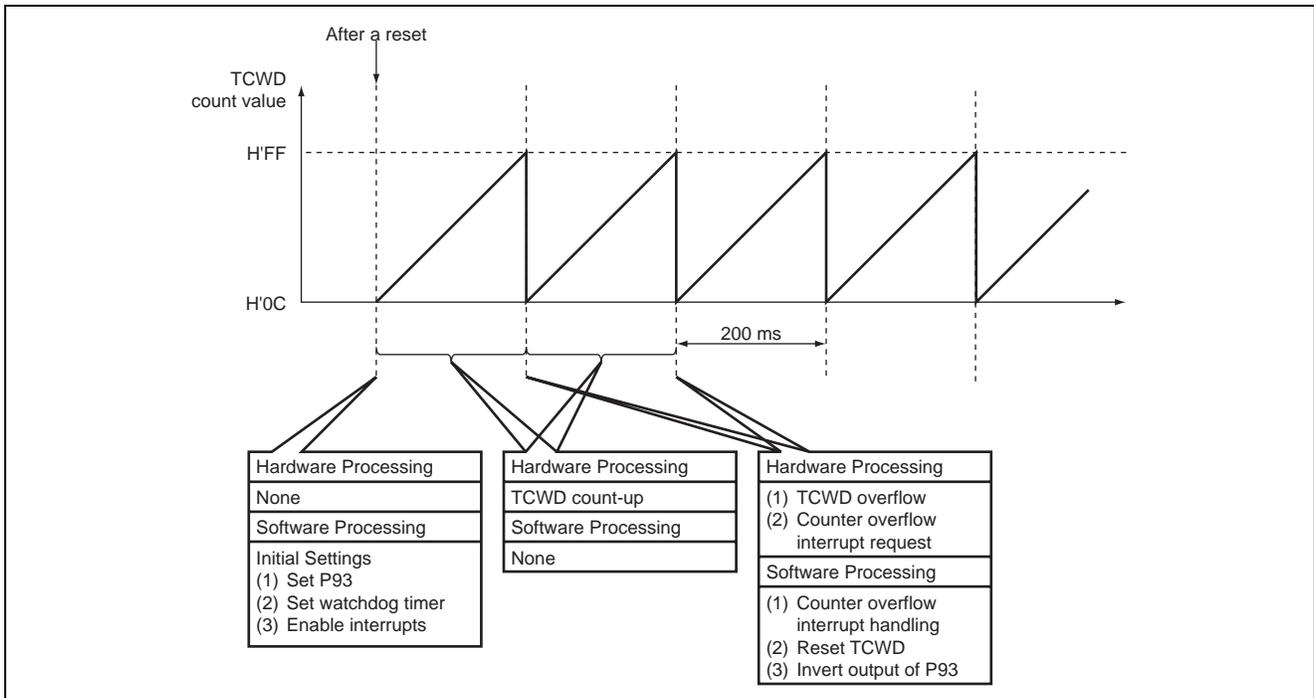


Figure 3 Principles of Operation in the Internal Timer Mode

4. Description of Software

4.1 Functions

Table 2 shows the functions used in this sample task.

Table 2 List of Functions

Function Name	Description
main	Performs initial setting of P93
init_wdt	Performs initial setting of WDT, sets TCWD, and starts WDT count
int_wovi	Handles WDT overflow interrupt requests, resets TCWD, performs processing for LED flashing

4.2 Constants

No constants are used in this sample task.

4.3 RAM Usage

No RAM is used in this sample task.

4.4 Modules

4.4.1 main() Function

1. Module Specifications

- Initial setting of P93

Table 3 Module Specifications

Item	Type	Variable	Description
Arguments	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

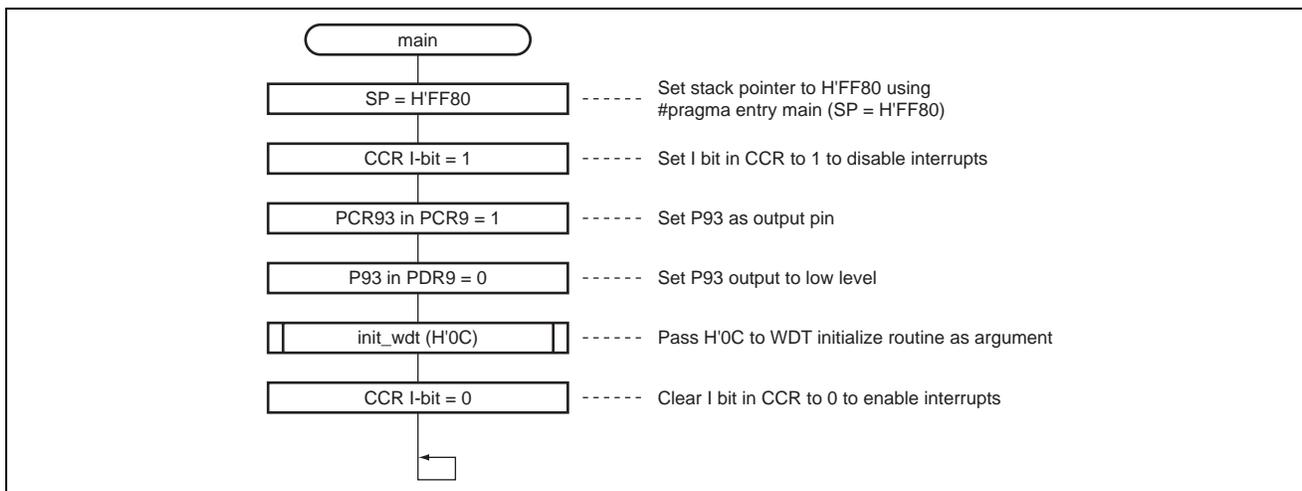
- PDR9 Port Data Register 9 Address: H'FFDC

Bit	Bit Name	Set Value	R/W	Description
3	P93	0	R/W	If port 9 is read while PCR9 is set to 1 the corresponding value stored in PDR9 is read directly, regardless of the actual pin state. If port 9 is read while PCR9 is cleared to 0 the corresponding pin state is read.

- PCR9 Port Control Register 9 Address: H'FFEC

Bit	Bit Name	Set Value	R/W	Description
3	PCR93	1	W	Setting a PCR9 bit to 1 makes the corresponding pin an output pin, while clearing the bit to 0 makes the pin an input pin. The settings in PCR9 and in PDR9 are valid when the corresponding pin is designated as a general I/O pin. PCR9 is a write-only register. These bits are always read as 1. 1: Output pin

3. Flowchart



4.4.2 init_wdt() Function

1. Module Specifications

- Initial setting of WDT, TCWD setting, and WDT count start

Table 4 Module Specifications

Item	Type	Variable	Description
Arguments	unsigned char	tc	Initial set value for TCWD. H'0C in this sample task
Return value	None	None	None

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- TCSRWD1 Timer Control/Status Register WD1 Address: H'FFB1

Bit	Bit Name	Set Value	R/W	Description
7	B6WI	1	R/W	Bit 6 Write Disable Bit 6 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
6	TCWE	1	R/W	Timer Counter WD Write Enable TCWD can be written when this bit is set to 1. When writing data to this bit the write value for bit 7 must be 0.
5	B4WI	1	R/W	Bit 4 Write Disable Bit 4 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
4	TCSRWE	1	R/W	Timer Control/Status Register WD Write Enable Writing to bits 2 and 0 of the register is enabled when this bit is set to 1. When writing data to this bit the write value for bit 5 must be 0.
3	B2WI	0	R/W	Bit 2 Write Disable Bit 2 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
2	WDON	1	R/W	Watchdog Timer On TCWD starts counting up when this bit is set to 1 and halts when it is cleared to 0. [Clearing conditions] <ul style="list-style-type: none"> • Reset • When 0 is written to the B2WI bit and 0 to the WDON bit while the TCSRWE bit is 1 [Setting condition] <ul style="list-style-type: none"> • When 1 is written to the B2WI bit and 0 to the WDON bit while the TCSRWE bit is 1
1	B0WI	0	R/W	Bit 0 Write Disable Bit 0 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Clearing conditions] <ul style="list-style-type: none"> • Reset by $\overline{\text{RES}}$ pin • When 0 is written to the B0WI bit and 0 to the WRST bit while the TCSRWE bit is 1 [Setting condition] <ul style="list-style-type: none"> • When TCWD overflows and an internal reset signal is generated

- TCSRWD2 Timer control/status register WD2 Address: H'FFB2

Bit	Bit Name	Set Value	R/W	Description
7	OVF	0	R/(W)* ¹	Overflow flag Indicates that TCWD has overflowed (changed from H'FF to H'00). [Setting condition] <ul style="list-style-type: none"> • When TCWD overflows (changes from H'FF to H'00) • However, when internal reset request generation is selected in the watchdog timer mode, this bit is cleared automatically by an internal reset after it has been set. [Clearing condition] <ul style="list-style-type: none"> • When TCSRWD2 is read when OVF = 1, then 0 is written to OVF*⁴
6	B5WI	0	R/(W)* ²	Bit 5 Write Disable Bit 5 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
5	WT/IT	1	R/(W)* ³	Timer Mode Select Selects whether the WDT is used as a watchdog timer or interval timer. 0: Watchdog timer mode 1: Interval timer mode
4	B3WI	1	R/(W)* ²	Bit 3 Write Disable Bit 3 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
3	IEOVF	0	R/(W)* ³	Overflow Interrupt Enable Enables or disables overflow interrupt requests in the interval timer mode. 0: Disables an overflow interrupt 1: Enables an overflow interrupt
2-0	—	All 1	—	Reserved These bits are always read as 1.

- Notes: 1. Only 0 can be written to clear the flag.
 2. Write operation is necessary because this bit controls data writing to another bit. This bit is always read as 1.
 3. Writing is possible only when the write conditions are satisfied.
 4. In the subactive mode, clear this flag after setting the CKS3 to CKS0 bits in TMWD to B'0XXX (internal oscillator).

- TCWD Timer Counter WD Address: H'FFB3

Bit	Bit Name	Set Value	R/W	Description
7	TCW7	0	R/W	TCWD is an 8-bit readable/writable up-counter.
6	TCW6	0	R/W	
5	TCW5	0	R/W	
4	TCW4	0	R/W	
3	TCW3	1	R/W	
2	TCW2	1	R/W	
1	TCW1	0	R/W	
0	TCW0	0	R/W	

- TMWD Timer Mode WD Address: H'FFB0

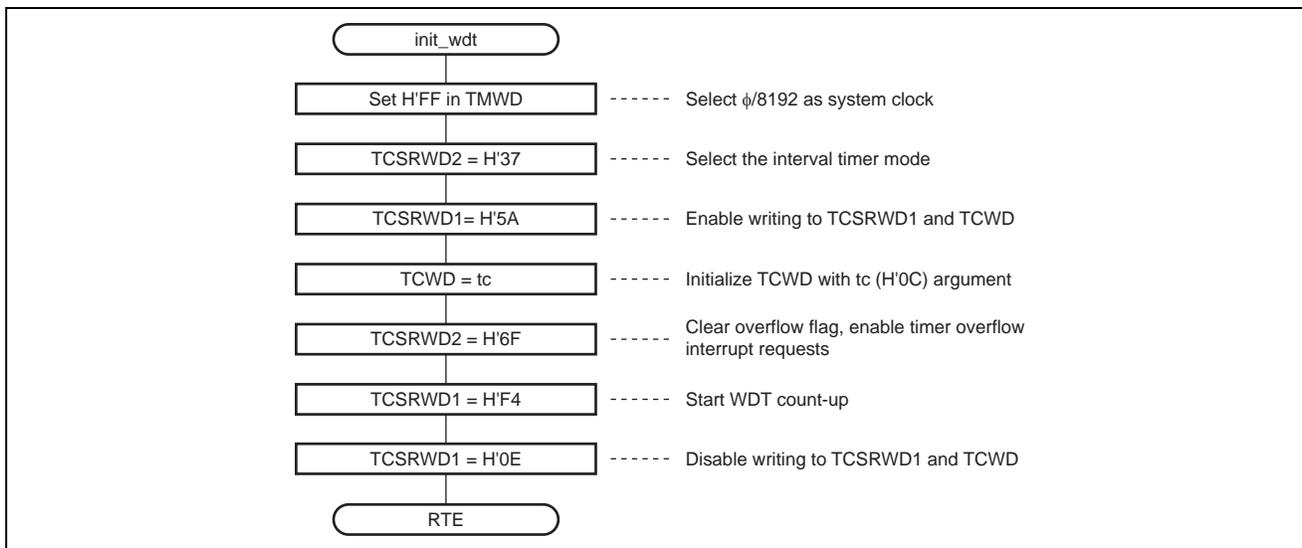
Bit	Bit Name	Set Value	R/W	Description
7-4	—	All 1	—	These bits are reserved. They are always read as 1.
3	CKS3	1	R/W	Clock select 3 to 0
2	CKS2	1	R/W	Select the clock to be input to TCWD.
1	CKS1	1	R/W	1000: Internal clock: counts on $\phi/64$
0	CKS0	1	R/W	1001: Internal clock: counts on $\phi/128$ 1010: Internal clock: counts on $\phi/256$ 1011: Internal clock: counts on $\phi/512$ 1100: Internal clock: counts on $\phi/1,024$ 1101: Internal clock: counts on $\phi/2,048$ 1110: Internal clock: counts on $\phi/4,096$ 1111: Internal clock: counts on $\phi/8,192$ 0XXX: Internal oscillator: counts on $R_{OSC}/2,048$

For details on the internal oscillator overflow periods, see section 24, Electrical Characteristics, in the Hardware Manual.

In the active (medium-speed) mode or the sleep (medium-speed) mode, the setting of B'0XXX and the interval timer mode is disabled.

[Legend] X: Don't care.

3. Flowchart



4.4.3 int_wovi() Function

1. Module Specifications

- Handles WDT overflow interrupt requests, resets TCWD, performs processing for LED flashing

2. Internal Registers Used

The internal registers used in this sample task are shown below. The set values shown are those used in the sample task and differ from the initial values.

- TCSRWD1 Timer Control/Status Register WD1 Address: H'FFB1

Bit	Bit Name	Set Value	R/W	Description
7	B6WI	0	R/W	Bit 6 Write Disable Bit 6 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
6	TCWE	1	R/W	Timer Counter WD Write Enable TCWD can be written when this bit is set to 1. When writing data to this bit the write value for bit 7 must be 0.
5	B4WI	1	R/W	Bit 4 Write Disable Bit 4 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
4	TCSRWE	0	R/W	Timer Control/Status Register WD Write Enable Bits 2 and 0 of the register can be written when this bit is set to 1. When writing data to this bit the write value for bit 5 must be 0.
3	B2WI	1	R/W	Bit 2 Write Disable Bit 2 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
2	WDON	1	R/W	Watchdog Timer On TCWD starts counting up when this bit is set to 1 and halts when it is cleared to 0. [Clearing conditions] <ul style="list-style-type: none"> • Reset • When 0 is written to the B2WI bit and 0 to the WDON bit while the TCSRWE bit is 1 [Setting condition] <ul style="list-style-type: none"> • When 1 is written to the B2WI bit and 0 to the WDON bit while the TCSRWE bit is 1
1	B0WI	1	R/W	Bit 0 Write Disable Bit 0 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
0	WRST	0	R/W	Watchdog Timer Reset [Clearing conditions] <ul style="list-style-type: none"> • Reset by \overline{RES} pin • When 0 is written to the B0WI bit and 0 to the WRST bit while the TCSRWE bit is 1 [Setting condition] <ul style="list-style-type: none"> • When TCWD overflows and an internal reset signal is generated

- TCSRWD2 Timer Control/Status Register WD2 Address: H'FFB2

Bit	Bit Name	Set Value	R/W	Description
7	OVF	0	R/(W) ^{*1}	Overflow flag Indicates that TCWD has overflowed (changed from H'FF to H'00). [Setting condition] <ul style="list-style-type: none"> • When TCWD overflows (changes from H'FF to H'00) • However, when internal reset request generation is selected in the watchdog timer mode, this bit is cleared automatically by an internal reset after it has been set. [Clearing condition] <ul style="list-style-type: none"> • When TCSRWD2 is read when OVF = 1, then 0 is written to OVF^{*4}
6	B5WI	1	R/(W) ^{*2}	Bit 5 Write Disable Bit 5 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
5	WT/IT	1	R/(W) ^{*3}	Timer Mode Select Selects whether the WDT is used as a watchdog timer or interval timer. 0: Watchdog timer mode 1: Interval timer mode
4	B3WI	0	R/(W) ^{*2}	Bit 3 Write Disable Bit 3 of the register can be written only when the write value for this bit is 0. This bit is always read as 1.
3	IEOVF	0	R/(W) ^{*3}	Overflow Interrupt Enable Enables or disables overflow interrupt requests in the interval timer mode. 0: Disables an overflow interrupt 1: Enables an overflow interrupt
2-0	—	All 1	—	Reserved These bits are always read as 1.

- Notes: 1. Only 0 can be written to clear the flag.
 2. Write operation is necessary because this bit controls data writing to another bit. This bit is always read as 1.
 3. Writing is possible only when the write conditions are satisfied.
 4. In the subactive mode, clear this flag after setting the CKS3 to CKS0 bits in TMWD to B'0XXX (internal oscillator).

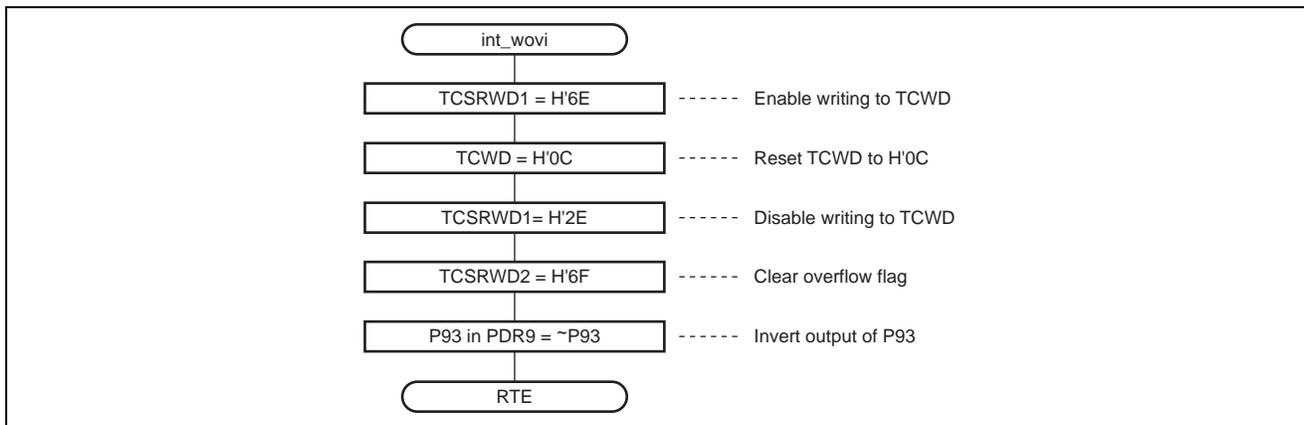
- TCWD Timer Counter WD Address: H'FFB3

Bit	Bit Name	Set Value	R/W	Description
7	TCW7	0	R/W	TCWD is an 8-bit readable/writable up-counter.
6	TCW6	0	R/W	
5	TCW5	0	R/W	
4	TCW4	0	R/W	
3	TCW3	1	R/W	
2	TCW2	1	R/W	
1	TCW1	0	R/W	
0	TCW0	0	R/W	

- PDR9 Port Data Register 9 Address: H'FFDC

Bit	Bit Name	Set Value	R/W	Description
3	P93	0	R/W	If port 9 is read while PCR9 bit is set to 1, the value stored in PDR9 is read regardless of the actual pin state. If port 9 is read while PCR9 bit is cleared to 0, the pin state is read.

3. Flowchart



4.5 Link Address Specifications

Section Name	Address
CVECT	H'0000
P	H'0100

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Mar.18.05	—	First edition issued

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