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SH7211 Group

Example of Setting SDRAM Interface

Introduction

This application note explains how to connect and use SDRAM, and is intended for reference to help in the design of user software.

Target Device

SH7211

Contents

1. Introduction

1.1 Specification

- 128-Mbit (2 Mwords × 16 bits × 4 banks) SDRAM is connected.
- SDRAM is connected with 16-bit bus width.
- The CS3 space is selected as the external connection space.
- SDRAM is initialized using the SDRAM interface function of the SH7211.

1.2 Used Module

Bus state controller (BSC)

1.3 Applicable Conditions

- Microcontroller: SH7211
- Operating Frequency: Internal clock 160 MHz
  Bus clock 40 MHz
  Peripheral clock 40 MHz
- Compiler: SuperH RISC engine family C/C++ compiler package Ver.9.01, manufactured by Renesas Technology

2. Description of Sample Application

2.1 Operational Overview of Module Used

The bus state controller of the SH7211 incorporates SDRAM interface function that enables direct connection to SDRAM. The specification of SDRAM used in this sample application is listed in table 1.

Table 1 Specification of SDRAM Used in this Sample Application

Item	Description
Configuration	2,097,152 words × 16 bits × 4 banks
Capacity	128 Mbits × 1
CAS latency	2 or 3 (programmable)
Refresh cycle	4096 cycles/64 ms
Row address	A11 to A0
Column address	A8 to A0
Precharge	Precharge command input A10 pin = “high”: all the banks are precharged A10 pin = “low”: the banks selected by BA0 and BA1 are precharged

2.1.1 Bus State Controller (BSC)

The bus state controller (BSC) outputs control signals to external devices and various types of memory that are connected to the external address space. This enables direct connections to SRAM, SDRAM, and other memory storage devices, and external devices.

An overview of the BSC is provided in table 2.

Table 2 Overview of BSC

Item	Description
External address space	Supports a maximum of 64 Mbytes for each of areas CS0 to CS7. Can specify the normal space interface, SRAM interface with byte selection, burst ROM (clock synchronous or asynchronous), MPX-I/O, and SDRAM.
Data bus width	8 or 16 bits.
Wait	Can insert wait cycles into each address space. Can insert wait cycles into each read access and write access.
Connectable memory devices	SRAM, burst ROM, MPX-I/O, SDRAM, and SRAM with byte selection.
Bus arbitration	Can release the bus mastership after receiving a bus mastership request from external devices.
Refresh function	Supports the auto-refresh and self-refresh functions.

2.1.2 SDRAM Interface Connection Configuration

The SH7211 is capable of connecting SDRAM, which meets the conditions listed in table 3, to area 2 (CS2 space) or area 3 (CS3 space). It supports burst read/single write (burst length 1) and burst read/burst write (burst length 1) as the SDRAM operating mode. In this sample application, mode 2 (MCU extension mode 2) is used as the MCU operation mode. For details, refer to the section on MCU operating mode in the SH7211 Group Hardware Manual.

The specification of SDRAM connectable to the SH7211 is listed in table 3. The SH7211 memory map for this sample application is illustrated in figure 1. Note that when only a single SDRAM is to be used, it should be connected to the CS3 space.

Table 3 Specification of SDRAM Connectable to the SH7211

Item	Description
Row address	11/12/13 bits
Column address	8/9/10 bits
Number of banks	Less than or equal to 4

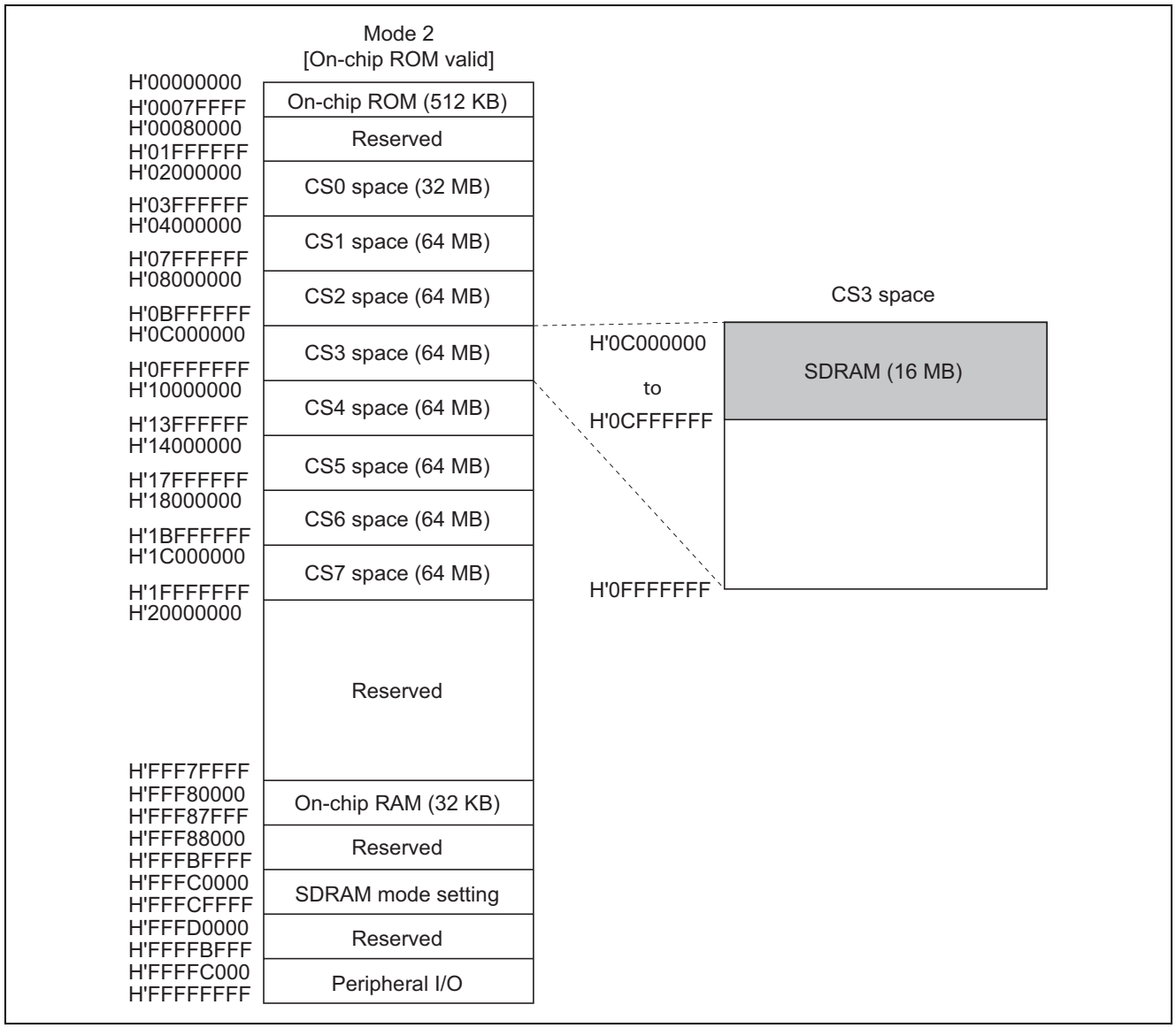


Figure 1 SH7211 Memory Map in this Sample Application

2.2 Operational Settings for Sample Application

In order to connect SDRAM with the SH7211, changing the port settings by using the pin function controller (PFC) is necessary.

An example of connecting SDRAM with the SH7211 is given in figure 2. Also, an example of setting the pin function controller (PFC) in this sample application is shown in table 4.

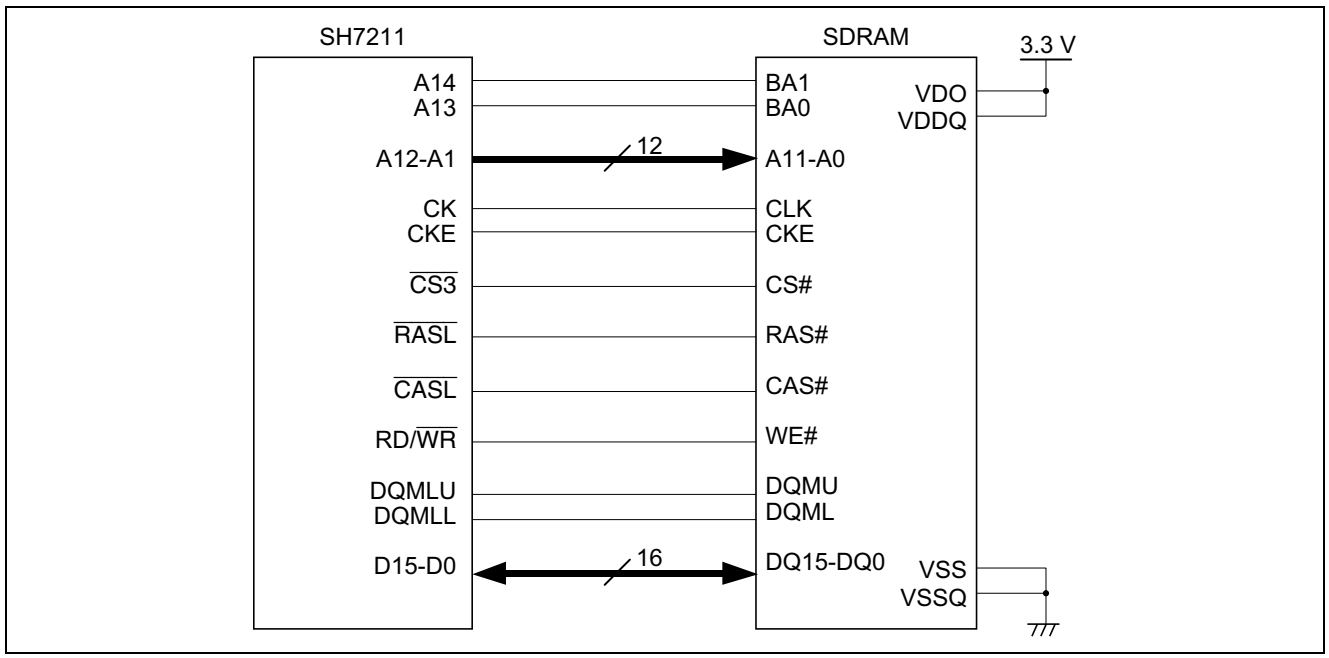


Figure 2 Example of Connecting with SDRAM

Table 4 Example of Setting PFC

PFC Initial Function	SDRAM Connecting Pin
PA14 to PA0	A14 to A0
PD15 to PD0	D15 to D0
PB9/PB8	$\overline{\text{DQMLU}}$/$\overline{\text{DQMLL}}$
PB1	RD/$\overline{\text{WR}}$
PB6/PB5	$\overline{\text{CASL}}$/$\overline{\text{RASL}}$
PB3/PB4	CK/CKE
PB17	$\overline{\text{CS3}}$

2.3 Operation of Sample Application

This section describes read and write operation in the sample program.

1. Read Operation
   An example of SDRAM single read timing at 40-MHz bus clock is provided in figure 3.
   The SH7211 performs the following operation in each cycle.

- Tr: Issue an ACTV (activate rows and banks) command
- Trw1, Twr2: Wait cycles from ACTV command to READ (A)/WRIT (A)
  Wait cycles specified by the WTRCD[1:0] bits in CS3WCR are inserted.
- Tc1: Issue a READ (A) command
- Tcw: Wait cycles from Tc1 cycle to Td1 cycle
- Td1: Retrieve read data
- Tde: Idle cycle required for transferring the read data to the LSI
  One idle cycle is always generated at all the time of burst or single read operation.
- Tap1, Tap2: Wait cycles for auto-precharge completion
  Wait cycles specified by the WTRP[1:0] bits in CS3WCR are inserted.

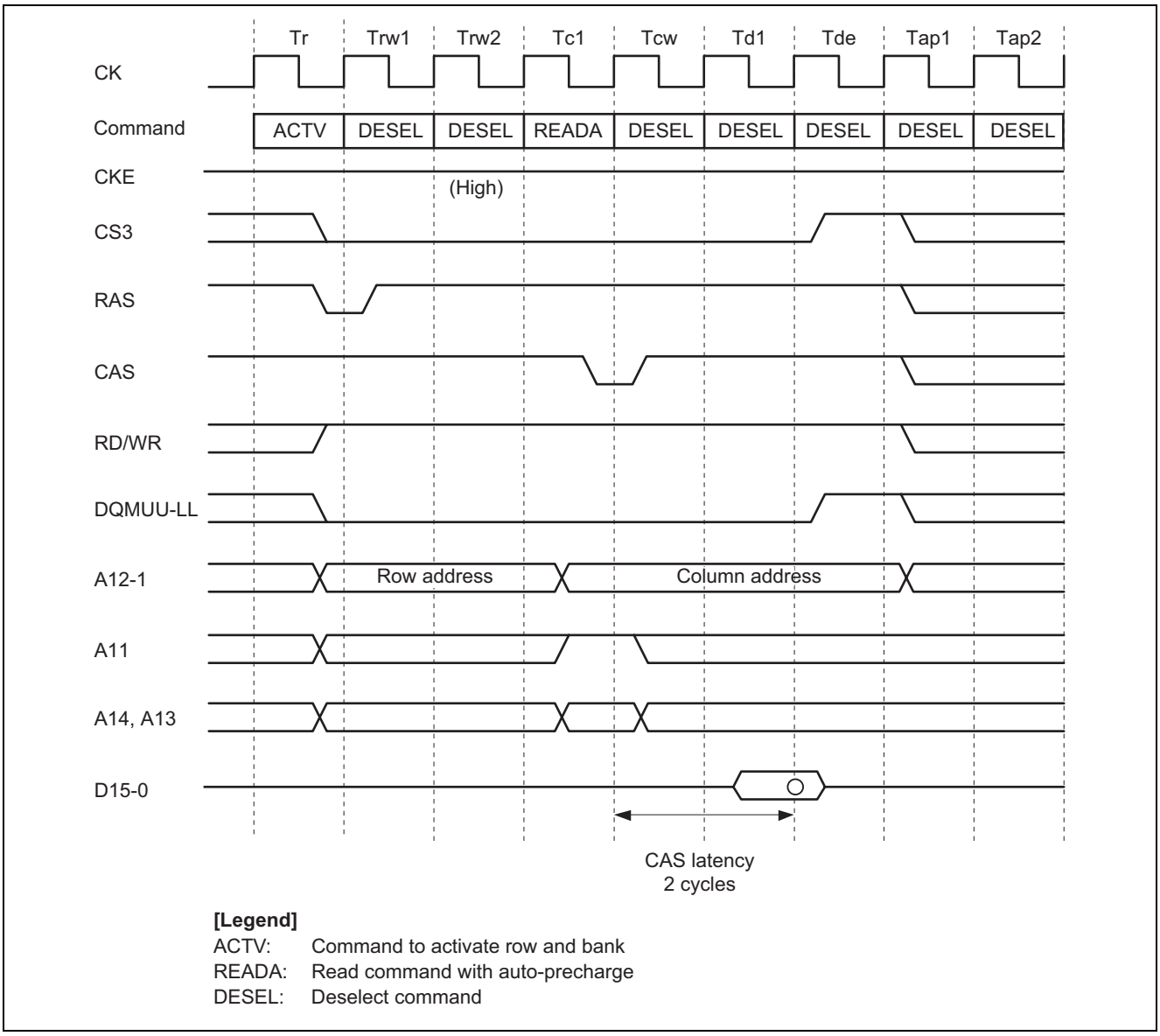


Figure 3 Example of SDRAM Single Read Timing (Bus Clock 40 MHz)

2. Write Operation
   An example of SDRAM single write timing at 40-MHz bus clock is provided in figure 3.
   The SH7211 performs the following operation in each cycle.

- Tr: Issue an ACTV (activate rows and banks) command
- Trw1, Trw2: Wait cycles from ACTV command to READ (A)/WRIT (A)
  Wait cycles specified by the WTRCD[1:0] bits in CS3WCR are inserted.
- Tc1: Issue a WRITA command
- Trwl1, Trwl2: Wait cycles for auto-precharge activation
  Wait cycles specified by the TRWL[1:0] bits in CS3WCR are inserted.
- Tap1, Tap2: Wait cycles for auto-precharge completion
  Wait cycles specified by the WTRP[1:0] bits in CS3WCR are inserted.

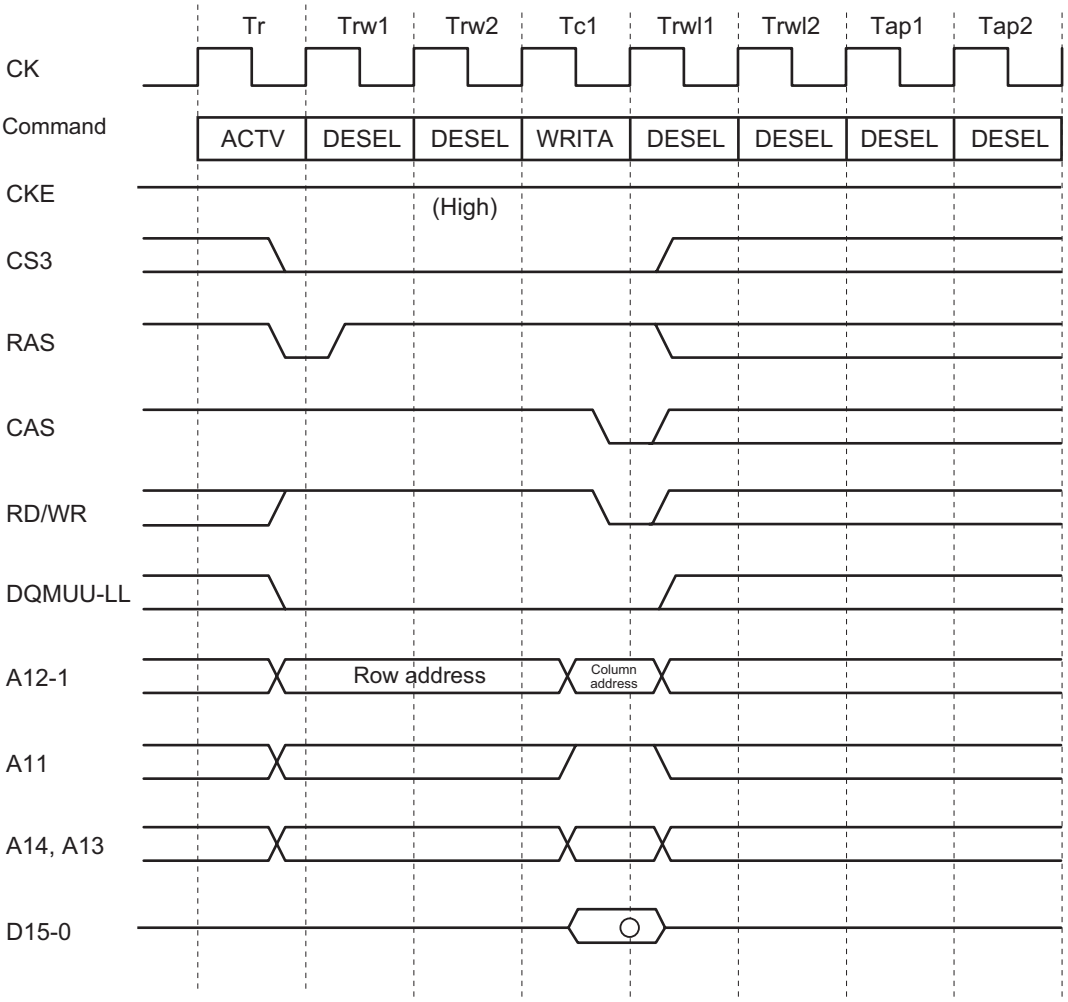


Figure 4 Example of SDRAM Single Write Timing (Bus Clock 40 MHz)

2.4 Procedure for Setting Modules Used

This section describes the procedure for specifying initial settings for writing to SDRAM. In this sample application, the pin function controller (PFC) and the bus state controller (BSC) are initialized before executing the main function. Flowcharts of setting the PFC and the BSC are illustrated in figure 4 and 5, respectively. In addition, a flowchart of the sample program is shown in figure 6.

For details on registers, refer to SH7211 Group Hardware Manual.

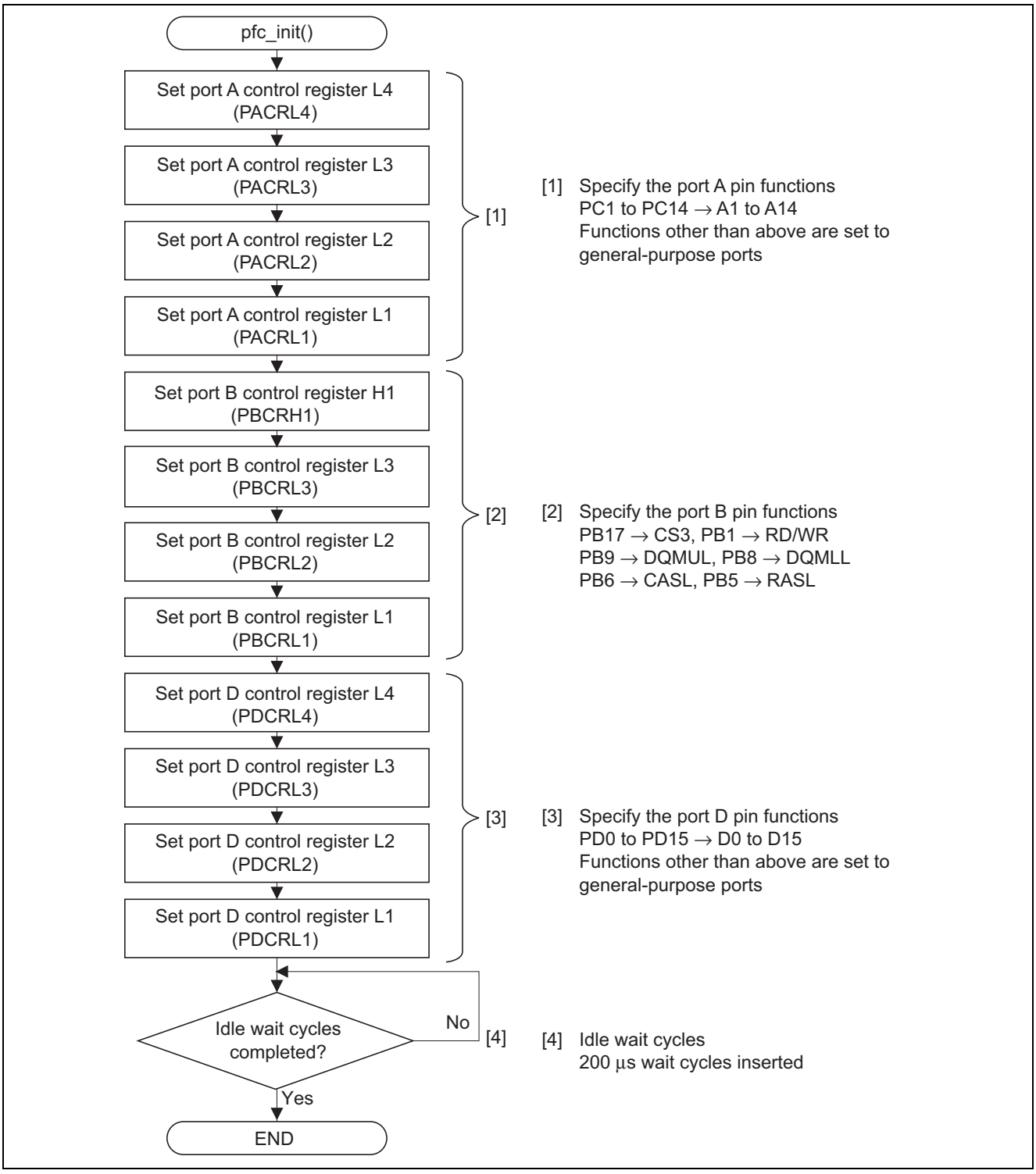


Figure 5 Flowchart of Setting Pin Function Controller

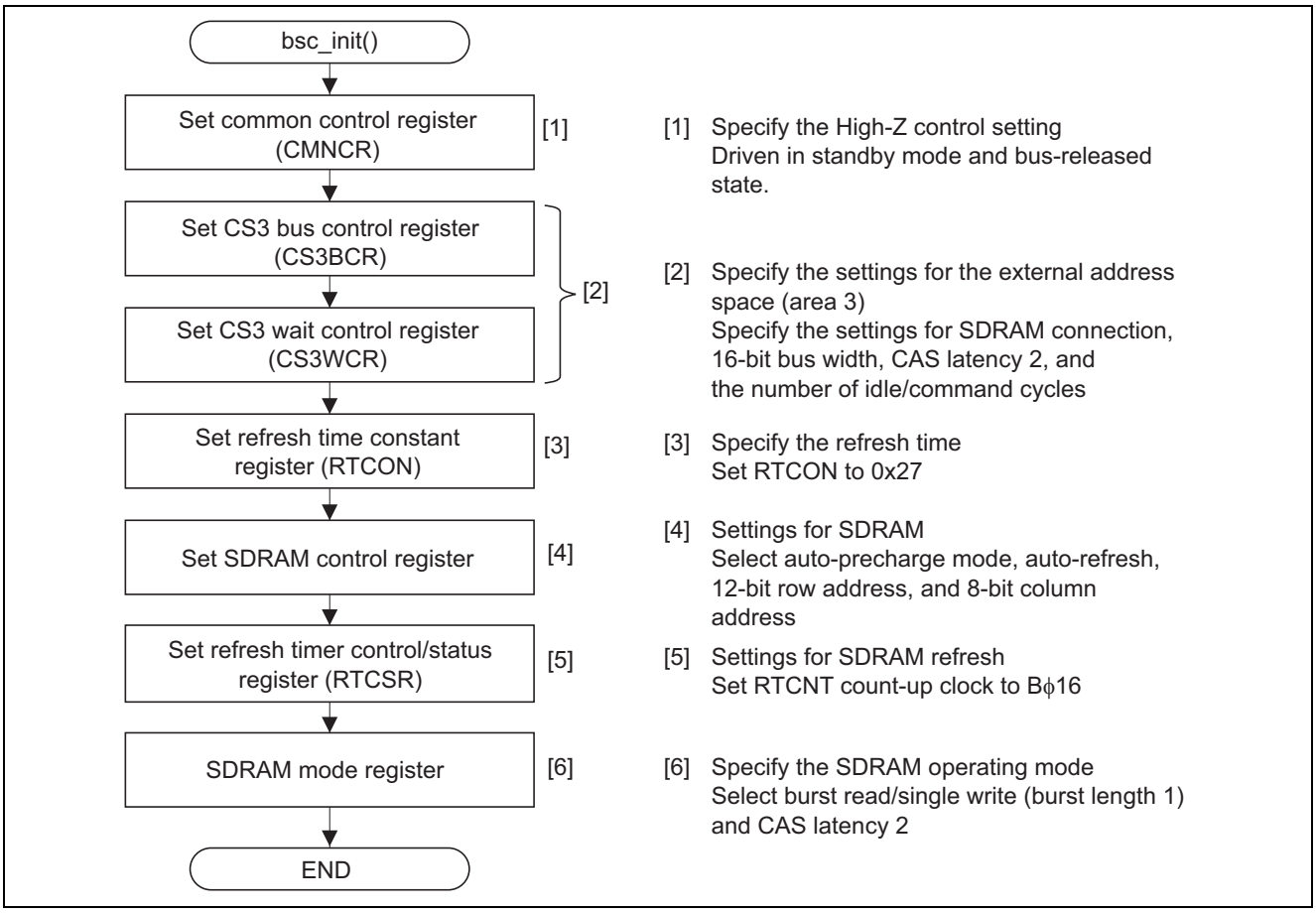
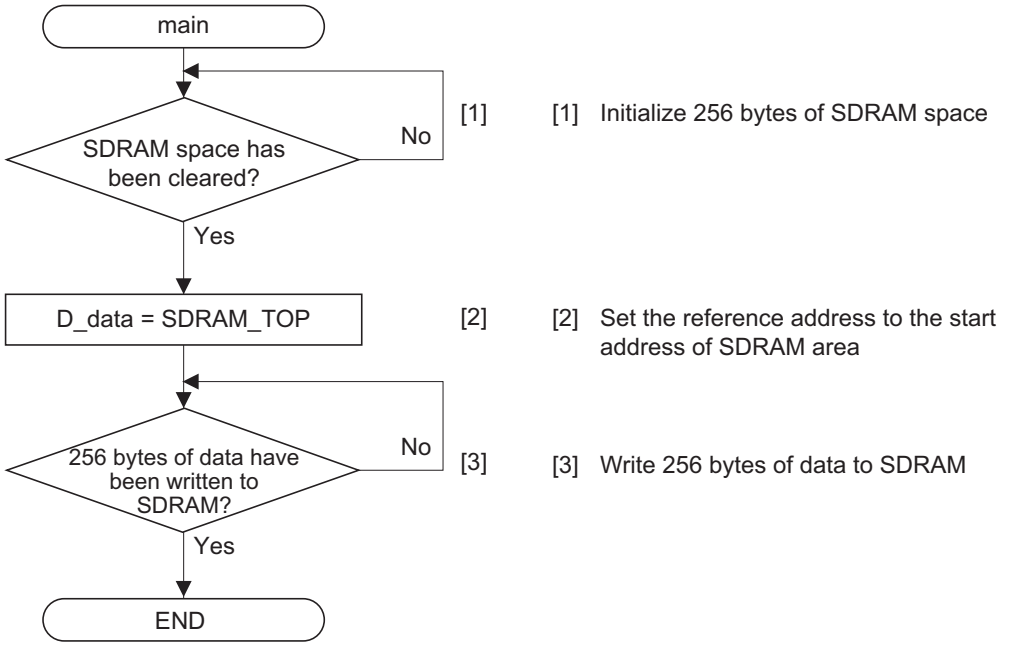


Figure 6 Flowchart of Setting Bus State Controller (BSC)



* In this sample application, sleep processing is performed after main processing is completed.

Figure 7 Flowchart of Sample Program

2.5 Register Settings for Sample Program

2.5.1 Clock Pulse Generator (CPG)

The settings of the clock pulse generator for the sample program are listed in table 5.

Table 5 Settings of Clock Pulse Generator

Register Name	Address	Setting Value	Description
Frequency control register (FRQCR)	H'FFFE0010	H'1303	CKOEN = "B'1": Clock is output STC[1:0] = "B'00": PLL circuit multiplication ratio ×1 IFC[2:0] = "B'000": Internal clock × 1 PFC[2:0] = "B'011": Peripheral clock × 1/4

2.5.2 Settings of Pin Function Controller (PFC)

Pins for connecting SDRAM are enabled by setting the pin function controller (PFC).

The settings of the PFC are listed in table 6.

Table 6 Settings of PFC

Register Name	Address	Setting Value	Description
Port A control register L4 (PACRL4)	H'FFFE3810	H'0111	PA14MD[2:0] = "B'001": A14 output PA13MD[2:0] = "B'001": A13 output PA12MD[2:0] = "B'001": A12 output
Port A control register L3 (PACRL3)	H'FFFE3812	H'1111	PA11MD[2:0] = "B'001": A 11 output PA10MD[2:0] = "B'001": A10 output PA9MD[2:0] = "B'001": A9 output PA8MD[2:0] = "B'001": A8 output
Port A control register L2 (PACRL2)	H'FFFE3814	H'1111	PA7MD[2:0] = "B'001": A7 output PA6MD[2:0] = "B'001": A6 output PA5MD[2:0] = "B'001": A5 output PA4MD[2:0] = "B'001": A4 output
Port A control register L1 (PACRL1)	H'FFFE3816	H'1111	PA3MD[2:0] = "B'001": A3 output PA2MD[2:0] = "B'001": A2 output PA1MD[2:0] = "B'001": A1 output PA0MD[2:0] = "B'001": A0 output
Port B control register H1 (PBCRH1)	H'FFFE388E	H'0010	PB17MD[2:0] = "B'001": CS3 output
Port B control register L3 (PBCRL3)	H'FFFE3892	H'0011	PB9MD[2:0] = "B'001": WE1/DQMLU PB8MD[2:0] = "B'001": WE0/DQMLL
Port B control register L2 (PBCRL2)	H'FFFE3894	H'0111	PB6MD[2:0] = "B'001": CASL output PB5MD[2:0] = "B'001": RASL output PB4MD[2:0] = "B'001": CKE output
Port B control register L1 (PBCRL1)	H'FFFE3896	H'1010	PB3MD[2:0] = "B'001": CK output PB1MD[2:0] = "B'001": RD/WR output
Port D control register L4 (PDCRL4)	H'FFFE3990	H'1111	PD15MD[2:0] = "B'001": D15 output PD14MD[2:0] = "B'001": D14 output PD13MD[2:0] = "B'001": D13 output PD12MD[2:0] = "B'001": D12 output
Port D control register L3 (PDCRL3)	H'FFFE3992	H'1111	PD11MD[2:0] = "B'001": D11 output PD10MD[2:0] = "B'001": D10 output PD9MD[2:0] = "B'001": D9 output PD8MD[2:0] = "B'001": D8 output
Port D control register L2 (PDCRL2)	H'FFFE3994	H'1111	PD7MD[2:0] = "B'001": D7 output PD6MD[2:0] = "B'001": D6 output PD5MD[2:0] = "B'001": D5 output PD4MD[2:0] = "B'001": D4 output
Port D control register L1 (PDCRL1)	H'FFFE3996	H'1111	PD3MD[2:0] = "B'001": D3 output PD2MD[2:0] = "B'001": D2 output PD1MD[2:0] = "B'001": D1 output PD0MD[2:0] = "B'001": D0 output

2.5.3 Settings of Bus State Controller

The type of the memory device connected to the CS3 space, the data bus width, and the number of wait cycles are specified.

The settings of the bus state controller (BSC) are listed in table 7.

Table 7 Settings of BSC

Register Name	Address	Setting Value	Description
Common control register (CMNCR)	H'FFFC0000	H'00000003	HIZMEM = "B'1": Driven HIZCNT = "B'1": CKE, RASL, and CASL are driven in standby mode and bus-released state.
CS3 space bus control register (CS3BCR)	H'FFFC0010	H'10004400	IWW[2:0] = "B'001": 1 idle cycle inserted TYPE[2:0] = "B'100": SDRAM BSZ[1:0] = "B'10": 16-bit bus width
CS3 space wait control register (CS3WCR)	H'FFFC0034	H'00004891	WTRP[1:0] = "B'10": 2 wait cycles WTRCD[1:0] = "B'10": 2 wait cycles A3CL[1:0] = "B'01": CAS latency 2 cycles TRWL[1:0] = "B'10": 2 wait cycles WTRC[1:0] = "B'01": 3 cycles
Refresh timer control/status register (RTCSR)	H'FFFC0050	H'A55A0010	CKS[2:0] = "B'010": Bϕ16 RRC[2:0] = "B'000": Once
Refresh timer constant register (RTCON)	H'FFFC0058	H'A55A0027	When the RTCON value matches the RTCNT value, a refresh request is made.*
SDRAM control register (RDCR)	H'FFFC004C	H'00000809	RFSH = "B'1": Perform refresh A3ROW = "B'01": Row address 12 bits A3COL = "B'01": Column address 9 bits

Note: * 1 cycle: 400 ns (40 MHz/16 = 2.5 MHz)
Refresh request interval of this SDRAM: 15.625 µs
15.625 µs/400 ns = 39 (0x27) cycles per number of times of refresh

Note: When writing, set the upper 16 bits to H'A55A to disable write protection.

2.6 Settings of SDRAM Mode Register

The SDRAM mode register is set by inputting a specific address to SDRAM. Setting the SDRAM mode register specifies the CAS latency and the burst length are specified.

The SH7211 supports burst read/single write (burst length 1), burst read/burst write (burst length 1), sequential wrap type (burst type), and CAS latency 2 or 3.

Access addresses for setting the mode register and their respective SDRAM modes are listed in the tables below.

A. Settings of Area 2

- Burst read/single write (burst length 1)

Data Bus Width	CAS Latency	Access Address	External Address Pin
16	2	H'FFFC4440	H'00000440
	3	H'FFFC4460	H'00000460

- Burst read/burst write (burst length 1)

Data Bus Width	CAS Latency	Access Address	External Address Pin
16	2	H'FFFC4040	H'00000040
	3	H'FFFC4060	H'00000060

B. Settings of Area 3

- Burst read/single write (burst length 1)

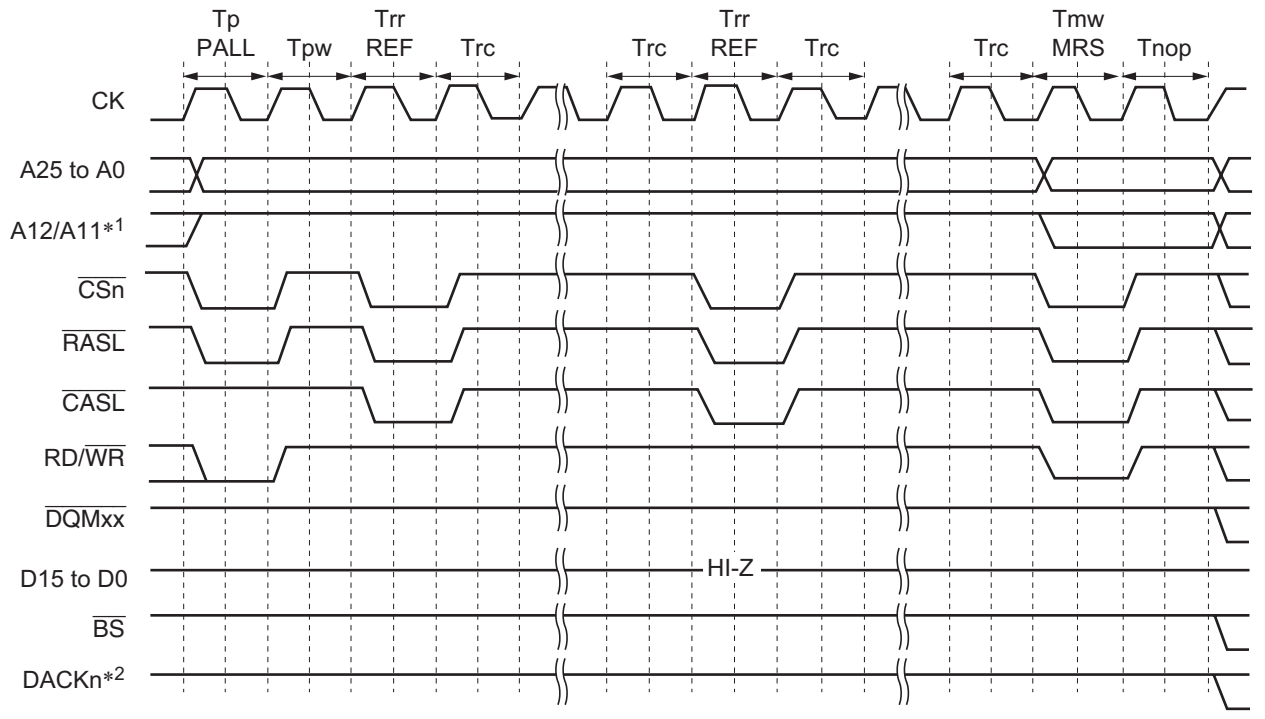
Data Bus Width	CAS Latency	Access Address	External Address Pin
16	2	H'FFFC5440	H'00000440
	3	H'FFFC5460	H'00000460

- Burst read/burst write (burst length 1)

Data Bus Width	CAS Latency	Access Address	External Address Pin
16	2	H'FFFC5040	H'00000040
	3	H'FFFC5060	H'00000060

In this sample application, the following settings of the SDRAM mode register are specified. An example of timing of writing to the SDRAM mode register is provided in figure 7.

- Burst length: burst read/single write (burst length 1)
- Area: area 3
- CAS latency: 2 cycles



Notes: 1. Address pin to be connected to pin A10 of SDRAM.
2. The waveform for DACKn is when active low is specified.

Figure 8 Example of Timing of Writing to SDRAM Mode Register

The SH7211 issues commands in the following order when setting the SDRAM mode register.

- All bank precharge command
- Auto refresh command (8 times)
- Mode register write command

Completing the setting of the mode register enables the use of SDRAM.

SDRAM requires a certain amount of idle time during a period from power-on to all-bank precharge. In this sample application, 200 µs of wait idle time is made in the pfc_init function.

For the necessary idle time, refer to the manual of SDRAM to be used.

3. Documents for Reference

- Software Manual
  SH-2A, SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website
  Hardware Manual
  SH7211 Group Hardware Manual
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