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# SH7285 Group

## Example of Initialization

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### Summary

This application note gives an example of configuration items to activate the SH7285 Microcomputers (MCUs).

### Target Device

SH7285 MCU

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## 1. Introduction

### 1.1 Specifications

Configure the clock pulse generator (CPG) after the reset is canceled.

### 1.2 Modules Used

- Clock pulse generator (CPG)

### 1.3 Applicable Conditions

MCU	SH7285
Operating Frequency	Internal clock: 100 MHz Bus clock: 50 MHz Peripheral clock: 50 MHz
Integrated Development Environment	Renesas Technology Corp. High-performance Embedded Workshop Ver.4.04.01
C compiler	Renesas Technology SuperH RISC engine Family C/C++ compiler package Ver.9.01 Release 01
Compiler options	Default setting in the High-performance Embedded Workshop (-cpu=sh2 -debug -gbr=auto -global_volatile=0 -opt_range=all -infinite_loop=0 -del_vacant_loop=0 -struct_alloc=1)

## 2. Applications

Configuration program for the minimum hardware setup is required to execute the main function created in C code. This application note describes the configuration example for the configuration program.

All of the SH7285 application notes assume to use the sample program described in this application note as the configuration program.

### 2.1 Sample Program

The configuration program consists of several source files such as the `resetprg.c`, describing the `PowerON_Reset_PC` function, and the `hwsetup.c`, describing the hardware setup function. Main source files are as follows.

- `resetprg.c`
- `hwsetup.c`
- `cpg.c`

"`resetprg.c`" is a source file created on the file automatically generated by the High-performance Embedded Workshop, and describes the `PowerON_ResetPC` function. The `PowerON_ResetPC` function initially executed after the reset is canceled. Its beginning address is set in the reset vector defined by the `vecttbl.c`.

"`hwsetup.c`" describes the `HardwareSetup` function called by the `PowerON_Reset_PC` function. The `HardwareSetup` function calls the `io_set_cpg` function to set the CPG.

"`cpg.c`" describes the `io_set_cpg` function which is called from the `HardwareSetup` function. The `io_set_cpg` function sets the frequency control registers (`FRQCR`, `MCLKCR`, and `ACLKCR`) to clear the module standby function for internal peripheral modules.

Figure 1 shows flow charts of the `PowerON_Reset_PC` function, the `HardwareSetup` function, and the `io_set_cpg` function.

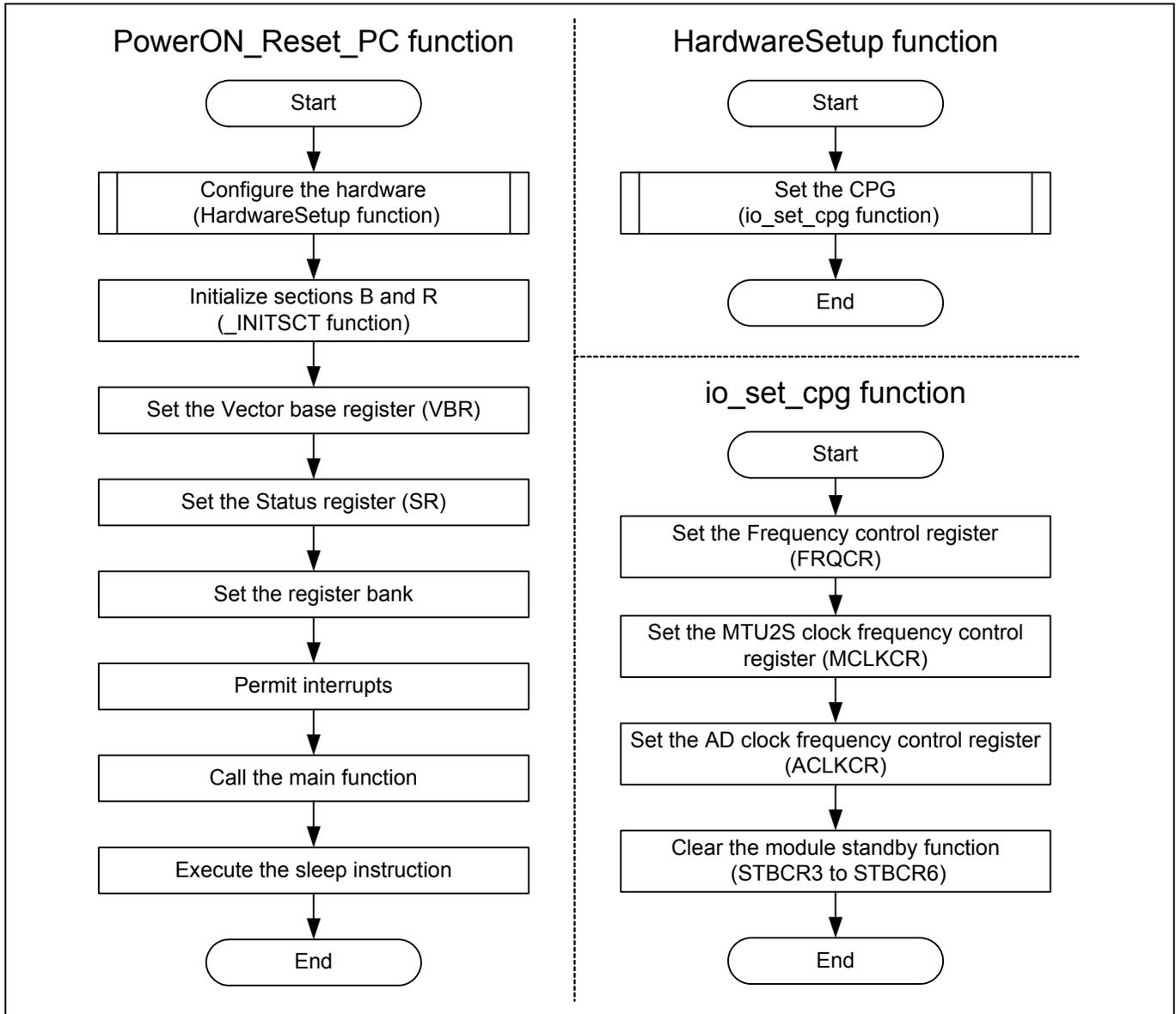


Figure 1 Flow Charts of Functions (PowerON\_Reset\_PC, HardwareSetup, io\_set\_cpg)

## 2.2 CPG Operation

CPG generates the internal clock ( $I\phi$ ), bus clock ( $B\phi$ ), peripheral clock ( $P\phi$ ), MTU2S clock ( $M\phi$ ), and AD clock ( $A\phi$ ). It also controls the clock in low power mode.

The following table gives an overview of the CPG. Figure 2 shows the CPG block diagram.

**Table 1 CPG Overview**

Item	Description
Generate clock	<ul style="list-style-type: none"> <li>• Internal clock (<math>I\phi</math>): Used by the CPU</li> <li>• Bus clock (<math>B\phi</math>): Used by the external bus interface</li> <li>• Peripheral clock (<math>P\phi</math>): Used by the internal peripheral module</li> <li>• MTU2S clock (<math>M\phi</math>): Used by the MTU2S module</li> <li>• AD clock (<math>A\phi</math>): Used by the AD module</li> </ul>
Change frequency	<ul style="list-style-type: none"> <li>• Sets frequencies for internal clock, bus clock, peripheral clock, MTU2S clock, and AD clock independently using the PLL (Phase Locked Loop) circuit and divider circuit in the CPG.</li> <li>• Changes frequency by software using the Frequency control registers (FRQCR, MCLKCR, and ACLKCR).</li> </ul>
Control the low power mode	Stops clock in sleep mode or software standby mode. Stops the module specified by module standby function.

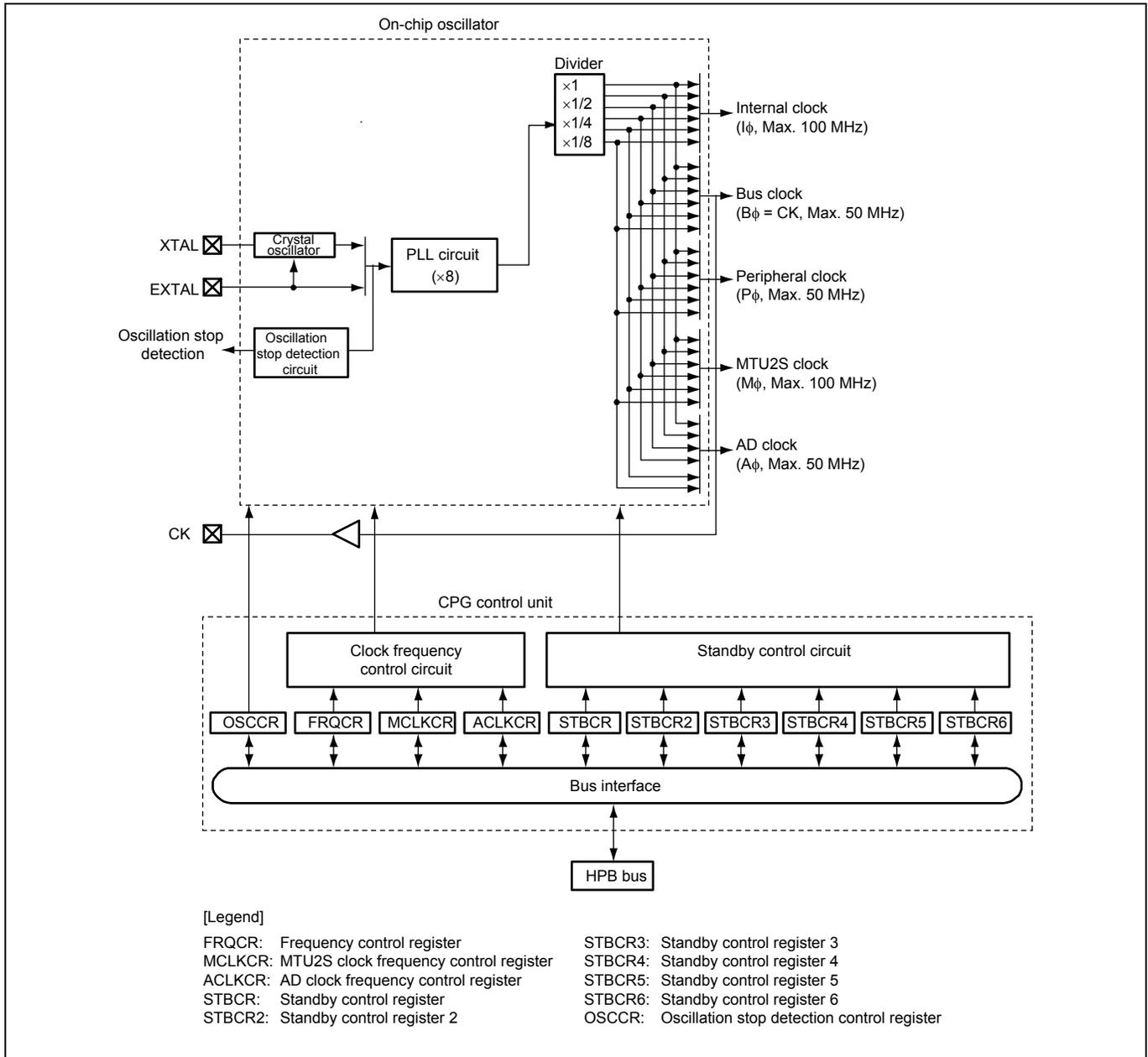


Figure 2 CPG Block Diagram

### 2.3 CPG Setting

The figure below shows the flow chart of setting CPG. Internal peripheral modules are in module standby mode after the reset is canceled. The sample program clears the module standby function for internal peripheral module after setting the Frequency control register (FRQCR), MTU2S clock frequency control register (MCLKCR), and AD clock frequency control register (ACLKCR). For details on these registers, refer to the SH7285 Group Hardware Manual.

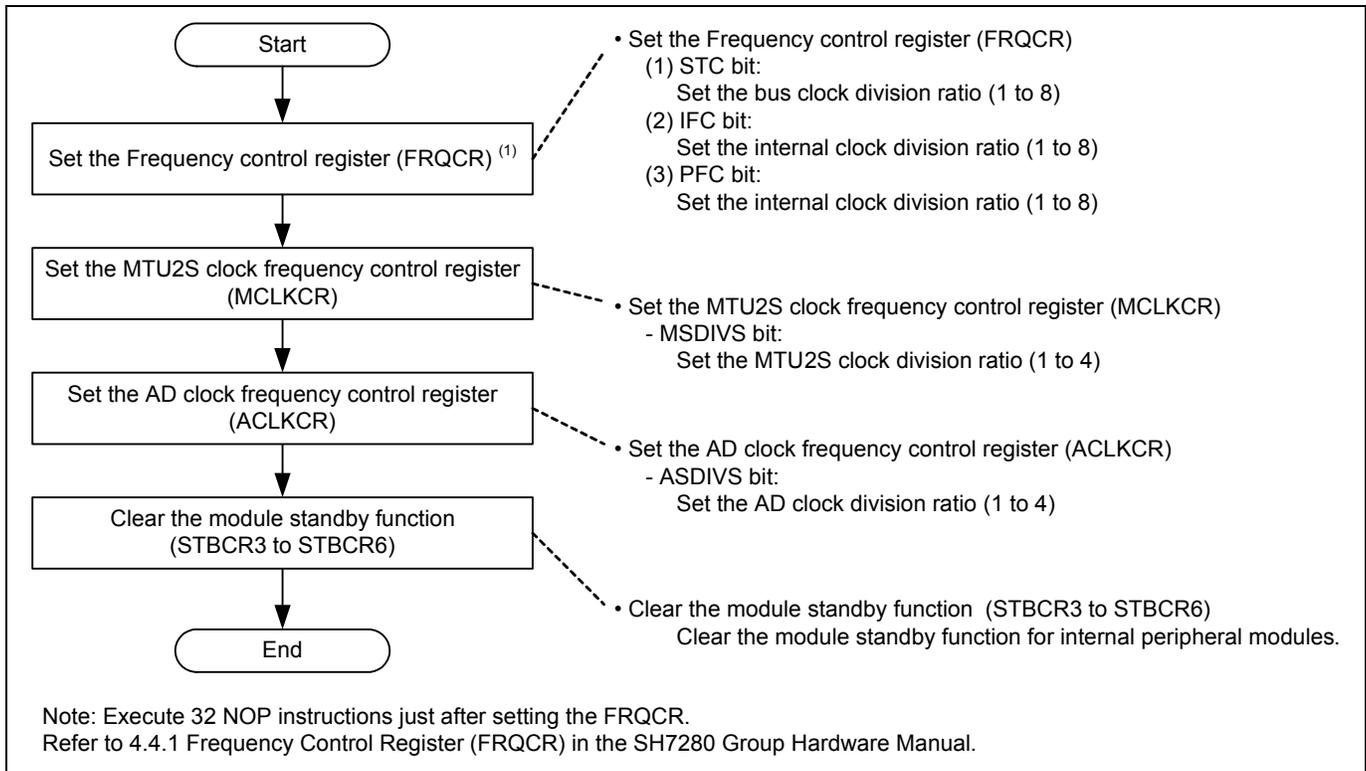


Figure 3 Flow Chart of CPG Setting

## 2.4 Setting in the Sample Program

Table 2 lists the setting in the sample program. Table 3 and

Table 4 list register settings for each module.

**Table 2 Module Setting in the Sample Program**

Module	Setting
Clock pulse generator (CPG)	<ul style="list-style-type: none"> <li>• Clock frequency (input clock is 12.5 MHz) Internal clock: 100 MHz Bus clock: 50 MHz Peripheral clock: 50 MHz MTU2S clock: 50 MHz AD clock: 50 MHz</li> <li>• Modules cleared the module standby function MTU2S, MTU2, POE2, IIC3, ADC0, ADC1, CMT, SCIF3, SCIO, SCI1, SCI2, SCI4, SSU, USB</li> </ul>

**Table 3 CPG Register Settings (1/2)**

Register Name	Address	Setting	Description
Frequency control register (FRQCR)	H'FFFE 0010	H'0101	<ul style="list-style-type: none"> <li>• STC[2:0] = "B'001": Bus clock (B<math>\phi</math>) division ratio: 2</li> <li>• IFC[2:0] = "B'000": Internal clock (I<math>\phi</math>) division ratio: 1</li> <li>• PFC[2:0] = "B'001": Peripheral clock (P<math>\phi</math>) division ratio = 2</li> </ul>
MTU2S clock frequency control register (MCLKCR)	H'FFFE 0410	H'41	<ul style="list-style-type: none"> <li>• MSDIVS[1:0] = "B'01": MTU2S clock (M<math>\phi</math>) division ratio = 2</li> </ul>
AD clock frequency control register (ACLKCR)	H'FFFE 0414	H'41	<ul style="list-style-type: none"> <li>• ASDIVS[1:0] = "B'01": AD clock (A<math>\phi</math>) division ratio = 2</li> </ul>

**Table 4 CPG Register Settings (2/2)**

Register Name	Address	Setting	Description
Standby control register 3 (STBCR3)	H'FFFE 0408	H'02	<ul style="list-style-type: none"> <li>• HIZ = "0": The pin state is held in software standby mode</li> <li>• MSTP36 = "0": MTU2S is operating</li> <li>• MSTP35 = "0": MTU2 is operating</li> <li>• MSTP34 = "0": POE2 is operating</li> <li>• MSTP33 = "0": IIC3 is operating</li> <li>• MSTP32 = "0": ADC0 is operating</li> </ul>
Standby control register 4 (STBCR4)	H'FFFE 040C	H'E2	<ul style="list-style-type: none"> <li>• MSTP44 = "0": SCIF3 is operating</li> <li>• MSTP42 = "0": CMT is operating</li> </ul>
Standby control register 5 (STBCR5)	H'FFFE 0418	H'12	<ul style="list-style-type: none"> <li>• MSTP57 = "0": SCI0 is operating</li> <li>• MSTP56 = "0": SCI1 is operating</li> <li>• MSTP55 = "0": SCI2 is operating</li> <li>• MSTP53 = "0": SCI4 is operating</li> <li>• MSTP52 = "0": ADC1 is operating</li> <li>• MSTP50 = "0": SSU is operating</li> </ul>
Standby control register 6 (STBCR6)	H'FFFE 041C	H'9F	<ul style="list-style-type: none"> <li>• USBSEL = "1": Selects the USB oscillator as the USB clock source</li> <li>• MSTP66 = "0": USB is operating</li> <li>• USBCLK = "0": USB oscillator is operating</li> </ul>

### 3. Sample Program Listing

#### 3.1 Sample Program Listing "resetprg.c" (1/3)

```

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29 *"FILE COMMENT"***** Technical reference data *****
30 *   System Name : SH7285 Sample Program
31 *   File Name   : resetprg.c
32 *   Abstract    : SH7285 Initial Setting
33 *   Version     : 1.00.00
34 *   Device      : SH7285
35 *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.04.01).
36 *               : C/C++ compiler package for the SuperH RISC engine family
37 *               :                               (Ver.9.01 Release01).
38 *   OS          : None
39 *   H/W Platform: M3A-HS85 (CPU board)
40 *   Description :
41 *****/
42 *   History     : Jun.18,2009 Ver.1.00.00
43 *"FILE COMMENT END"*****/
44 #include <machine.h>
45 #include <_h_c_lib.h>
46 #include "stacksct.h"
47 #include "iodefine.h"
48

```

### 3.2 Sample Program Listing "resetprg.c" (2/3)

```

49  /* ==== Macro definition ==== */
50  #define SR_Init      0x000000F0
51  #define INT_OFFSET  0x10
52
53  /* ==== Prototype declaration ==== */
54  void PowerON_Reset_PC(void);
55  void Manual_Reset_PC(void);
56
57  /* ==== External reference declaration ==== */
58  /* ---- Function prototype ---- */
59  extern void HardwareSetup(void);
60  extern void main(void);
61  /* ---- Global variable ---- */
62  extern unsigned int INT_Vectors;
63
64  /* ==== Section name changed to ResetPRG ==== */
65  #pragma section ResetPRG
66
67  /* ==== Entry function specified ==== */
68  #pragma entry PowerON_Reset_PC
69
70  /*"FUNC COMMENT"*****
71  * ID          :
72  * Outline     : CPU initialization
73  *-----
74  * Include     : <machine.h>, <_h_c_lib.h>, and "iodefine.h"
75  *-----
76  * Declaration : void PowerON_Reset_PC(void);
77  *-----
78  * Description : Executes the CPU initialization processing to register
79  *              : the power-on reset vector to the exception vector table.
80  *-----
81  * Argument    : void
82  *-----
83  * Return Value : void
84  *-----
85  * Note        : This function is executed first after power-on reset.
86  *"FUNC COMMENT END"*****
87  void PowerON_Reset_PC(void)
88  {
89      /* ==== Hardware initialization ==== */
90      HardwareSetup();          /* HardwareSetup function */
91
92      /* ==== B and R sections initialization ==== */
93      _INITSCT();
94

```

### 3.3 Sample Program Listing "resetprg.c" (3/3)

```

95     /* ==== Vector Base Register setting ==== */
96     set_vbr((void *)((char *)&INT_Vectors - INT_OFFSET));
97
98     /* ==== Status Register initialization ==== */
99     set_cr(SR_Init);
100    nop();
101
102    /* ==== Bank Number Register setting ==== */
103    INTC.IBNR.BIT.BE = 0x01;          /* Use of register banks enabled for all */
104                                       /* interrupts except NMI and user break */
105
106    /* ==== Interrupt enabling ==== */
107    set_imask(0);                    /* Interrupt mask bits clear */
108
109    /* ==== Main function call ==== */
110    main();
111
112    /* ==== Sleep instruction execution ==== */
113    sleep();
114 }
115
116 // #pragma entry Manual_Reset_PC    /* Remove the comment when you use Manual Reset */
117 /*"FUNC COMMENT"*****
118 * ID          :
119 * Outline     : Manual reset processing
120 *-----
121 * Include     :
122 *-----
123 * Declaration : void Manual_Reset_PC(void);
124 *-----
125 * Description : Registers the manual reset vector to the exception vector table.
126 *-----
127 * Argument    : void
128 *-----
129 * Return Value : void
130 *-----
131 * Note        : This sample does not describe the processing content at all.
132 *              : Add the program in this function as needed.
133 *"FUNC COMMENT END"*****
134 void Manual_Reset_PC(void)
135 {
136     /* NOP */
137 }
138
139 /* END of File */

```

### 3.4 Sample Program Listing "hwsetup.c" (1/2)

```

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29 *"FILE COMMENT"***** Technical reference data *****
30 *   System Name : SH7285 Sample Program
31 *   File Name   : hwsetup.c
32 *   Abstract    : Hardware Function Initial Setting
33 *   Version     : 1.00.00
34 *   Device      : SH7285
35 *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.04.01).
36 *                : C/C++ compiler package for the SuperH RISC engine family
37 *                :                               (Ver.9.01 Release01).
38 *   OS          : None
39 *   H/W Platform: M3A-HS85 (CPU board)
40 *   Description :
41 *****/
42 *   History     : Jun.18,2009 Ver.1.00.00
43 *"FILE COMMENT END"*****/
44 #include "iodefine.h"
45
46 /* ==== Prototype declaration ==== */
47 void HardwareSetup(void);
48

```

### 3.5 Sample Program Listing "hwsetup.c" (2/2)

```

49  /* ==== External reference ==== */
50  /* ---- Function prototype ---- */
51  extern void io_set_cpg(void);
52
53  /*"FUNC COMMENT"*****
54  * ID          :
55  * Outline     : Hardware initialization
56  *-----
57  * Include     :
58  *-----
59  * Declaration : void HardwareSetup(void);
60  *-----
61  * Description : Initializes the hardware function.
62  *-----
63  * Argument    : void
64  *-----
65  * Return Value : void
66  *-----
67  * Note        : None
68  *"FUNC COMMENT END"*****/
69  void HardwareSetup(void)
70  {
71      /* ==== CPG setting ==== */
72      io_set_cpg();
73  }
74
75  /* End of File */

```

### 3.6 Sample Program Listing "cpg.c" (1/2)

```

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28 *   Copyright (C) 2009. Renesas Technology Corp., All Rights Reserved.
29 *   "FILE COMMENT"***** Technical reference data *****
30 *   System Name : SH7285 Sample Program
31 *   File Name   : cpg.c
32 *   Abstract    : CPG Setting Processing
33 *   Version     : 1.00.00
34 *   Device      : SH7285
35 *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.04.01).
36 *               : C/C++ compiler package for the SuperH RISC engine family
37 *               :                               (Ver.9.01 Release01).
38 *   OS          : None
39 *   H/W Platform: M3A-HS85 (CPU board)
40 *   Description :
41 *****/
42 *   History     : Jun.18,2009 Ver.1.00.00
43 *   "FILE COMMENT END"*****/
44 #include <machine.h>
45 #include "iodefine.h"
46
47 /* ==== Prototype declaration ==== */
48 void io_set_cpg(void);
49

```

### 3.7 Sample Program Listing "cpg.c" (2/2)

```

50  /*"FUNC COMMENT"*****
51  * ID          :
52  * Outline     : CPG setting
53  *-----
54  * Include     : <machine.h> and "iodefine.h"
55  *-----
56  * Declaration : void io_set_cpg(void);
57  *-----
58  * Description : Initializes the clock pulse generator (CPG) as follows:
59  *             : I-clock = 100MHz, B-clock = 50MHz, P-clock = 50MHz,
60  *             : M-clock = 50MHz, and A-clock = 50MHz.
61  *             : And then supplies clock to all peripheral modules.
62  *-----
63  * Argument    : void
64  *-----
65  * Return Value : void
66  *-----
67  * Note        : This function is an example of CPG setting at the input clock
68  *             : of 12.5MHz.
69  *"FUNC COMMENT END"*****/
70  void io_set_cpg(void)
71  {
72      /* ==== CPG setting ==== */
73      CPG.FRQCR.WORD = 0x0101;          /* Clock-in = 12.5MHz */
74                                      /* I-clock = 100MHz */
75                                      /* B-clock = 50MHz */
76                                      /* P-clock = 50MHz */
77
78      nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
79      nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
80      nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
81      nop(); nop(); nop(); nop(); nop(); nop(); nop(); nop();
82
83      CPG.MCLKCR.BYTE = 0x41;          /* M-clock = 50MHz */
84      CPG.ACLKCR.BYTE = 0x41;          /* A-clock = 50MHz */
85
86
87      /* ==== Module Stanby Clear ==== */
88      STB.CR3.BYTE = 0x02;             /* HIZ, MTU2S, MTU2, POE2, */
89                                      /* IIC3, ADC0, Reserve(1), Reserve(0) */
90
91      STB.CR4.BYTE = 0xe2;             /* Reserve(1), Reserve(1), Reserve(1), SCIF3, */
92                                      /* Reserve(0), CMT, Reserve(1), Reserve(0) */
93
94      STB.CR5.BYTE = 0x12;             /* SCI0, SCI1, SCI2, Reserve(1), */
95                                      /* SCI4, ADC1, Reserve(1), SSU */
96
97      STB.CR6.BYTE = 0x9f;             /* USB: Using USBXTAL/USBEXTAL for USBCLK. */
98  }
99
100 /* End of File */
    
```

### 3.8 Sample Program Listing "vecttbl.c" (1/2)

```

1  /*****
2  *   DISCLAIMER
3  *
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26 *   http://www.renesas.com/disclaimer
27 *****/
28 *   Copyright (C) 2009. Renesas Technology Corp., All Rights Reserved.
29 *"FILE COMMENT"***** Technical reference data *****
30 *   System Name : SH7285 Sample Program
31 *   File Name   : vecttbl.c
32 *   Abstract    : Initialization for Vector Table
33 *   Version     : 1.00.00
34 *   Device      : SH7285
35 *   Tool-Chain  : High-performance Embedded Workshop (Ver.4.04.01).
36 *                : C/C++ compiler package for the SuperH RISC engine family
37 *                :                               (Ver.9.01 Release01).
38 *   OS          : None
39 *   H/W Platform: M3A-HS85 (CPU board)
40 *   Description :
41 *****/
42 *   History     : Jun.18,2009 Ver.1.00.00
43 *"FILE COMMENT END"*****/
44 #include "vect.h"
45
46 #pragma section VECTTBL
47 void *RESET_Vectors[] = {
48 // <<VECTOR DATA START (POWER ON RESET)>>
49 // 0 Power On Reset PC
50     (void *)PowerON_Reset_PC,

```

### 3.9 Sample Program Listing "vecttbl.c" (2/2)

```

51 // <<VECTOR DATA END (POWER ON RESET)>>
52 // 1 Power On Reset SP
53     __secend("S"),
54 // <<VECTOR DATA START (MANUAL RESET)>>
55 // 2 Manual Reset PC
56     (void *)Manual_Reset_PC,
57 // <<VECTOR DATA END (MANUAL RESET)>>
58 // 3 Manual Reset SP
59     __secend("S")
60 };
61
62 #pragma section INTTBL
63 void *INT_Vectors[] = {
64 // 4 Illegal code
65     (void *)INT_Illegal_code,
66
67 ...
68
69
70
71
72 // 255 SCIF SCIF3 TXI3
73     (void *)INT_SCIF_SCIF3_TXI3,
74 // xx Reserved
75     (void *)Dummy
76 };
77
78 /* End of File */

```

#### 4. References

- Software Manual  
SH-1/SH2/SH-DSP Software Manual Rev. 7.00  
(Download the latest version from the Renesas website.)
- Hardware Manual  
SH7280 Group Hardware Manual Rev. 2.00  
(Download the latest version from the Renesas website.)

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## Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Jun 30, 2009	—	First edition issued

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