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SH7763 Group

Example of DDR-SDRAM Interface Connection

Introduction

This application note provides an application example of setting items necessary for the DDR-SDRAM interface (DDRIF) of the SH7763.

Target Device

SH7763

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1. Preface

1.1 Specifications

Two 512-Mbit DDR-SDRAMs (32 M × 16 bits) are connected in parallel in area 2 and 3. The DDR-SDRAM interface's initial settings for 32-bit use are specified.

1.2 Modules Used

- DDR-SDRAM interface (DDRIF)

1.3 Applicable Conditions

- Evaluation board: SH7763 Solution Engine (type no.: MS7763SE02) from Hitachi ULSI Systems Co., Ltd.
(area 2, 3): 128-MB DDR-SDRAM (64 MB × 2):
MT46V32M16TG-6T from Micron
- MCU: SH7763 (R5S77631AY266BGV)
- Operating frequency:

CPU clock:	266.66 MHz
SuperHyway bus clock:	133.33 MHz
Bus clock:	66.66 MHz
DDR-SDRAM clock:	133.33 MHz
Peripheral bus clock 0:	66.66 MHz
Peripheral bus clock 1:	33.33 MHz
- Clock operating mode: Mode 0 (with the MD0 to MD2 pin at the low level)
- Endian: Big endian (with the MD5 pin at the low level)
- Toolchain: SuperH RISC engine Standard Toolchain Ver.9.3.0.0 from Renesas Technology
- Compiler options: Default settings of High-performance Embedded Workshop

```
(-cpu=sh4a -include="$(PROJDIR)¥inc"
-object="$(CONFIGDIR)¥$(FILELEAF).obj" -debug -gbr=auto -chgincpath
-errorpath -global_volatile=0 -opt_range=all -infinite_loop=0
-del_vacant_loop=0 -struct_alloc=1 -nologo)
```

1.4 Related Application Note

The operation of the reference program for this document was confirmed with the setting conditions described in the *SH7763 Group Application Note: SH7763 Example of Initialization* (REJ06B0934). Please refer to that document in combination with this one.

2. Description of Sample Application

2.1 Operational Overview of Module Used

- The DDR-SDRAM interface can connect DDR-SDRAMs by arbitrating access from the CPU and modules and by outputting control signals to the DDR-SDRAMs.
- 32-bit data bus configuration, DDR266 (133 MHz) and DDR200 (100 MHz), and a burst length of 2 are supported. The DDRIF only supports a SHwy-to-external-memory clock ratio of 1:1. The maximum operating frequency of the SHwy clock is 133 MHz, but its minimum operating frequency depends on the clock frequency of the DDR-SDRAM to be used. Therefore, refer to the data sheet of the DDR-SDRAM.
- The available memory capacities and configurations are as follows. Addresses must be multiplexed according to the settings of the BW bit in the MIM register and the SPLIT bit in the SDRA register, so that DDR-SDRAMs can be connected without external address multiplexers. For details on the settings concerned, refer to *SH7763 Group Hardware Manual* (REJ09B0256).
 - Parallel connection of two 128-Mbit DDRs (8 M × 16)
 - Parallel connection of two 256-Mbit DDRs (16 M × 16)
 - Parallel connection of two 512-Mbit DDRs (32 M × 16)
 - Parallel connection of two 1-Gbit DDRs (64 M × 16)

2.2 Overview of Setting Example

Table 1 provides the specifications of DDR-SDRAM used in this sample application.

Table 1 Specifications of DDR-SDRAM Used in this Sample Application

Item	Description
Type number	MT46V32M16TG-6T from Micron
Capacity (configuration)	512 Mbits (32 M × 16 bits)
Number of units used	2
CAS latency	2.5
Refresh cycles	Refresh cycles: 64 ms, average refresh time: 7.8125 μs
Burst length	2, 4, or 8 (programmable)
Row address	A0 to A12
Column address	A0 to A9
Precharge	Auto precharge/all bank precharge controlled via A10

Figure 1 shows a memory map in this sample setting.

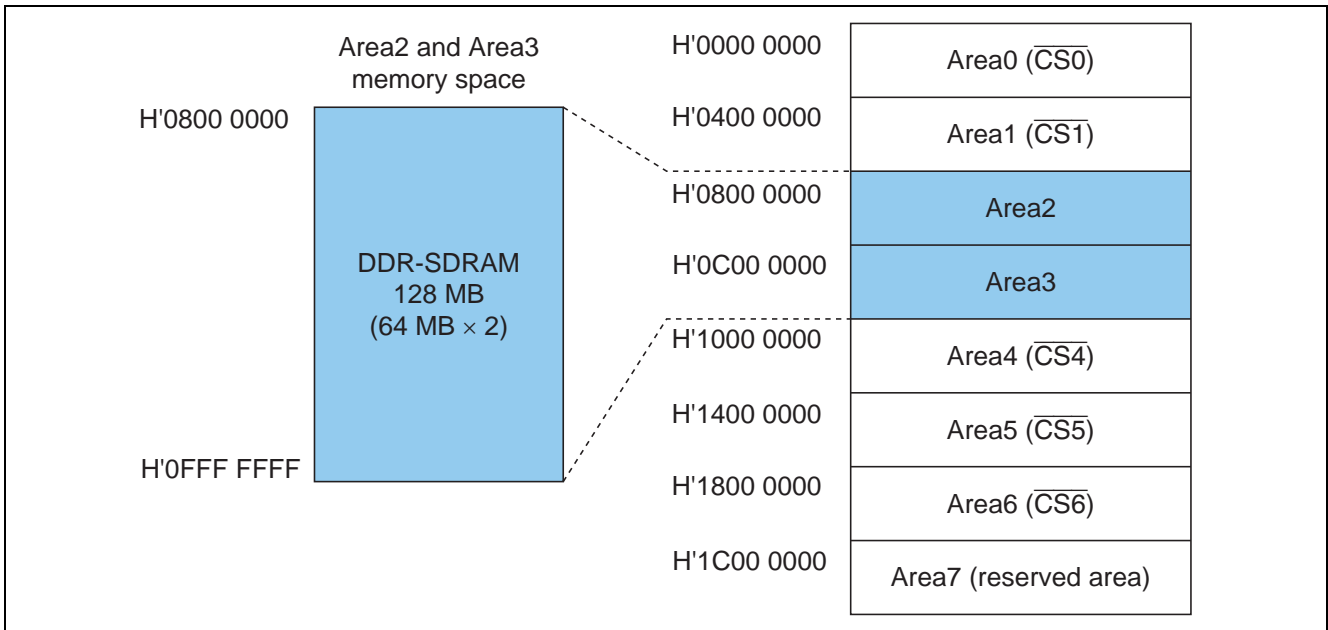


Figure 1 Memory Map

Figure 2 shows a conceptual diagram of connection between the SH7763 and the two parallel-connected 512-Mbit DDR-SDRAMs (32 M × 16 bits) to be used in this setting example. This diagram does not provide details on how to actually implement DDR-SDRAMs in pattern design. All such details must be fully worked out in design process.

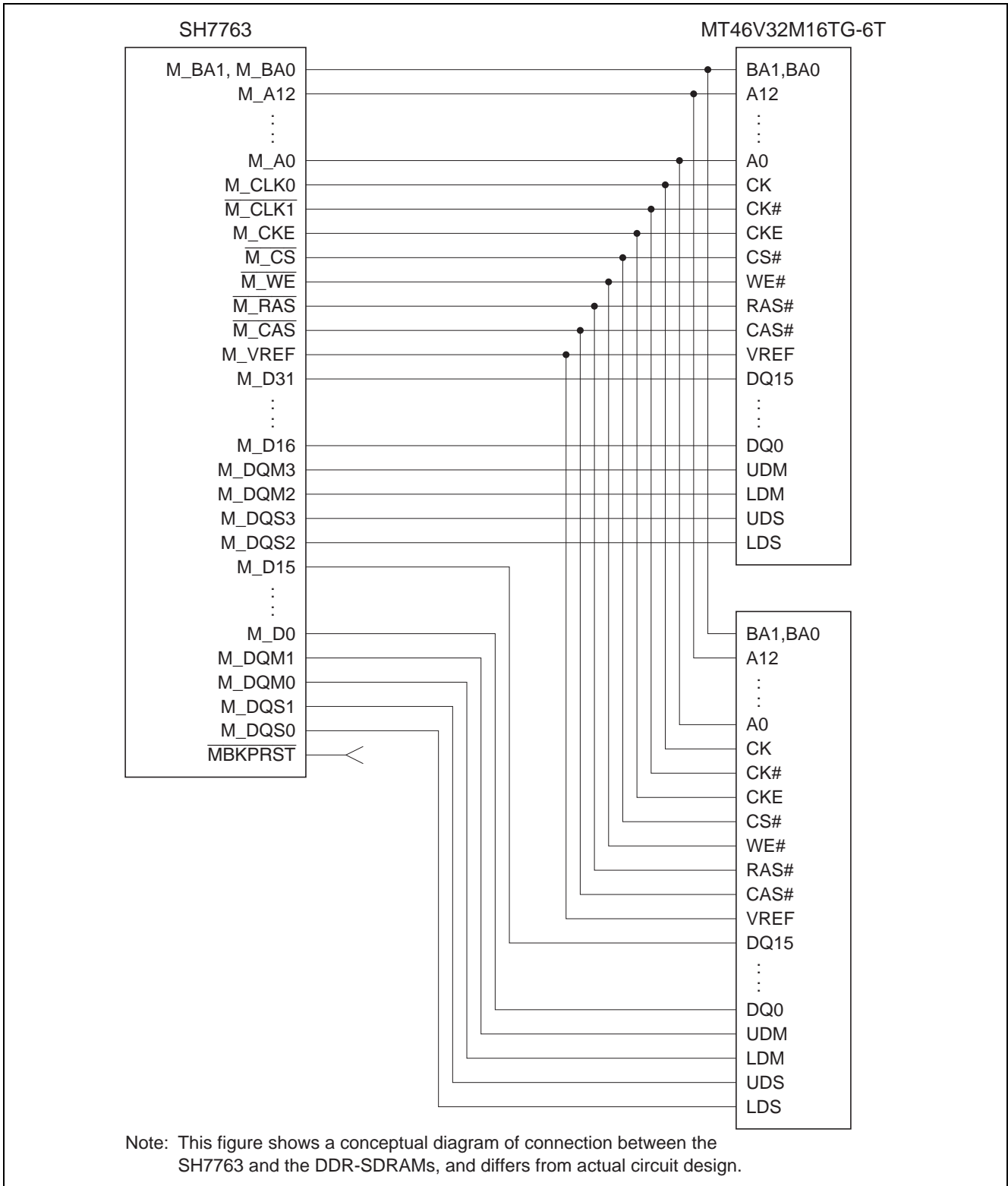


Figure 2 Conceptual Diagram of Connecting Two 512-Mbit DDR-SDRAMs in Parallel (32 M × 16 bits)

Figure 3 shows the sample program sequence.

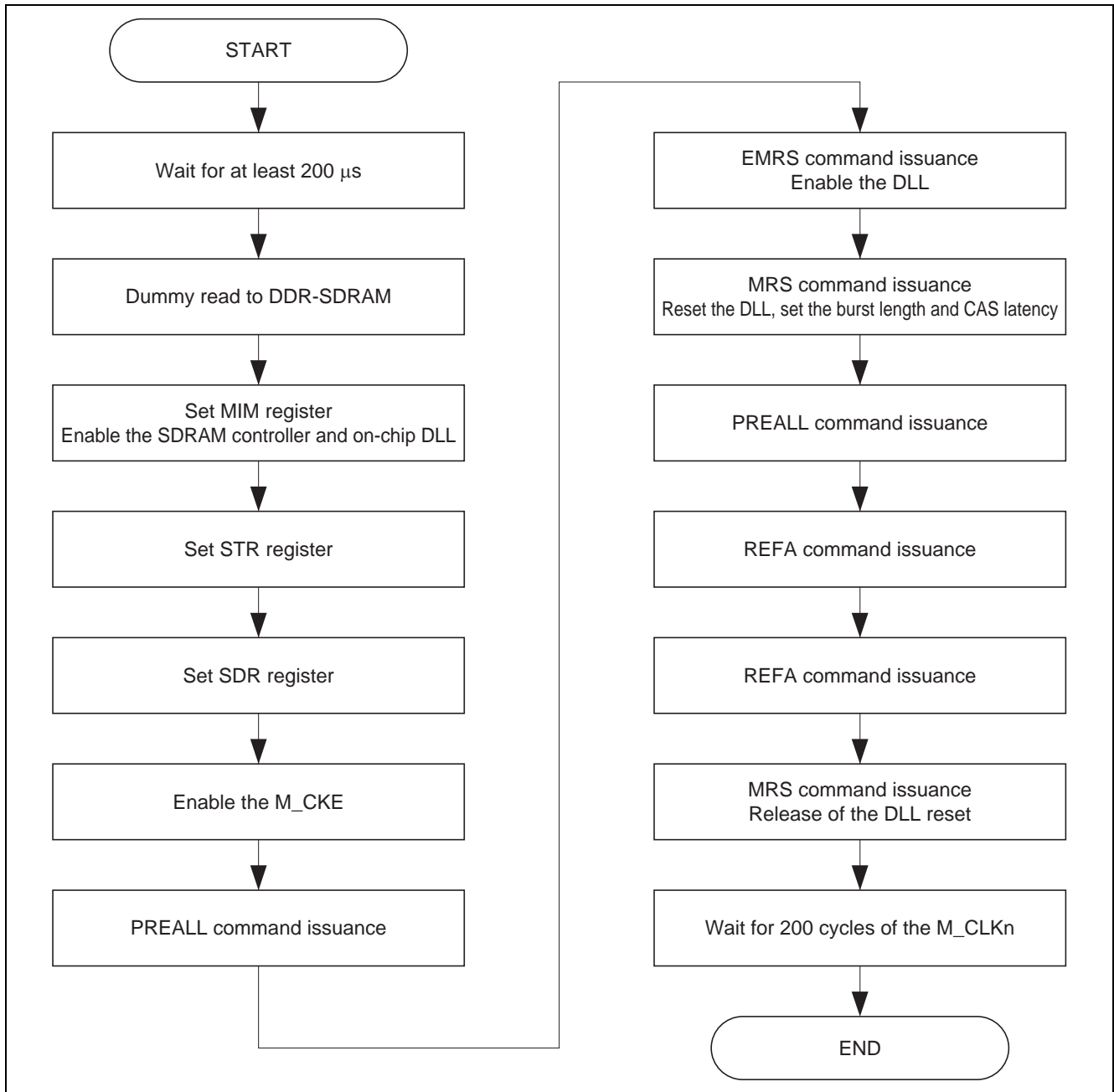


Figure 3 DDR-SDRAM Initialization Sequence

Table 2 shows examples of settings for the DDR-SDRAM interface registers in this setting example. For details on individual registers, please refer to the section on the DDR-SDRAM interface (DDRIF) in the *SH7763 Group hardware manual* (REJ09B0256).

Table 2 Example of Settings for the DDR-SDRAM Interface Registers

Name of Register	Address	Setting Value	Description
Memory interface mode register (MIM)	H'FE80 0008	H'0000 0000	[63-32bit] <ul style="list-style-type: none"> Retains the initial value
	H'FE80 000C	H'02EE 0309	[31-0bit] <ul style="list-style-type: none"> Maximum refresh intervals DRI[12:0] = "H'2EE": $7.5 \text{ ns} \times 750 = 5.6 \mu\text{s} < 7.8 \mu\text{s}$ Refresh DRE = "B'1": Valid DLL enable DLLEN = "B'1": Enable DDR controller enable DCE = "B'1": Enable
DDR-SDRAM control register (SCR)	H'FE80 0014	H'0000 0001	[31-0bit] <ul style="list-style-type: none"> DDR-SDRAM mode select
		H'0000 0002	SMS[2:0] = "B'001": NOP command
		H'0000 0003	SMS[2:0] = "B'010": PREALL command
		H'0000 0004	SMS[2:0] = "B'011": M_CKE enable SMS[2:0] = "B'100": REFA command
DDR-SDRAM timing register (STR)	H'FE80 001C	H'0005 0040	[31-0bit] <ul style="list-style-type: none"> Minimum number of cycles from write command to read commands WR[1:0] = "B'01": 4 cycles Minimum number of cycles from read command to write commands RW[1:0] = "B'01": 4 cycles Number of cycles in same bank SRFC[2:0] = "B'000": 11 cycles PRE/PREALL command issuance cycle SWR = "B'0": 2 cycles ACT command issuance cycle between banks SRRD = "B'0": 2 cycles Minimum number of cycles between ACT and PRE commands SRAS[2:0] = "B'000": 6 cycles Auto-refresh/ACT command issuance cycle SRC[2:0] = "B'010": 8 cycles CAS latency (CL) SCL[2:0] = "B'000": 2.5 cycles Number of cycles between RAS and CAS commands SRCD = "B'0": 3 cycles Number of cycles between PRE and ACT commands SRP = "B'0": 3 cycles
DDR-SDRAM row attribute register (SDR)	H'FE80 0034	H'0000 0400	[31-0bit] <ul style="list-style-type: none"> DDR-SDRAM memory configuration SPLIT[3:0] = "B0100": $32 \text{ M} \times 16 \text{ bits}$ product

Note: * The initial settings of registers other than those listed above are retained in this setting example.

2.3 Notes on Powering On

It is recommended that when the VCCQ_DDR (the DDR-SDRAM interface power supply) is powered on, the M_CKE output be fixed to the low level by inputting a low level to the M_BKPRST of the SH7763, in the same way as the DDR-SDRAM power supply backup sequence described in section 18.7 *DDR-SDRAM Power Supply Backup of SH7763 Group Hardware Manual* (REJ09B0256).

This is because it is necessary to prevent contention on the data buses of both the SH7763 and the DDR-SDRAMs. (Refer to RENESAS TECHNICAL UPDATE TN-SH7-A618A/J.)

2.4 Notes on Capacity of DDR-SDRAM to be Connected to SH7763 and Memory Area Setting

The location of the DDR-SDRAMs in memory area is determined by setting the AREASEL bits in the memory address map select register (MMSELR) of the Local Bus State Controller (LBSC).

Also, the configuration of the DDR-SDRAMs to be connected is determined by setting the SPLIT bits in the DDR-SDRAM low attribute register (SDR) of the DDRIF.

Note that when the SPLIT bits are set, the capacity of the DDR-SDRAMs must not exceed the size of the memory area specified by the AREASEL bits.

3. Listing of the Sample Program

3.1 Sample Program Listing: "vhandler.src"(1)

```

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26 ;* http://www.renesas.com/disclaimer
27 ;*****/
28 ;/* Copyright (C) 2009. Renesas Technology Corp., All Rights Reserved.      */
29 ;/"FILE COMMENT"***** Technical reference data *****/
30 ;* System Name   : SH7763 Sample Program
31 ;* File Name    : vhandler.src
32 ;* Abstract     : Sample Program for the SH7763 Initial Setting
33 ;* Version      : Ver 1.00
34 ;* Device       : SH7763
35 ;* Tool-Chain   : High-performance Embedded Workshop (Version 4.05.01.001)
36 ;*              : C/C++ Compiler Package for SuperH Family (V.9.03 release00)
37 ;* OS           : None
38 ;* H/W Platform : MS7763SE02
39 ;* Description  : Sample Program for Setting the SH7763 Initialization
40 ;*              :
41 ;* Operation    :
42 ;* Limitation   :
43 ;*              :
44 ;*****
45 ;* History      : 28.July.2009 Ver. 1.00 First Release
46 ;/"FILE COMMENT END"*****/
47
...Omitted

```

3.2 Sample Program Listing: "vhandler.src"(2)

```

48  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
49  ;   DDRIF_INIT                                     ;
50  ;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;;
51  DDRIF_INIT:
52          mov.l   #H'00007000,r0
53  LOOP1:
54          dt     r0
55          bf     LOOP1           ;200µs wait
56          nop
57          nop
58  ;
59          mov.l   #H'A8000000,r0           ;set dummy read access
60          mov.l   @r0,r1
61  ;
62          mov.l   #H'FE80000C,r0           ;set MIM(31-0bit) address
63          mov.l   #H'02EE0109,r1           ;DRAM refresh disable,DLL enable,DDRIF enable
64          mov.l   r1,@r0
65  ;
66          mov.l   #H'02EE0309,r1           ;Refresh enable
67          mov.l   r1,@r0
68  ;
69          mov.l   #H'FE80001C,r0           ;set STR(31-0bit) address
70          mov.l   #H'00050040,r1
71          mov.l   r1,@r0
72  ;
73          mov.l   #H'FE800034,r2           ;set SDR(31-0bit) address
74          mov.l   #H'00000400,r1           ;32Mx16bit
75          mov.l   r1,@r2
76  ;
77          mov.l   #H'FE800014,r2           ;set SCR(31-0bit) address
78          mov.l   #H'00000003,r1           ;SCR M_CKE enable
79          mov.l   r1,@r2
80          mov.l   #H'00000001,r1           ;SCR NOP
81          mov.l   r1,@r2
82          mov.l   #H'00000002,r1           ;SCR PREALL
83          mov.l   r1,@r2
84  ;
85          mov.l   #H'FE902000,r3           ;EMRS DLL enable
86          mov.l   #H'00000000,r4
87          mov.l   r4,@r3
88  ;
89          mov.l   #H'00000001,r1           ;SCR NOP
90          mov.l   r1,@r2
91  ;
92          mov.l   #H'FE900B08,r3           ;MRS DLL reset,CAS Latency=2.5,burstlength=2
93          mov.l   r4,@r3
94  ;
95          mov.l   #H'00000001,r1           ;SCR NOP
96          mov.l   r1,@r2
97          mov.l   #H'00000002,r1           ;SCR PREALL

```

3.3 Sample Program Listing: "vhandler.src"(3)

```

98         mov.l   r1,@r2
99         mov.l   #H'00000001,r1           ;SCR NOP
100        mov.l   r1,@r2
101        mov.l   #H'00000004,r1           ;SCR REFA
102        mov.l   r1,@r2
103        mov.l   #H'00000001,r1           ;SCR NOP
104        mov.l   r1,@r2
105        mov.l   #H'00000004,r1           ;SCR REFA
106        mov.l   r1,@r2
107        ;
108        mov.l   #H'FE900308,r3           ;MRS Reset Cancel
109        mov.l   r4,@r3
110        ;
111        mov.l   #H'00001000,r0
112 LOOP2:
113        dt      r0
114        bf      LOOP2                    ;more then 200 MCLK wait
115        nop
116        nop
117        ;
118        mov.l   #DDRIF_INIT_END,r0
119        jmp     @r0
120        nop
121        ;
122        .pool
123        ;
...Omitted

```

4. Documents for Reference

- Software Manual
SH-4A Software Manual (REJ09B0003)
(The most up-to-date versions of the documents are available on the Renesas Technology Website.)
- Hardware Manual
SH7763 Group Hardware Manual (REJ09B0256)
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