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M16C/64 Group

Example application for timer pulse output when Timer A is insufficient

1. Abstract

This document describes the procedure and example usage for performing timer output using timer B and DMAC when timer A is insufficient to produce the timer output.

2. Introduction

This application note is applied to the M16C/64 group microcomputers.

This program can be operated under the condition of M16C family products with the same SFR (Special Function Register) as M16C/64 Group products. Because some functions may be modified of the M16C family products, see the user's manual. When using the functions shown in this application note, evaluate them carefully for an operation.

3. Specification

The following shows an example of how to use timer B and the DMAC in the M16C/64 group to produce timer pulse output.

- System

XIN = 16MHz, VCC1 = VCC2 = 5V

- DMAC

DMA request factor = TB0 interrupt request, transfer mode = repeat transfer, transfer unit = 8 bit, source address direction = forward (pulse output data), destination address direction = fix (port P0)

- TB0

timer mode, count source = fTIMAB, timer period = 1ms (timer value = 16000 - 1)

4. Operation

The output level of P0_0 functioning as an output port in DMA transfer is changed each time timer B0 underflows in 1 ms cycle. Figure 1 shows timing chart.

Figure 1 shows timing chart.

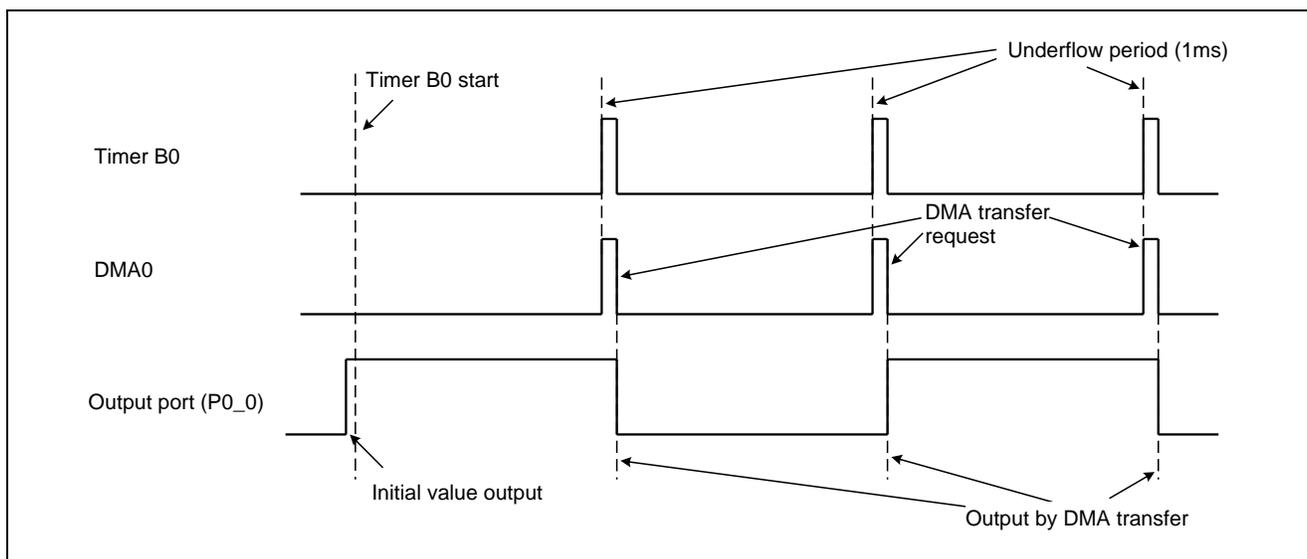


Figure 1. Pulse output timing chart

Note that for reasons of SFR bit assignments, operation in this sample program may involve manipulating some bits whose functions are unused. Make sure the values of these bits are set according to the working condition in the user system.

5. Set-up procedure

Table 1 shows Timer B count source, Figure 2 shows block diagram of Timer B count source in timer mode.

Table 1. Count Source Selection of Timer B

TBCSj register (Note 1)				TBiMR register		Count source	Count source period
TCS3/ TCS7	TCS2/ TCS6	TCS1/ TCS5	TCS0/ TCS4	TCK1	TCK0		f(PLL):24MHz f(XcIN):32.768kHz
0	-	-	-	0	0	f1TIMAB/f2TIMAB (Note 2)	41.7ns or 83.3ns
0	-	-	-	0	1	f8TIMAB	333.3ns
0	-	-	-	1	0	f32TIMAB	1333.3ns
0	-	-	-	1	1	fc32	976.56µs
1	0	0	0	-	-	f1TIMAB/f2TIMAB (Note 2)	41.7ns or 83.3ns
1	0	0	1	-	-	f8TIMAB	333.3ns
1	0	1	0	-	-	f32TIMAB	1333.3ns
1	0	1	1	-	-	f64TIMAB	2666.7ns
1	1	0	1	-	-	foco-s	About 8µs
1	1	1	0	-	-	fc32	976.56µs

Note 1: TCS3~TCS0 bits of TBCS0 register correspond to Timer B0 count source selection, TCS7~TCS4 bits of TBCS0 register correspond to Timer B1 count source selection, TCS3~TCS0 bits of TBCS1 register correspond to Timer B2 count source selection, TCS3~TCS0 bits of TBCS2 register correspond to Timer B3 count source selection, TCS7~TCS4 bits of TBCS2 register correspond to Timer B4 count source selection, and TCS3~TCS0 bits of TBCS3 register correspond to Timer B4 count source selection.

Note 2: When the PCLK0 bit in the PCLKR register is “1”, the selected clock source is f1TIMAB. When the PCLK0 bit is “0”, the selected clock source is f2TIMAB.

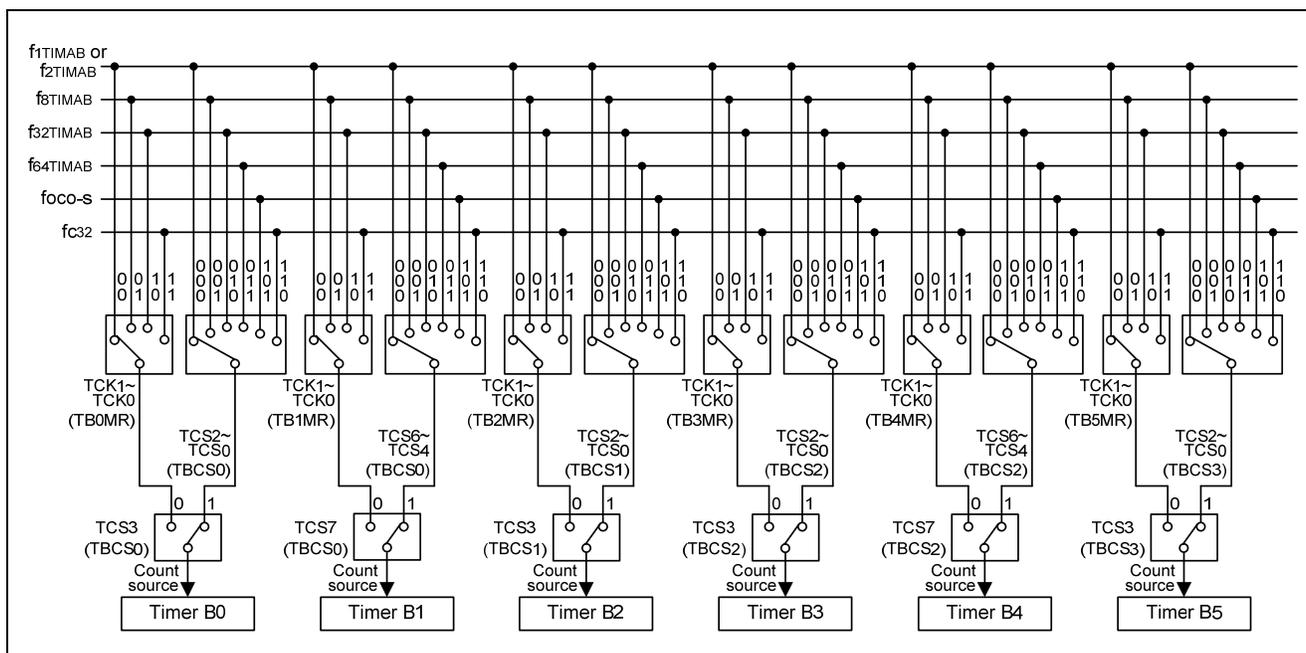
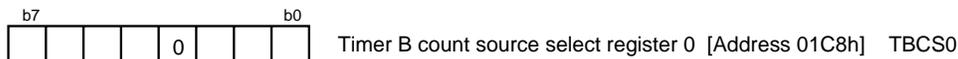


Figure 2. Count source of Timer B

(1) Timer B0 Setting

Select timer count source



TB0 count source select bit (Note1)

b2 b1 b0

0 0 0 : f1TIMAB or f2TIMAB (Note2)

0 0 1 : f8TIMAB

0 1 0 : f32TIMAB

0 1 1 : f64TIMSB

1 0 0 : Do not set

1 0 1 : foco-s

1 1 0 : fc32

1 1 1 : Do not set

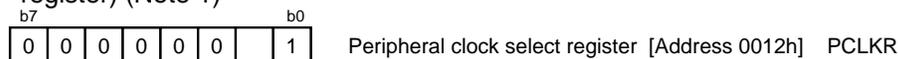
TB0 count source option specified bit (Note1)

0 : TCK0, TCK1 enabled, TCS0 to TCS2 disabled

Note 1: About the count source period, please refer to Table 2.

Note 2: When the PCLK0 bit in the PCLKR register is "1", the selected clock source is f1TIMAB. When the PCLK0 bit is "0", the selected clock source is f2TIMAB.

Select f1TIMAB for the timer A and B clocks using the PCLKR register (peripheral clock select register) (Note 1)



Timer A, B clock select bit

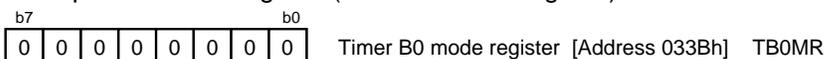
1 : f1TIMAB

Reserved bit

Set to "0"

Note 1: Write to this register after setting the PRC0 bit in the PRCR register to "1" (write enable).

Set up the TB0MR register (timer B0 mode register)



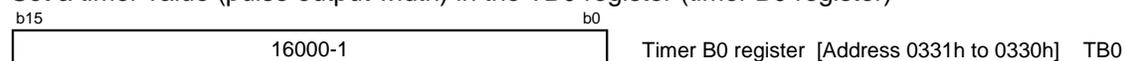
Operation mode select bit

0 0 : Timer mode

Count source select bit

0 0 : f1TIMAB or f2TIMAB

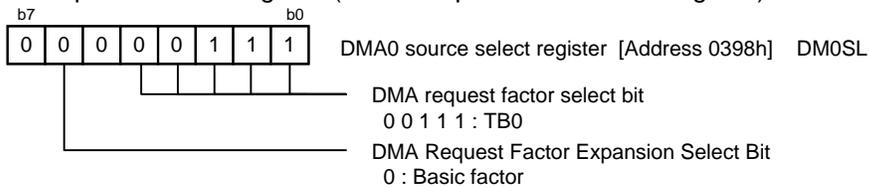
Set a timer value (pulse output width) in the TB0 register (timer B0 register)



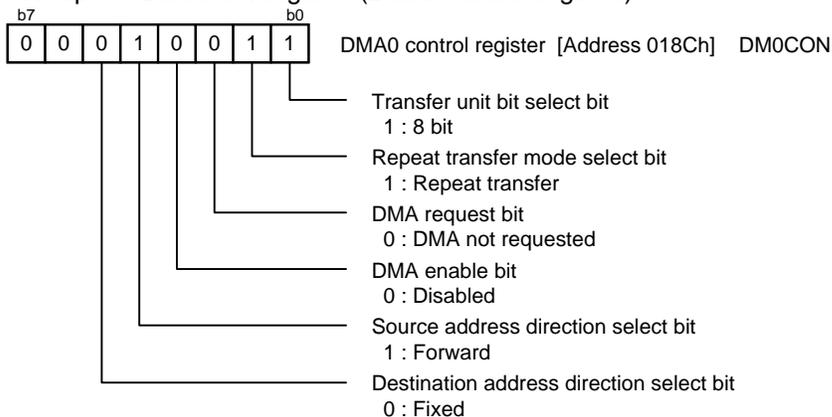
Value for the case where count source = f1TIMAB, f (XIN) = 16 MHz, and pulse is output in 1 ms width.

(2) DMAC Setting

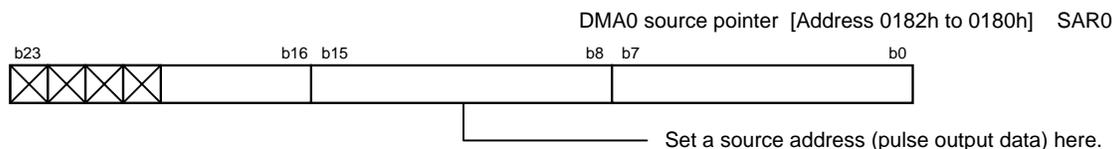
Set up the DM0SL register (DMA0 request factor select register)



Set up the DM0CON register (DMA0 control register)



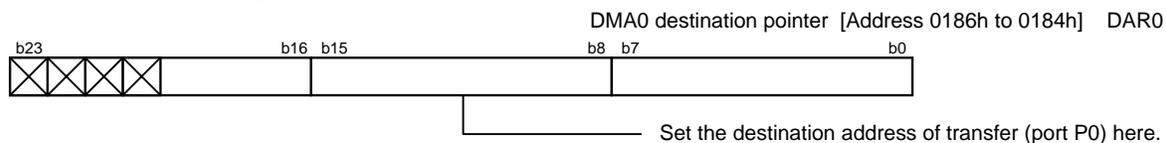
Set up the SAR0 register (DMA0 source pointer)



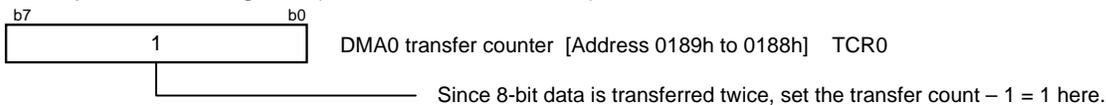
Set the data for pulse output as shown below.

- If initial output = low
char pulse_data[2] = {0x00, 0x01};
- If initial output = high
char pulse_data[2] = {0x01, 0x00};

Set up the DAR0 register (DMA0 destination pointer)

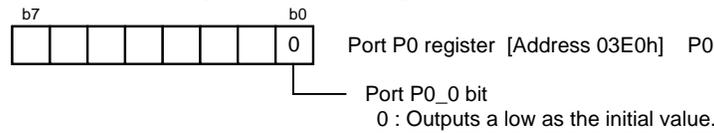


Set up the TCR0 register (DMA0 transfer counter)

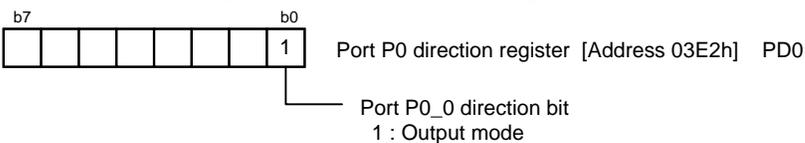


⋮
(3) Set the port P0_0 as an output port for pulse output

Set up the P0 register (port P0 register)

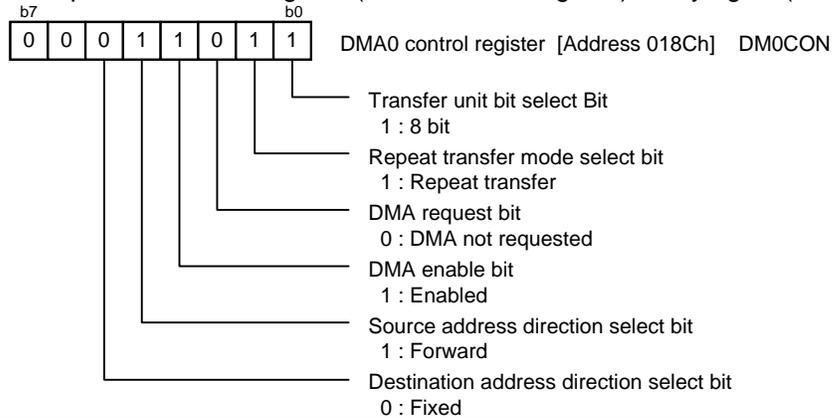


⋮
Set up the PD0 register (port P0 direction register)



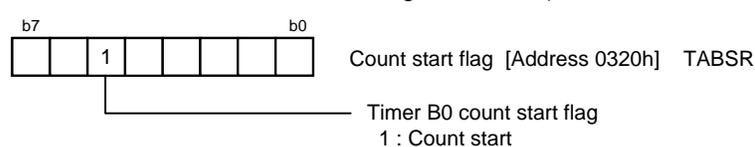
⋮
(4) DMA Enable

Set up the DM0CON register (DMA0 control register) newly again (to enable DMA)



⋮
(5) Timer B0 Start

Set the TB0S bit in the TABSR register to "1" (to let the timer start counting)



6. Precaution

When using timer B and the DMAC in combination to produce timer pulse output, pay attention to the following.

(1) Limitations Due to DMAC Specifications

For reasons of DMAC specifications, the following limitations apply.

- If a DMA request occurs in other interrupt sequence processing, DMA transfer is kept waiting.
- If DMA0 and DMA1 requests occur at the same time, DMA0 is serviced first because it has higher priority and DMA1 is kept waiting.

Therefore, the procedure presented here cannot be used for short-cycle, high-accuracy applications. For such applications, we recommend using timer A preferentially over the other timer.

(2) Pulse Output Delay

- Delay time at start of timer B

For pulse output produced first at start of timer B, the instruction execution time from when the port direction register is set for output to when timer B is made to start constitutes a delay time.

- Delay Time Due to DMA Transfer

Pulse output actually is produced a finite time after a timer B interrupt request occurred, which is equal to the DMA setup time + number of DMA transfer cycles (see “(3) DMA Transfer Cycles” in “6 Precaution”). This delay time can be adjusted by adjusting the timer value.

Figure 3 shows an example of pulse output delay when the same timer value is set in timers A and B.

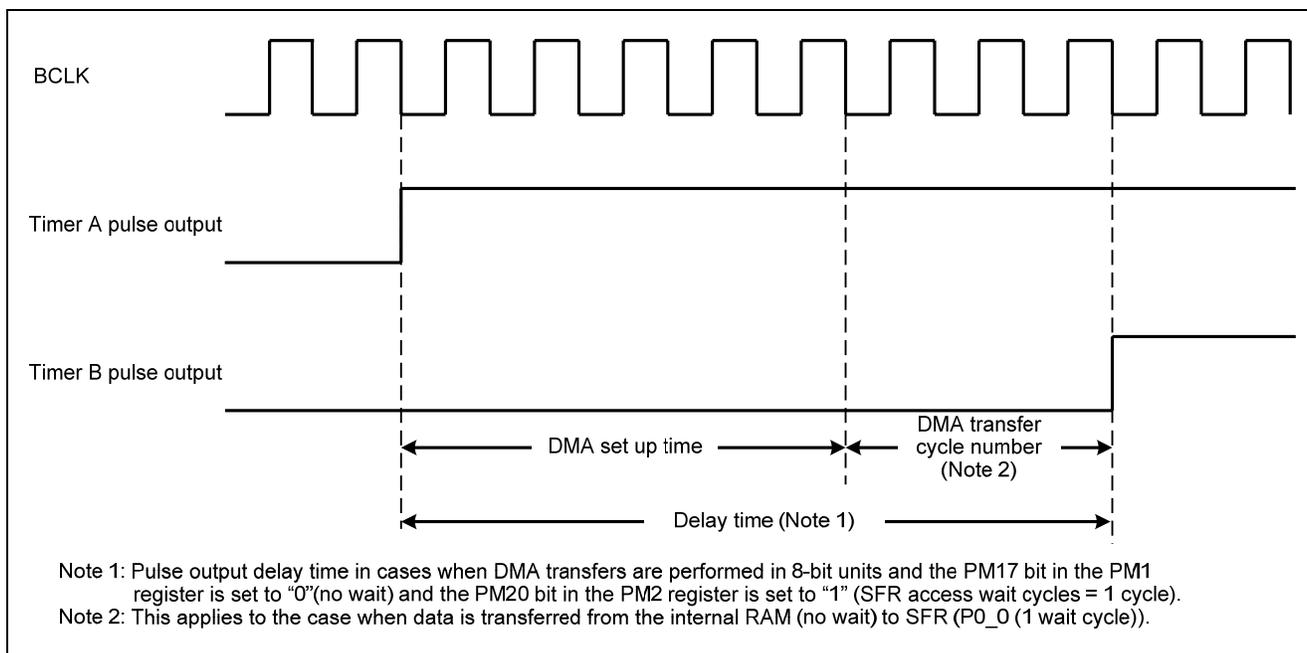


Figure 3. Pulse output delay example

(3) DMA Transfer Cycles

The number of DMAC transfer cycles can be calculated as follows:

Table 2 shows the number of DMA transfer cycles. Table 3 shows the Coefficient j, k.

No. of transfer cycles per transfer unit = No. of read cycles × j + No. of write cycles × k

Table 2. DMA Transfer Cycles

Transfer Unit	Bus Width	Access Address	Single-Chip Mode		Memory Expansion Mode	
			No. of Read Cycles	No. of Write Cycles	No. of Read Cycles	No. of Write Cycles
8-bit Transfers	16-bit	Even	1	1	1	1
		Odd	1	1	1	1
	8-bit	Even	-	-	1	1
		Odd	-	-	1	1
16-bit Transfers	16-bit	Even	1	1	1	1
		Odd	2	2	2	2
	8-bit	Even	-	-	2	2
		Odd	-	-	2	2

Table 3. Coefficient j, k

	Internal Area				External Area						
	Internal ROM, RAM		SFR		Separate Bus			Multiplex Bus			
	No Wait	With Wait	1-Wait (Note 1)	2-Wait (Note 2)	No Wait	With Wait (Note 1)			With Wait (Note 1)		
						1 Wait	2 Waits	3 Waits	1 Wait	2 Waits	3 Waits
j	1	2	2	3	1	2	3	4	3	3	4
k	1	2	2	3	2	2	3	4	3	3	4

NOTES:

1. Depends on the set value of CSE register.
2. Depends on the set value of PM20 bit in the PM2 register.
- (4) Limitations on Output Port

Since DMA transfers are performed in 8-bit units, no other pins (P0_1 to P0_7), except P0_0 used for timer pulse output, can be used as output ports.

7. Reference

Hardware manual

M16C/64 Group Hardware Manual

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