To our customers,

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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Renesas Technology Corp.
Customer Support Dept.
April 1, 2003

M16C/80 Series

Dividing 32 Bits

1.0 Abstract

This program performs a 32-bit unsigned division using registers.

2.0 Introduction

This program performs a 32-bit unsigned division using registers. Set the dividend in R2 and R0 and the divisor in R3 and R1 beginning with the upper half, respectively. The quotient and the remainder are output to R2 and R3, and to A1 and A0 beginning with the upper half, respectively. The zero divide information is output to the Z flag.

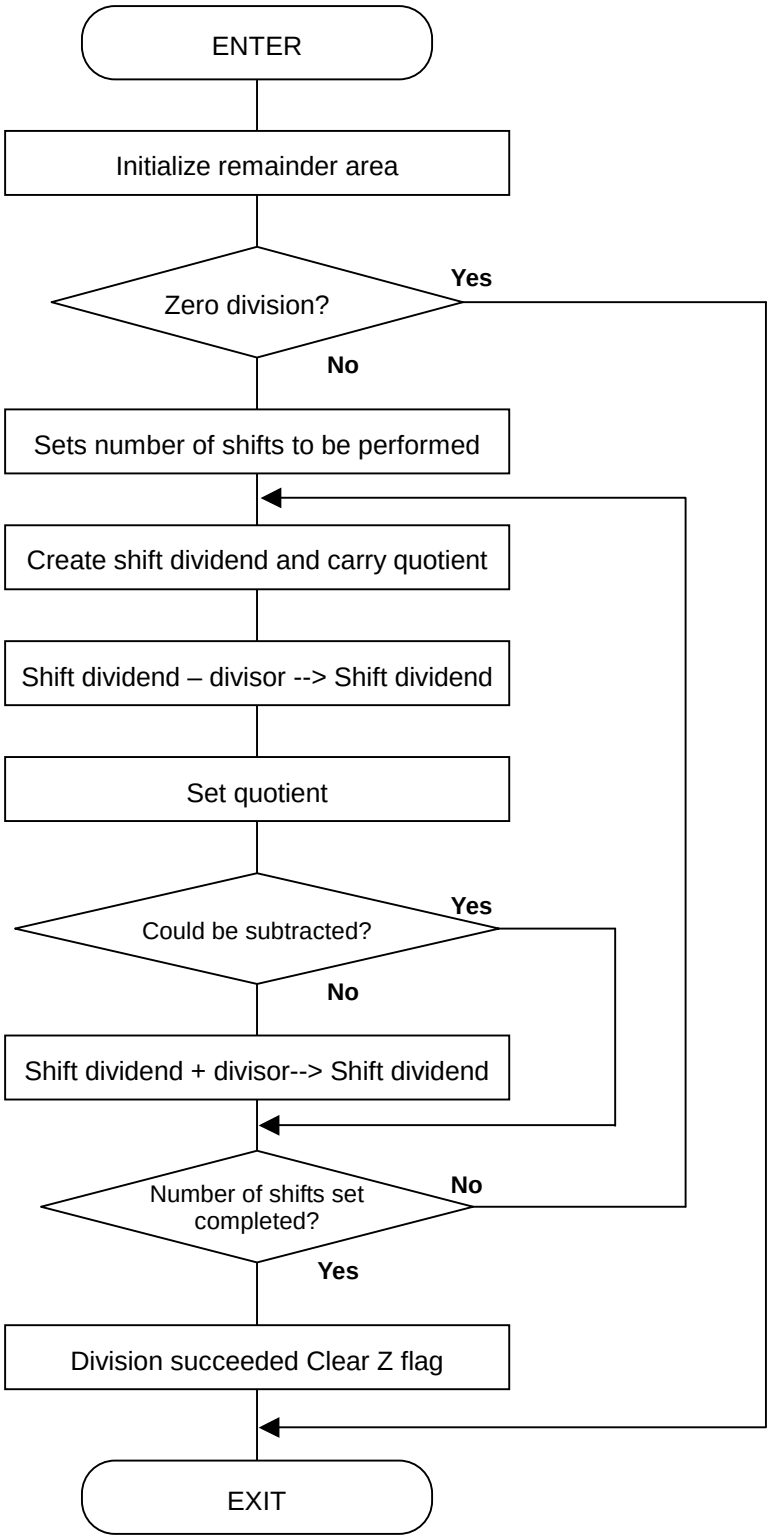
In this program, the dividend is pushed out one bit at a time beginning with the most significant bit as the program creates a dividend for calculation purposes and the divisor is subtracted from that data to get the quotient beginning with the most significant bit. The quotient and the remainder are obtained by repeating this operation as many times as the number of bits in the dividend.

Z	Meaning
0	Quotient and remainder are valid.
1	Quotient and remainder are invalid because division by zero is attempted.

Subroutine name : DIVIDE32	ROM capacity : 47byte
Interrupt during execution:Accepted	Number of stacks used : 3byte

Register/memory	Input	Output	Usage condition
R0	Lower half of dividend	Lower half of quotient	←
R1	Lower half of divisor	Does not change	←
R2	Upper half of dividend	Upper half of quotient	←
R3	Upper half of divisor	Does not change	←
A0	-	Lower half of remainder	←
A1	-	Upper half of remainder	←
CNT	-	Indeterminate	Number of shifts performed
Z flag	-	Zero divide information	←
Usage precautions	CNT is allocated in a stack area by configuring a stack frame as a temporary variable area in the program. Therefore, the value of CNT when program execution is completed is indeterminate. The dividend is destroyed as a result of program execution.		

3.0 Flowchart



4.0 Programming Code

```
;*****************************************************************
;       M16C Program Collection
;       CPU : M16C/80 series
;*****************************************************************
VromTOP     .EQU    0FE0000H                ; Declares start address of ROM
FBcnst      .EQU    001000H                 ; Assumed FB register value
;                                           ;
;===============================================================================
;   Title: Dividing 32 bits
;   Outline: Divides 32-bit data together using registers
;   Input:      ------------------------------>     Output:
;   R0(Lower half of dividend)          R0(Lower half of quotient)
;   R1(Lower half of divisor)           R1(Lower half of divisor)
;   R2(Upper half of dividend)          R2(Upper half of quotient)
;   R3(Upper half of divisor)           R3(Upper half of divisor)
;   A0( )                               A0(Lower half of remainder)
;   A1( )                               A1(Upper half of remainder)
;   Stack amount used: 3 bytes
;   Notes: R2R0 , R3R1
;           Division by zero is returned by Z flag.
;===============================================================================
            .SECTION    PROGRAM,CODE
            .ORG        VromTOP             ; ROM area
            .FB         FBcnst              ; Assumes FB register value
DIVIDE32:                                   ;
;-------------------------------------------------------------------------------;
;       Declaration of temporary variable;
;-------------------------------------------------------------------------------;
CNT         .EQU    -1                      ; Shift count counter
  ENTER     #1                              ; Sets stack frame
  MOV.B     #0,A0                           ; Initializes remainder area
  MOV.B     #0,A1                           ;
  CMP.W     #0,R1                           ;
  JNE       DIVIDE32_10                     ;
  CMP.W     #0,R3                           ;
  JEQ       DIVIDE32exit                    ; --> Division by zero
DIVIDE32_10:                                ;
  MOV.B     #32,CNT[FB]                     ; Sets number of shifts performed (32 times)
DIVIDE32_20:                                ;
  SHL.W     #1,R0                           ; Pushes dividend and carry quotient
  ROLC.W    R2                              ;
  ROLC.W    A0                              ; Creates dividend
  ROLC.W    A1                              ;
  SUB.W     R1,A0                           ; Subtracts divisor
  SBB.W     R3,A1                           ;
  BMC       0,R0L                           ; Sets quotient
  JC        DIVIDE32_30                     ; --> Subtraction of divisor succeeded
  ADD.W     R1,A0                           ; Restored to original data because
                                            ; subtraction of divisor failed
  ADC.W     R3,A1                           ;
DIVIDE32_30:                                ;
  ADJNZ.B   #-1,CNT[FB],DIVIDE32_20         ; --> Executes next digit
  FCLR      Z                               ; Division succeeded
DIVIDE32exit:                               ;
  EXITD                                     ; Clears stack frame
  ;                                         ;
            .END ;
```

5.0 Reference

MCU Technical Information Homepage

http://www.infomicom.maec.co.jp/indexe.htm
(or http://www.mdece.com/ , http://www.mitsubishichips.com/products/mcu/index.html or your local Web Site.)

Technical Support

E-mail: support@apl.maec.co.jp
(or your local support E-mail address. A private e-mail address should NOT be used.)

Data Sheet

M16C/80 group
(Use the latest version on the Homepage: http://www.infomicom.maec.co.jp/indexe.htm)

User's Manual

M16C/80 group
(Use the latest version on the Homepage: http://www.infomicom.maec.co.jp/indexe.htm)

RENESAS
Renesas Technology Corp.

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