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April 1st, 2010
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R8C/25, R8C/2B, R8C/2D Groups

Differences of R8C/25, R8C/2B and R8C/2D Groups

1. Abstract

This document is reference material for identifying differences of the R8C/25, R8C/2B, and R8C/2D Groups.

2. Introduction

This document is applied to the following MCUs:
- Applicable MCU: R8C/25, R8C/2B, and R8C/2D Groups

3. R8C/2B and R8C/2D Groups Replace R8C/25 Group

Since the R8C/2B and R8C/2D Groups are upward compatible products for the R8C/25 Group, replacing the R8C/25 Group with the R8C/2B and R8C/2D Groups is easy. For more details, refer to Chapter 4 in this document and to the hardware manual.

3.1 Upward Compatibility of Functions

Additional functions for the R8C/2B and R8C/2D Groups are shown below:
- Added timer RC and timer RF
- Added 1ch of UART/clock synchronous serial interface (UART2)
- Added repeat mode 1, single-sweep mode, and repeat sweep mode to the operating modes of the A/D converter (R8C/2D only)
- Added a D/A converter
- Added bus collision detection to the hardware LIN when Synch Break is transmitted

3.2 Upward Compatibility of Pins

Changes of the R8C/2B and 2D Groups are shown below:
- The UART1 CLK1 pin can be selected as P0_5 or P6_5 (no ports can be selected after reset is deasserted).
- The VREF pin is now independent of the P4_2 (input port) pin. The P4_2 (input port) pin has been eliminated.

3.3 Software Compatibility

The R8C/2B and R8C/2D Groups can use the R8C/25 Group software. However, characteristics such as timing may be changed depending on function improvements. Evaluate the software thoroughly. Note the following points when replacing the R8C/25 Group:
- To enable access to the registers associated with timer RD (addresses 0137h to 015Fh), set bit 4 (MSTTRD) in the module operation enable register (MSTCR) to 1.
- To enable access to the registers associated with SSU and I^2C bus (addresses 00B8h to 00BFh), set bit 3 (MSTIIC) in the module operation enable register (MSTCR) to 1.
- When setting the A/D input group select bit (bit 4 (ADGSEL0) in the A/D control register 0 (ADCON0)):
  (1) In the R8C/2B Group, set bit 3 (ADGSEL0) in A/D control register 2 (ADCON2); and
  (2) In the R8C/2D Group, set bit 4 (ADGSEL1) and bit 3 (ADGSEL0) in A/D control register 2 (ADCON2)
- When using the CLK1 pin for UART1, select the assignment of the CLK1 pin by bit 4 (CLK11PSEL) and bit 3 (CLK10PSET) in the UART1 function select register (U1SR).

4. Group Differences

4.1 Function and Specification Differences

Table 4.1 and Table 4.2 list differences in the functions and specifications.

Table 4.1 Function and Specification Differences (1) [1]

Item		R8C/25 Group	R8C/2B Group	R8C/2D Group
Flash memory versions		16 KB 24 KB 32 KB 48 KB 64 KB	48 KB 64 KB 96 KB 128 KB	
FLGA package		Available	Available	Not available
Power consumption		500 mW/300 mW [2]	700 mW	
High-speed on-chip oscillator	Oscillation frequency temperature and supply voltage dependence	40 MHz ± 5 % (-20°C to 85°C) (VCC = 2.7 V to 5.5 V)	40 MHz ± 2 %(-20°C to 85°C) (VCC = 2.7 V to 5.5 V)	
		40 MHz ± 6 % (-40 °C to 85 °C) (VCC = 2.7 V to 5.5 V)	40 MHz ± 2.5 % (-40 °C to 85 °C) (VCC = 2.7 V to 5.5 V)	
	Self powered consumption at oscillation	400 μA	550 μA	
Timers		Timer RA, RB, RD [3], and RE	Timer RA, RB, RC [4], RD [4], RE, and RF	
Serial interface		UART0 and UART1	UART0, UART1, and UART2	
SSU/I^{2}C bus[5]		No module operation enable bit	Module operation enable bit	

NOTES:
1. Refer to the hardware manual for details and electrical characteristics.
2. PTLG0064JA-A package
3. Module operation enable bit not provided.
4. Module operation enable bit provided.
5. I^{2}C bus is a trademark of Koninklijke Philips Electronics N.V.

Table 4.2 Function and Specification Differences (2) (1)

Item		R8C/25 Group	R8C/2B Group	R8C/2D Group
A/D converter	Operating mode	• One-shot mode • Repeat mode	• One-shot mode • Repeat mode 0	• One-shot mode • Repeat mode 0 • Repeat mode 1 • Single sweep mode • Repeat sweep mode
	Analog input pins	12 (AN0 to AN11)	12 (AN0 to AN11)	20 (AN0 to AN19)
D/A converter		Not included	Included	
Hardware LIN		Bus collision cannot be detected when transmitting Synch Break.	Bus collision can be detected when transmitting Synch Break (enable or disable can be switched).	
I/O ports		I/O ports: 41 Input port: 3	I/O ports: 55 Input port: 2	I/O ports: 71 Input port: 2

NOTES:
1. Refer to the hardware manual for details and electrical characteristics.

4.2 Pin Function Differences

Table 4.3 and Table 4.4 list the pin function differences.

Table 4.3 Pin Function Differences (1)

R8C/25 Group	R8C/2B Group	R8C/2D Group
P0_5/AN2	P0_5/AN2/CLK1 (1)	
P0_6/AN1	P0_6/AN1/DA0	
P0_7/AN0	P0_7/AN0/DA1	
–	P3_2/($\overline{\text{INT2}}$) (2)	
–	P3_6/(INT1) (2)	
VREF/P4_2	VREF	
–	P5_0/TRCCLK	
–	P5_1/TRCIOA/TRCTRG	
–	P5_2/TRCIOB	
–	P5_3/TRCIOC	
–	P5_4/TRCIOD	
–		P5_5
–		P5_6
–		P5_7
P6_3	P6_3/TXD2	
P6_4	P6_4/RXD2	
P6_5/CLK1	P6_5/(CLK1) (1)/CLK2	
–		P7_0/AN12
–		P7_1/AN13
–		P7_2/AN14
–		P7_3/AN15
–		P7_4/AN16
–		P7_5/AN17
–		P7_6/AN18
–		P7_7/AN19

NOTES:
1. The assignment of the CLK1 pin can be set.
2. These pins can be assigned to the pins in parentheses.

Table 4.4 Pin Function Differences (2)

R8C/25 Group	R8C/2B Group	R8C/2D Group
–	P8_0/TRFO00	
–	P8_1/TRFO01	
–	P8_2/TRFO02	
–	P8_3/TRFO10/TRFI	
–	P8_4/TRFO11	
–	P8_5/TRFO12	
–	P8_6	
–		P8_7
–		P9_0
–		P9_1
–		P9_2
–		P9_3
VCC/AVCC (1 pin)	VCC/AVCC (2 pins)	
VSS/AVSS (1 pin)	VSS/AVSS (2 pins)	

4.3 SFR Differences

Tables 4.5 to 4.7 list the differences in the SFRs.

Table 4.5 SFR Differences (1)

R8C/25 Group	R8C/2B Group	R8C/2D Group	Remarks
–	MSTCR		
FRA4	–		
–	FRA7		
–	TRCIC		
–	S2TIC		
–	S2RIC		
ADIC	ADIC		Assigned addresses differ
–	CMP1IC		
–	TRFIC		
–	CMP0IC		
–	CAPIC		
AD	AD0		Register names changed. Assigned addresses changed.
–		AD1	
–		AD2	
–		AD3	
ADCON2	ADCON2	ADCON2	Bits 3 and 4 added. Assigned addresses differ.
ADCON0	DCON0	ADCON0	Bit 4 functions changed. Assigned addresses differ.
ADCON1	ADCON1	ADCON1	Bit 0 added (1). Assigned addresses differ.
–	DA0		
–	DA1		
–	DACON		

NOTES:
1. This bit is only added to the R8C/2D Group.

Table 4.6 SFR Differences (2)

R8C/25 Group	R8C/2B Group	R8C/2D Group	Remarks
P3	P3		Bits 2 and 6 added
PD3	PD3		Bits 2 and 6 added
P4	P4		Bit 2 deleted
–	P5	P5	
–	PD5	PD5	
–		PD7	
–		P7	
–	PD8	PD8	
–		PD9	
–	P8	P8	
–		P9	
U1SR	U1SR		Functions changed
PMR	PMR		Bits 0 and 1 added
PUR0	PUR0		Bit 6 and bit 7 functions added
PUR1	PUR1		Bits 2 and 3 added
–	PUR2		
–	LINCR		
–	TRCMR		
–	TRCCR1		
–	TRCIER		
–	TRCSR		
–	TRCIOR0		
–	TRCIOR1		
–	TRC		
–	TRCGRA		
–	TRCGRB		
–	TRCGRC		
–	TRCGRD		
–	TRCCR2		
–	TRCDF		
–	TRCOER		

Table 4.7 SFR Differences (3)

R8C/25 Group	R8C/2B Group	R8C/2D Group	Remarks
–	U2MR		
–	U2BRG		
–	U2TB		
–	U2C0		
–	U2C1		
–	U2RB		
FMR0	FMR0		Bit 2 functions added
–	TRF		
–	TRFCR0		
–	TRFCR1		
–	TRFM0		
–	TRFM1		
–	TRFOUT		

4.4 Interrupt Vector Differences

Table 4.8 lists the differences in the relocatable vector tables.

Table 4.8 Relocatable Vector Table Differences

R8C/25 Group Interrupt Source	R8C/2B Group Interrupt Source	R8C/2D Group Interrupt Source	Software Interrupt Number
–	Timer RC		7
–	UART2 transmit		11
–	UART2 receive		12
A/D conversion	–		14
–	Compare 1		16
–	Timer RF		27
–	Compare 0		28
–	A/D conversion		30
–	Capture		31

5. Reference Document

Hardware Manual
R8C/25 Group Hardware Manual
R8C/2B Group Hardware Manual
R8C/2D Group Hardware Manual
(Use the most recent version of the document on the Renesas Technology Web site.)

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REVISION HISTORY	R8C/25, R8C/2B, R8C/2D Groups Differences of R8C/25, R8C/2B and R8C/2D Groups

Rev.	Date	Description	
		Page	Summary
1.00	Apr 18, 2008	–	First Edition issued

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