RX13T Group, RX130 Group

Differences Between the RX13T Group and the RX130 Group

Summary

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX13T Group and RX130 Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 48-pin package version of the RX13T Group and the 100-pin package version of the RX130 Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User’s Manual: Hardware of the products in question.

Target Devices

RX13T Group and RX130 Group

Contents

1. Comparison of Built-In Functions of RX13T Group and RX130 Group

A comparison of the built-in functions of the RX13T Group and RX130 Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a comparison of built-in functions of RX13T Group and RX130 Group.

Table 1.1 Comparison of Built-In Functions of RX13T Group and RX130 Group

Function	RX130	RX13T
CPU	●	
Operating modes	○	
Address space	▲	
Resets	○	
Option-setting memory (OFSM)	■	
Voltage detection circuit (LVDAb)	■	
Clock generation circuit	■	
Clock frequency accuracy measurement circuit (CAC)	■	
Low power consumption	■	
Register write protection function	■	
Exception handling	●	
Interrupt controller (ICUb)	■	
Buses	▲	
Data transfer controller (DTCa): RX130, (DTCb): RX13T	●/■	
Event link controller (ELC)	○	×
I/O ports	●/■	
Multi-function pin controller (MPC)	▲	
Multi-function timer pulse unit 2 (MTU2a): RX130, Multi-function timer pulse unit 3 (MTU3c): RX13T	●	
Port output enable 2 (POE2a): RX130, Port output enable 3 (POE3C): RX13T	●	
8-bit timer (TMR)	○	×
Compare match timer (CMT)	■	
Realtime clock (RTC)	○	×
Low-power timer (LPT)	○	×
Independent watchdog timer (IWDTa)	○	
Serial communications interface (SCIg, SCIh)	▲/■	
Remote Control Signal Receiver (REMC)	○	×
I^{2}C bus interface (RIICa)	■	
Serial peripheral interface (RSPIa)	○	×
CRC calculator (CRC)	○	
Capacitive touch sensing unit (CTSUa)	○	×
12-bit A/D converter (S12ADE): RX130, (S12ADF): RX13T	●/■	
D/A converter (DAa): RX130, D/A converter for generating comparator C reference voltage (DA): RX13T	■	
Temperature sensor	○	×
Comparator B (CMPBa): RX130, Comparator C (CMPC): RX13T	●/■	
Data operation circuit (DOC)	■	
RAM	▲	
Flash memory (FLASH)	▲	
Packages	●/■	

○: Available, ×: Unavailable, ●: Differs due to added functionality,
▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and **black text** indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is a comparative overview of CPU, and Table 2.2 is a comparison of CPU registers.

Table 2.1 Comparative Overview of CPU

Item	RX130	RX13T
CPU	• Maximum operating frequency: 32 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Eight 32-bit registers — Accumulator: One 64-bit register • Basic instructions: 73, variable-length instruction format • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 32 MHz • 32-bit RX CPU • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Nine 32-bit registers — Accumulator: One 64-bit registers • Basic instructions: 73, variable-length instruction format • Floating point instructions: 8 • DSP instructions: 9 • Addressing modes: 10 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian or big endian • On-chip 32-bit multiplier: 32 × 32 → 64 bits • On-chip divider: 32 / 32 → 32 bits • Barrel shifter: 32 bits
FPU	—	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard

Table 2.2 Comparison of CPU Registers

Register	Bit	RX130	RX13T
FPSW	—	—	Floating-point status word

2.2 Address space

Figure 2.1 is a comparative memory map of single-chip mode.

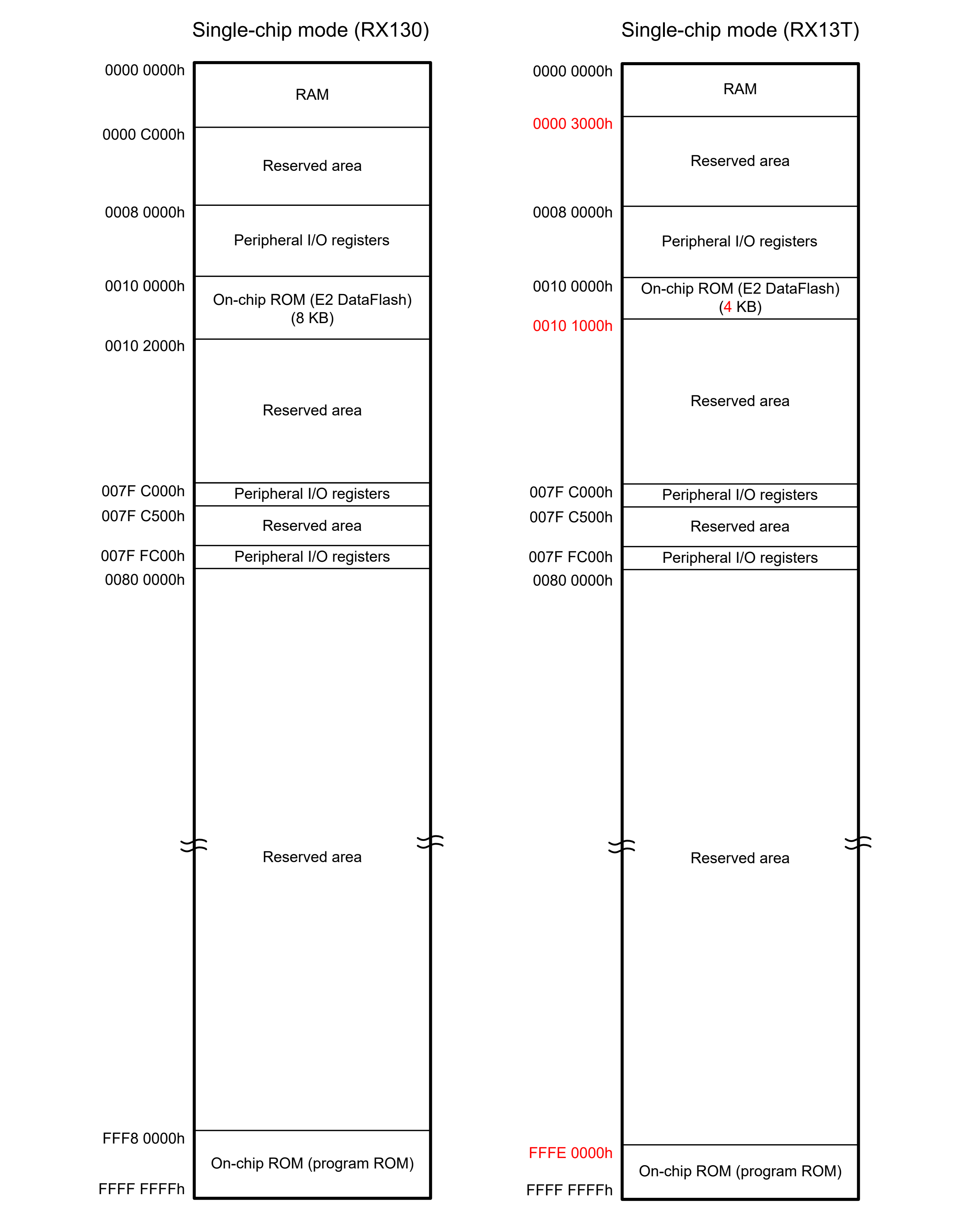

Figure 2.1 Comparative Memory Map of Single-Chip Mode

2.3 Option-Setting Memory

Table 2.3 is a comparison of option-setting memory registers.

Table 2.3 Comparison of Option-Setting Memory Registers

Register	Bit	RX130 (OFSM)	RX13T (OFSM)
OFS1	VDSEL[1:0]	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected 0 1: 2.82 V is selected 1 0: 2.51 V is selected 1 1: 1.90 V is selected	Voltage detection 0 level select bits b1 b0 0 0: 3.84 V is selected 0 1: 2.82 V is selected 1 0: 2.51 V is selected Do not set a value other than those above when using the voltage detection 0 circuit.
	FASTSTUP	Power-on fast startup time bit	—

2.4 Voltage Detection Circuit

Table 2.4 is a comparative overview voltage detection circuits, Table 2.5 is a comparison of voltage detection circuit registers, Table 2.6 is a comparative listing of the Vdet2 monitor setting procedure, and Table 2.7 is a comparative listing of the procedures for setting bits related to the voltage monitoring 2 interrupt and voltage monitoring 2 reset.

Table 2.4 Comparative Overview of Voltage Detection Circuits

Item		RX130 (LVDAb)			RX13T (LVDAb)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	Voltage drops past Vdet0	When voltage rises above or drops below Vdet1	When voltage rises above or drops below Vdet2	Voltage drops past Vdet0	Voltage rises or drops past Vdet1	Voltage rises or drops past Vdet2
				Input voltages to VCC and CMPA2 pin can be switched using LVCMPCR.EXVCCINP2 bit			
	Detection voltage	Voltage selectable from four levels using OFS1 register	Voltage selectable from 14 levels using the LVDLVLR.LVD1LVL[3:0] bits	Voltage selectable from four levels using the LVDLVLR.LVD2LVL[1:0] bits	Voltage selectable from three levels using OFS1 register	Voltage selectable from nine levels using the LVDLVLR.LVD1LVL[3:0] bits	Voltage selectable from four levels using the LVDLVLR.LVD2LVL[1:0] bits
	Monitor flag	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	—	LVD1SR.LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR.LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection		LVD1SR.LVD1DET flag: Vdet1 passage detection	LVD2SR.LVD2DET flag: Vdet2 passage detection
Voltage detection processing	Reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset	Voltage monitoring 0 reset	Voltage monitoring 1 reset	Voltage monitoring 2 reset
		Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC or CMPA2 pin CPU restart timing selectable: after specified time with VCC or CMPA2 pin > Vdet2 or after specified time with Vdet2 > VCC or CMPA2 pin	Reset when Vdet0 > VCC CPU restart after specified time with VCC > Vdet0	Reset when Vdet1 > VCC CPU restart timing selectable: after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC CPU restart timing selectable: after specified time with VCC > Vdet2 or Vdet2 > VCC

Item		RX130 (LVDAb)			RX13T (LVDAb)		
		Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2	Voltage Monitoring 0	Voltage Monitoring 1	Voltage Monitoring 2
Voltage detection processing	Interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt	—	Voltage monitoring 1 interrupt	Voltage monitoring 2 interrupt
			Non-maskable or maskable is selectable	Non-maskable or maskable is selectable		Non-maskable or maskable selectable	Non-maskable or maskable selectable
			Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC or CMPA2 pin and VCC or CMPA2 pin > Vdet2, or either		Interrupt request issued when Vdet1 > VCC and VCC > Vdet1 or either	Interrupt request issued when Vdet2 > VCC and VCC > Vdet2 or either
Event link function		—	Available Vdet1 passage detection event output	—	—	—	—

Table 2.5 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX130 (LVDAb)	RX13T (LVDAb)
LVD2CR1	LVD2IDTSEL [1:0]	Voltage monitoring 2 interrupt generation condition select bits b1 b0 0 0: When VCC or CMPA2 pin ≥ Vdet2 (rise) is detected 0 1: When VCC or CMPA2 pin < Vdet2 (drop) is detected 1 0: When drop and rise are detected 1 1: Setting prohibited	Voltage monitoring 2 interrupt generation condition select bits b1 b0 0 0: VCC ≥ Vdet2 (rise) is detected 0 1: VCC < Vdet2 (drop) is detected 1 0: When drop and rise are detected 1 1: Setting prohibited
LVD2SR	LVD2MON	Voltage monitoring 2 signal monitor flag 0: VCC or CMPA2 pin < Vdet2 1: VCC or CMPA2pin ≥ Vdet2 or LVD2MON is disabled	Voltage monitoring 2 signal monitor flag 0: VCC < Vdet2 1: VCC ≥ Vdet2 or LVD2MON is disabled
LVCMPCR	EXVCCINP2	Voltage detection 2 comparison voltage external input select bit	—

Register	Bit	RX130 (LVDAb)	RX13T (LVDAb)
LVDLVLR	LVD1LVL [3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V 1 0 0 1: 2.58 V 1 0 1 0: 2.48 V 1 0 1 1: 2.20 V 1 1 0 0: 1.96 V 1 1 0 1: 1.86 V Settings other than the above are prohibited.	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 0 0 0: 4.29 V 0 0 0 1: 4.14 V 0 0 1 0: 4.02 V 0 0 1 1: 3.84 V 0 1 0 0: 3.10 V 0 1 0 1: 3.00 V 0 1 1 0: 2.90 V 0 1 1 1: 2.79 V 1 0 0 0: 2.68 V Settings other than the above are prohibited.
LVD2CR0	LVD2RN	Voltage monitoring 2 reset negation select bit 0: Negation follows stabilization time (tLVD2) after VCC or CMPA2 pin > Vdet2 is detected. 1: Negation follows stabilization time (tLVD2) after assertion of voltage monitoring 2 reset.	Voltage monitoring 2 reset negation select bit 0: Negation follows stabilization time (tLVD2) after VCC > Vdet2 is detected. 1: Negation follows stabilization time (tLVD2) after assertion of voltage monitoring 2 reset.

Table 2.6 Comparison of Setting Procedures for Vdet2 Voltage Monitoring

Item		RX130 (LVDAb)	RX13T (LVDAb)
Vdet2 voltage monitoring setting procedure	1	Set the LVDLVLR.LVD2LVL[1:0] bits (voltage detection 2 detection voltage).	Set the LVDLVLR.LVD2LVL[1:0] bits (voltage detection 2 detection voltage).
	2	Set the LVCMPCR.EXVCCINP2 bit to 0 (VCC voltage) or 1 (CMPA2 pin input voltage).	—
	3	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).
	4	After waiting for td(E-A), set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison results output enabled).	After waiting for $Td_{(E-A)}$, set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison results output enabled).

Table 2.7 Comparison of Operation Setting Procedures for Voltage Monitoring 2 Interrupt and Voltage Monitoring 2 Reset Related Bits

Item		RX130 (LVDAb)	RX13T (LVDAb)
Voltage monitoring 2 interrupt	1	Select the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.
	2	Set the LVCMPCR.EXVCCINP2 bit to 0 (VCC voltage) or 1 (CMPA2 pin input voltage).	—
	3	Clear the LVD2CR0.LVD2RI bit to 0 (voltage monitoring 2 interrupt).	Clear the LVD2CR0.LVD2RI bit to 0 (voltage monitoring 2 interrupt).
	4	Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.	Select the timing of interrupt requests by setting the LVD2CR1.LVD2IDTSEL[1:0] bits. Select the type of interrupt by setting the LVD2CR1.LVD2IRQSEL bit.
	5	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).	Set the LVCMPCR.LVD2E bit to 1 (voltage detection 2 circuit enabled).
	6	Wait for at least td(E-A).	Wait for at least $Td_{(E-A)}$.
	7	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison results output enabled).	Set the LVD2CR0.LVD2CMPE bit to 1 (voltage monitoring 2 circuit comparison results output enabled).
	8	Wait for at least 2 μs.	Wait for at least 2 μs.
	9	Clear the LVD2SR.LVD2DET bit to 0.	Clear the LVD2SR.LVD2DET bit to 0.
	10	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled).	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled).
Voltage monitoring 2 reset	1	Select the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.	Select the detection voltage by setting the LVDLVLR.LVD2LVL[1:0] bits.
	2	Set the LVCMPCR.EXVCCINP2 bit to 0 (VCC voltage) or 1 (CMPA2 pin input voltage).	—
	3	Set the LVD2CR0.LVD2RI bit to 1 (voltage monitoring 2 reset). Select the type of reset negation by setting the LVD2CR0.LVD2RN bit.	Set the LVD2CR0.LVD2RI bit to 1 (voltage monitoring 2 reset). Select the type of reset negation by setting the LVD2CR0.LVD2RN bit.
	4	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled).	Set the LVD2CR0.LVD2RIE bit to 1 (voltage monitoring 2 interrupt/reset enabled).

2.5 Clock Generation Circuit

Table 2.8 is a comparative overview of the clock generation circuits, and Table 2.9 is a comparison of clock generation circuit registers.

Table 2.8 Comparative Overview of Clock Generation Circuits

Item	RX130	RX13T
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKB and PCLKD) supplied to the peripheral modules, PCLKD is the operating clock for the S12AD, and PCLKB is the operating clock for modules other than S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the RTC-dedicated sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the LPT clock (LPTCLK) to be supplied to the LPT. • Generates the REMC clock (REMCLK) to be supplied to the REMC.	• Generates the system clock (ICLK) to be supplied to the CPU, DTC, ROM, and RAM. • Of the peripheral module clocks (PCLKB and PCLKD) supplied to the peripheral modules, PCLKD is the operating clock for the S12AD and PCLKB is the operating clock for the other peripheral modules. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.
Operating frequency	• ICLK: 32 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 32 MHz (max.) • FCLK: — 1 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash) — 32 MHz (max.) (for reading from the E2 DataFlash) • CACCLK: Same as clock from respective oscillators • RTCSCLK: 32.768 kHz • IWDTCLK: 15 kHz • LPTCLK: Same as clock from selected oscillator • REMCLK: Same as clock from respective oscillators	• ICLK: 32 MHz (max.) • PCLKB: 32 MHz (max.) • PCLKD: 32 MHz (max.) • FCLK: — 1 MHz to 32 MHz (for programming and erasing the ROM and E2 DataFlash) — 32 MHz (max.) (for reading from the E2 DataFlash) • CACCLK: Same as clock from respective oscillators • IWDTCLK: 15 kHz

Item	RX130	RX13T
Main clock oscillator	• Resonator frequency: 1 MHz to 20 MHz (VCC ≥ 2.4 V), 1 MHz to 8 MHz (VCC < 2.4 V) • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function	• Resonator frequency: 1 MHz to 20 MHz • External clock input frequency: 20 MHz (max.) • Connectable resonator or additional circuit: ceramic resonator, crystal • Connection pins: EXTAL, XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance. • Drive capacity switching function
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: crystal • Connection pins: XCIN and XCOUT • Drive capacity switching function	—
PLL circuit	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 8 MHz • Frequency multiplication ratio: Selectable from 4 to 8 (increments of 0.5) • Oscillation frequency: 24 MHz to 32 MHz (VCC ≥ 2.4 V)	• Input clock source: Main clock • Input pulse frequency division ratio: Selectable from 1, 2, and 4 • Input frequency: 4 MHz to 8 MHz • Frequency multiplication ratio: Selectable from 4 to 8 (increments of 0.5) • Oscillation frequency: 24 MHz to 32 MHz
High-speed on-chip oscillator (HOCO)	Oscillation frequency: 32 MHz	Oscillation frequency: 32 MHz
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 4 MHz	Oscillation frequency: 4 MHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 15 kHz	Oscillation frequency: 15 kHz

Table 2.9 Comparison of Clock Generation Circuit Registers

Register	Bit	RX130	RX13T
SCKCR3	CKSEL[2:0]	Clock source select bits b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 0 1 1: Sub-clock oscillator 1 0 0: PLL circuit Settings other than the above are prohibited.	Clock source select bits b10 b8 0 0 0: LOCO 0 0 1: HOCO 0 1 0: Main clock oscillator 1 0 0: PLL circuit Settings other than the above are prohibited.
SOSCCR	—	Sub-clock oscillator control register	—
HOFCR	—	High-speed on-chip oscillator forced oscillation control register	—
CKOCR	—	CLKOUT output control register	—
MOFCR	MODRV21	Main clock oscillator drive capability switch bit VCC ≥ 2.4 V 0: 1 MHz to 10 MHz 1: 10 MHz to 20 MHz VCC < 2.4 V 0: 1 MHz to 8 MHz 1: Setting prohibited	Main clock oscillator drive capability switch bit 0: 1 MHz to less than 10 MHz 1: 10 MHz to 20 MHz

2.6 Clock Frequency Accuracy Measurement Circuit

Table 2.10 is a comparative overview of clock frequency accuracy measurement circuits, and Table 2.11 is a comparison of clock frequency accuracy measurement circuit registers.

Table 2.10 Comparative Overview of Clock Frequency Accuracy Measurement Circuits

Item	RX130 (CAC)	RX13T (CAC)
Measurement target clocks	The frequencies of the following clocks can be measured: • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB)	The frequencies of the following clocks can be measured: • Main clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)
Measurement reference clocks	• External clock input on CACREF pin • Main clock • Sub-clock • HOCO clock • LOCO clock • IWDTCLK clock • Peripheral module clock B (PCLKB)	• External clock input on CACREF pin • Main clock • HOCO clock • LOCO clock • IWDT-dedicated clock (IWDTCLK) • Peripheral module clock B (PCLKB)
Selectable function	Digital filter function	Digital filter function
Interrupt sources	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt	• Measurement end interrupt • Frequency error interrupt • Overflow interrupt
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.11 Comparison of Clock Frequency Accuracy Measurement Circuit Registers

Register	Bit	RX130 (CAC)	RX13T (CAC)
CACR1	FMCS[2:0]	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDTCLK clock 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.	Measurement target clock select bits b3 b1 0 0 0: Main clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.
CACR2	RSCS[2:0]	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 0 1: Sub-clock oscillator 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDTCLK clock 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.	Measurement reference clock select bits b3 b1 0 0 0: Main clock 0 1 0: HOCO clock 0 1 1: LOCO clock 1 0 0: IWDT-dedicated clock (IWDTCLK) 1 0 1: Peripheral module clock B (PCLKB) Settings other than the above are prohibited.

2.7 Low Power Consumption

Table 2.12 is a comparative overview of the low power consumption functions, Table 2.13 is a comparison of procedures for entering and exiting low power consumption modes and operating states in each mode, and Table 2.14 is a comparison of low power consumption registers.

Table 2.12 Comparative Overview of Low Power Consumption Functions

Item	RX130	RX13T
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clock (PCLKB), S12AD clock (PCLKD), and FlashIF clock (FCLK).
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • Deep sleep mode • Software standby mode	• Sleep mode • Deep sleep mode • Software standby mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Three operating power control modes are available — High-speed operating mode — Middle-speed operating mode — Low-speed operating mode	• Power consumption can be reduced in normal operation, sleep mode, and deep sleep mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Two operating power control modes are available — High-speed operating mode — Middle-speed operating mode

Table 2.13 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX130	RX13T
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	—
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 BFFFh: RX130, 0000 0000h to 0000 2FFFh: RX13T)	Operation possible (retained)	Operation possible (retained)
	DTC	Operation possible	Operation possible
	Flash memory	Operation	Operation
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Remote control signal receiver (REMC)	Operation possible	—
	Realtime clock (RTC)	Operation possible	—
	Low-power timer (LPT)	Operation possible	—
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	RTCOUT output	Operation possible	—
	CLKOUT output	Operation possible	—
	Comparator B	Operation possible	Operation possible
Deep sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	—
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 BFFFh: RX130, 0000 0000h to 0000 2FFFh: RX13T)	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX130	RX13T
Deep sleep mode	Remote control signal receiver (REMC)	Operation possible	—
	Realtime clock (RTC)	Operation possible	—
	Low-power timer (LPT)	Operation possible	—
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
	RTCOUT output	Operation possible	—
	CLKOUT output	Operation possible	—
	Comparator B	Operation possible	Operation possible
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of cancellation other than reset	Interrupt	Interrupt
	State after cancellation	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Stopped	Stopped
	Sub-clock oscillator	Operation possible	—
	High-speed on-chip oscillator	Operation possible	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM0 (0000 0000h to 0000 BFFFh: RX130, 0000 0000h to 0000 2FFFh: RX13T)	Stopped (retained)	Stopped (retained)
	DTC	Stopped (retained)	Stopped (retained)
	Flash memory	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Remote control signal receiver (REMC)	Operation possible	—
	Realtime clock (RTC)	Operation possible	—
	Low-power timer (LPT)	Operation possible	—
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
	CLKOUT output	Operation possible	—
	CLKOUT output	Operation possible	—
	Comparator B	Operation possible	Operation possible

Note: “Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.
“Stopped (retained)” means that internal register values are retained and internal operations are suspended.
“Stopped (undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

Table 2.14 Comparison of Low Power Consumption Registers

Register	Bit	RX130	RX13T
MSTPCRA	MSTPA4	8-bit timer 3 and 2 (unit 1) module stop bit	—
	MSTPA5	8-bit timer 1 and 0 (unit 0) module stop bit	—
MSTPCRB	MSTPB9	ELC module stop bit	—
	MSTPB17	Serial peripheral interface 0 module stop bit	—
	MSTPB25	Serial communication interface 6 module stop bit	—
	MSTPB31	Serial communication interface 0 module stop bit	—
MSTPCRC	MSTPC26	Serial communication interface 9 module stop bit	—
	MSTPC27	Serial communication interface 8 module stop bit	—
	MSTPC28	Remote control signal receiver 1 module stop bit	—
	MSTPC29	Remote control signal receiver 0 module stop bit	—
MSTPCRD	—	Module stop control register D	—
SOPCCR	—	Sub operating power control register	—
RSTCKCR	—	Sleep mode return clock source switching register	—

2.8 Register Write Protection Function

Table 2.15 is a comparative overview of the register write protection functions, and Table 2.16 is a comparison of register write protection function registers.

Table 2.15 Comparative Overview of Register Write Protection Functions

Item	RX130	RX13T
PRC0 bit	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOFCR, OSTDCR, OSTDSR, CKOCR, LOCOTRR, ILOCOTRR, HOCOTRR0	Registers related to the clock generation circuit: SCKCR, SCKCR3, PLLCR, PLLCR2, MOSCCR, LOCOCR, ILOCOCR, HOCOCR, OSTDCR, OSTDSR, LOCOTRR, ILOCOTRR, HOCOTRR0
PRC1 bit	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, SOPCCR • Registers related to the clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR	• Register related to the operating modes: SYSCR1 • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, OPCCR • Registers related to clock generation circuit: MOFCR, MOSCWTCR • Software reset register: SWRR
PRC2 bit	Registers related to the low power timer: LPTCR1, LPTCR2, LPTCR3, LPTPRD, LPCMR0, LPWUCR	—
PRC3 bit	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

Table 2.16 Comparison of Register Write Protection Function Registers

Register	Bit	RX130	RX13T
PRCR	PRC2	Protect bit 2	—

2.9 Exception Handling

Table 2.17 is a comparative overview of exception handling, Table 2.18 is a comparative listing of vectors, and Table 2.19 is a comparative listing of instructions for returning from exception handling routines.

Table 2.17 Comparative Overview of Exception Handling

Item	RX130	RX13T
Exception events	• Undefined instruction exception • Privileged instruction exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap	• Undefined instruction exception • Privileged instruction exception • Floating-point exception • Reset • Non-maskable interrupt • Interrupt • Unconditional trap

Table 2.18 Comparative Listing of Vectors

Item		RX130	RX13T
Undefined instruction exception		Fixed vector table	Fixed vector table
Privileged instruction exception		Fixed vector table	Fixed vector table
Floating-point exception		—	Fixed vector table
Reset		Fixed vector table	Fixed vector table
Non-maskable interrupt		Fixed vector table	Fixed vector table
Interrupt	Fast interrupt	FINTV	FINTV
	Other than fast interrupt	Relocatable vector table (INTB)	Relocatable vector table (INTB)
Unconditional trap		Relocatable vector table (INTB)	Relocatable vector table (INTB)

Table 2.19 Comparative Listing of Instructions for Returning from Exception Handling Routines

Item		RX130	RX13T
Undefined instruction exception		RTE	RTE
Privileged instruction exception		RTE	RTE
Floating-point exception		—	RTE
Reset		Return not possible	Return not possible
Non-maskable interrupt		Return not possible	Return not possible
Interrupt	Fast interrupt	RTFI	RTFI
	Other than fast interrupt	RTE	RTE
Unconditional trap		RTE	RTE

2.10 Interrupt Controller

Table 2.20 is a comparative overview of the interrupt controllers, and Table 2.21 is a comparison of interrupt controller registers.

Table 2.20 Comparative Overview of Interrupt Controllers

Item		RX130 (ICUb)	RX13T (ICUb)
Interrupts	Peripheral function interrupts	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules	• Interrupts from peripheral modules • Interrupt detection: Edge detection/level detection Edge detection or level detection is fixed for each source of connected peripheral modules
	External pin interrupts	• Interrupts from pins IRQ0 to IRQ7 • Number of sources: 8 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges. One of these detection methods can be set for each source. • Digital filter function: Supported	• Interrupts from pins IRQ0 to IRQ5 • Number of sources: 6 • Interrupt detection: Low level/falling edge/rising edge/rising and falling edges. One of these detection methods can be set for each source. • Digital filter function: Supported
	Software interrupt	• Interrupt generated by writing to a register. • One interrupt source	• Interrupt generated by writing to a register. • One interrupt source
	Event link interrupt	The ELSR8I or ELSR18I interrupt is generated by an ELC event	—
	Interrupt priority level	Priority levels are specified by registers.	Priority levels are specified by registers.
	Fast interrupt function	Faster interrupt processing of the CPU can be set only for a single interrupt source.	Faster interrupt processing of the CPU can be set only for a single interrupt source.
	DTC control	The DTC can be activated by interrupt sources.	The DTC can be activated by interrupt sources.
Non-maskable interrupts	NMI pin interrupt	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported	• Interrupt from the NMI pin • Interrupt detection: Falling edge/rising edge • Digital filter function: Supported
	Oscillation stop detection interrupt	Interrupt on detection of oscillation having stopped	Interrupt on detection of oscillation having stopped
	IWDT underflow/ refresh error interrupt	Interrupt on an underflow of the down counter or occurrence of a refresh error	Interrupt on an underflow of the down counter or occurrence of a refresh error
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1)	Interrupt from voltage monitoring circuit 1 (LVD1)
	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2)

Item	RX130 (ICUb)	RX13T (ICUb)
Return from low power consumption modes	• Sleep mode, deep sleep mode: Return is initiated by a non-maskable interrupt or any other interrupt source. • Software standby mode: Return is initiated by a non-maskable interrupt, IRQ0 to IRQ7 interrupt, or an RTC alarm/periodic interrupt.	• Sleep mode, deep sleep mode: Return is initiated by a non-maskable interrupt or any other interrupt source. • Software standby mode: Return is initiated by a non-maskable interrupt or IRQ0 to IRQ5 interrupt.

Table 2.21 Comparison of Interrupt Controller Registers

Register	Bit	RX130 (ICUb)	RX13T (ICUb)
IRQCRi	—	IRQ control register i (i = 0 to 7)	IRQ control register i (i = 0 to 5)
IRQFLTE0	FLTEN6	IRQ6 digital filter enable bit	—
	FLTEN7	IRQ7 digital filter enable bit	—
IRQFLTC0	FCLKSEL6 [1:0]	IRQ6 digital filter sampling clock bits	—
	FCLKSEL7 [1:0]	IRQ7 digital filter sampling clock bits	—

2.11 Buses

Table 2.22 is a comparative overview of the buses, and Table 2.23 is a comparative listing of bus errors.

Table 2.22 Comparative Overview of Buses

Bus Type		RX130	RX13T
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to ROM
Internal main buses	Internal main bus 1	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC • Connected to on-chip memory (RAM, ROM) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)	• Connected to peripheral modules (DTC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules • Operates in synchronization with the peripheral-module clock (PCLKB, PCLKD)	• Connected to peripheral modules • Operates in synchronization with the peripheral-module clock (PCLKB, PCLKD)
	Internal peripheral bus 3	• Connected to peripheral modules (Touch) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 6	• Connected to ROM (P/E) and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to ROM (P/E) and E2 DataFlash • Operates in synchronization with the FlashIF clock (FCLK)

Table 2.23 Comparative Listing of Bus Errors

Address	Description	RX130		RX13T	
		Illegal Address Access	Timeout	Illegal Address Access	Timeout
0000 0000h to 0007 FFFFh	Memory bus 1	—	—	—	—
0008 0000h to 0008 7FFFh	Internal peripheral bus 1	—	—	—	—
0008 8000h to 0009 FFFFh	Internal peripheral bus 2	△	—	△	△
000A 0000h to 000B FFFFh	Internal peripheral bus 3	△	—	△	—
000C 0000h to 000F FFFFh	Reserved area	○	—	○	—
0010 0000h to 00FF FFFFh	Internal peripheral bus 6	△	—	△	—
0100 0000h to 07FF FFFFh	Reserved area	○	—	○	—
0800 0000h to 0FFF FFFFh	Reserved area	—	—	—	—
1000 0000h to 7FFF FFFFh	Reserved area	○	—	○	—
8000 0000h to FFFF FFFFh	Memory bus 2	—	—	—	—

—: A bus error does not result.

△: A bus error may or may not result.

○: A bus error results.

2.12 Data Transfer Controller

Table 2.24 is a comparative overview of the data transfer controllers, and Table 2.25 is a comparison of data transfer controller registers.

Table 2.24 Comparative Overview of Data Transfer Controllers

Item	RX130 (DTCa)	RX13T (DTCb)
Number of transfer channels	Equal to number of all interrupt sources that can start a DTC transfer.	Equal to number of all interrupt sources that can start a DTC transfer.
Transfer modes	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.	• Normal transfer mode — A single activation leads to a single data transfer. • Repeat transfer mode — A single activation leads to a single data transfer. — The transfer address returns to the transfer start address when the number of data transfers equals the repeat size. — The maximum number of repeat transfers is 256, and the maximum data transfer size is 256 × 32 bits, or 1,024 bytes. • Block transfer mode — A single activation leads to the transfer of a single block of data. — The maximum block size is 256 × 32 bits = 1,024 bytes.
Chain transfer function	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.	• Multiple data transfer types can be executed sequentially in response to a single transfer request. • Either “performed only when the transfer counter reaches 0” or “every time” can be selected.
Sequence transfer	—	A complex series of transfers can be registered as a sequence. Any sequence can be selected by the transfer data and executed. • Only one sequence transfer trigger source can be selected at a time. • Up to 256 sequences can correspond to a single trigger source. • The data that is initially transferred in response to a transfer request determines the sequence. • The entire sequence can be executed on a single request, or the sequence can be suspended in the middle and resumed on the next transfer request (sequence division).

Item	RX130 (DTCa)	RX13T (DTCb)
Transfer space	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)	• 16 MB in short-address mode (within 0000 0000h to 007F FFFFh or FF80 0000h to FFFF FFFFh, excluding reserved areas) • 4 GB in full-address mode (within 0000 0000h to FFFF FFFFh, excluding reserved areas)
Data transfer units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units	• Single data unit: 1 byte (8 bits), 1 word (16 bits), or 1 longword (32 bits) • Single block size: 1 to 256 data units
CPU interrupt requests	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.	• An interrupt request to the CPU can be generated by a DTC activation interrupt. • An interrupt request to the CPU can be generated after a single data transfer. • An interrupt request to the CPU can be generated after transfer of the specified number of data units.
Event link function	An event link request is generated after one data transfer (for block transfers, after one block).	—
Read skip	Reading of the transfer information can be skipped when the same transfer is repeated.	Reading of the transfer information can be skipped when the same transfer is repeated.
Write-back skip	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.	Write-back of transferred data that is not updated can be skipped when the address of the transfer source or destination is fixed.
Write-back disable	—	Ability to disable write-back of transfer information
Displacement addition	—	Ability to add displacement to the transfer source address (selectable by each transfer information)
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state

Table 2.25 Comparison of Data Transfer Controller Registers

Register	Bit	RX130 (DTCa)	RX13T (DTCb)
MRA	WBDIS	—	Write-back disable bit*1
MRB	SQEND	—	Sequence transfer end bit
	INDX	—	Index table reference bit
MRC	—	—	DTC mode register C
DTCIBR	—	—	DTC index table base register
DTCOR	—	—	DTC operation register
DTCSQE	—	—	DTC sequence transfer enable register
DTCDISP	—	—	DTC address displacement register

Note: 1. Transfer information is usually allocated to a RAM area, but it can be allocated to a ROM area by setting the MRA.WBDIS bit to 1 (no write-back).

2.13 I/O Ports

Table 2.26 is a comparative overview of the I/O ports (of 48-pin products), Table 2.27 is a comparative listing of I/O port functions, and Table 2.28 is a comparison of I/O port registers.

Table 2.26 Comparative Overview of I/O Ports (48-Pin)

Port Symbol	RX130 (48-Pin)	RX13T (48-Pin)
PORT1	P14 to P17	P10, P11
PORT2	P26, P27	P22 to P24
PORT3	P30, P31, P35 to P37	P36, P37
PORT4	P40 to P42, P45 to P47	P40 to P47
PORT7	—	P70 to P76
PORT9	—	P93, P94
PORTA	PA1, PA3, PA4, PA6	PA2, PA3
PORTB	PB0, PB1, PB3, PB5	PB0 to PB7
PORTC	PC0 to PC7	—
PORTD	—	PD3 to PD6
PORTE	PE1 to PE4	PE2
PORTH	PH0 to PH3	—
PORTJ	PJ6, PJ7	—

Table 2.27 Comparison of I/O Port Functions

Item	Port Symbol	RX130	RX13T
Input pull-up function	PORT0	P03 to P07	—
	PORT1	P12 to P17	P10, P11
	PORT2	P20 to P27	P22, P23, P24
	PORT3	P30 to P34, P36, P37	P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P55	—
	PORT7	—	P70 to P76
	PORT9	—	P93, P94
	PORTA	PA0 to PA7	PA2, PA3
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	—
	PORTD	PD0 to PD7	PD3 to PD6
	PORTE	PE0 to PE7	—
	PORTH	PH0 to PH3	—
	PORTJ	PJ1, PJ3, PJ6, PJ7	—
Open drain output function	PORT1	P12 to P17	P10, P11
	PORT2	P20, P21 to P23, P26, P27	P22, P23, P24
	PORT3	P30 to P34, P36, P37	P36, P37
	PORT7	—	P70 to P76
	PORT9	—	P93, P94
	PORTA	PA0 to PA7	PA2, PA3
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	—
	PORTD	PD0 to PD2	PD3 to PD6
	PORTE	PE0 to PE3	—
	PORTJ	PJ3	—

Item	Port Symbol	RX130	RX13T
Drive capacity switching function	PORT0	P03 to P07	—
	PORT1	P12 to P17	P10, P11
	PORT2	P20 to P27	P22, P23, P24
	PORT3	P30 to P34, P36, P37	—
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P55	—
	PORT7	—	P70 to P76
	PORT9	—	P93, P94
	PORTA	PA0 to PA7	PA2, PA3
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	—
	PORTD	PD0 to PD7	PD3 to PD6
	PORTE	PE0 to PE7	—
	PORTH	PH0 to PH3	—
	PORTJ	PJ1, PJ3, PJ6, PJ7	—
5 V tolerant	PORT1	P12, P13, P16, P17	—
	PORTB	—	PB1, PB2

Table 2.28 Comparison of I/O Port Registers

Register	Bit	RX130	RX13T
PDR	B0 to B7	Pm0 to Pm7 I/O select bits (m = 0 to 5, A to E, H, J)	Pm0 to Pm7 I/O select bits (m = 1 to 4, 7, 9, A, B, D)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 5, A to E, H, J)	Pm0 to Pm7 output data store bits (m = 1 to 4, 7, 9, A, B, D)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 5, A to E, H, J)	Pm0 to Pm7 bits (m = 1 to 4, 7, 9, A, B, D)
PMR	B0 to B7	Pm0 pin mode control bits (m = 0 to 5, A to E, H, J)	Pm0 to Pm7 pin mode control bits (m = 1 to 3, 7, 9, A, B, D, E)
ODR0	B0 (RX130) B0, B1 (RX13T)	Pm0 output type select bit (m = 1 to 3, A to E, J) 0: CMOS output 1: N-channel open-drain	Pm0 output type select bit (m = 1, 2, 7, 9, A, B, D) • P10, P70 b0 0: CMOS output 1: N-channel open-drain b1 This bit is read as 0. The write value should be 0. • PB0 b1 b0 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Hi-Z

Register	Bit	RX130	RX13T
ODR0	B2, B3 (RX130) B2 (RX13T)	Pm1 output type select bit (m = 1 to 3, A to E, J) • P21, P31, PA1, PB1, PC1, PD1 b2 0: CMOS output 1: N-channel open-drain b3 This bit is read as 0. The write value should be 0. • PE1 b3 b2 0 0: CMOS output 0 1: N-channel open-drain 1 0: P-channel open-drain 1 1: Hi-Z	Pm1 output type select bit (m = 1, 2, 7, 9, A, B, D) 0: CMOS output 1: N-channel open-drain
	B4, B6	Pm2 and Pm3 output type select bits (m = 1 to 3, A to E, J)	Pm2 and Pm3 output type select bits (m = 1, 2, 7, 9, A, B, D)
ODR1	B0, B2, B4, B6	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 1 to 3, A to C)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 2, 3, 7, 9, B, D)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 5, A to E, H, J)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 4, 7, 9, A, B, D)
PSRA	—	Port switching register A	—
PSRB	—	Port switching register B	—
DSCR	B0 to B7	Pm0 to Pm7 drive capacity control bits (m = 1 to 3, 5, A to E, H, J)	Pm0 to Pm7 drive capacity control bits (m = 1, 2, 7, 9, A, B, D)

2.14 Multi-Function Pin Controller

Table 2.29 is a comparison of the assignments of multiplexed pins, and Table 2.30 to Table 2.44 are comparisons of multi-function pin controller registers.

In the following comparison of the assignments of multiplexed pins, **light blue text** designates pins that exist on the RX13T Group only and **orange text** pins that exist on the RX130 Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.29 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX130 (MPC) 48-Pin	RX13T (MPC) 48-Pin
Interrupt	NMI (input)	P35	○	×
		PE2	×	○
	IRQ0 (input)	P30	○	×
		PH1	○	×
		P10	×	○
		P93	×	○
		PE2	×	○
	IRQ1 (input)	P31	○	×
		PH2	○	×
		P11	×	○
		P94	×	○
	IRQ2 (input)	P22	×*1	○
		PB1	×*1	○
		PD4	×*1	○
	IRQ3 (input)	P24	×*1	○
		PB4	×*1	○
		PD5	×*1	○
	IRQ4 (input)	PB1	○	×
		P14	○	×
		P23	×	○
		PA2	×	○
	IRQ5 (input)	PA4	○	×
		P15	○	×
		P70	×	○
		PB7	×	○
		PD6	×	○
	IRQ6 (input)	PA3	○	
		P16	○	
	IRQ7 (input)	PE2	○	
		P17	○	
Clock generation circuit	CLKOUT (output)	PE3	○	
		PE4	○	
Multi-function timer unit 2 (RX130) / multi-function timer unit 3 (RX13T)	MTIOC0A (input/output)	PB3	○	○
		PD3	×	○
	MTIOC0B (input/output)	P15	○	×
		PA1	○	×
		PB2	×	○
		PD4	×	○
	MTIOC0C (input/output)	PB1	○	○
		PD5	×	○

Module/ Function	Pin Function	Port Allocation	RX130 (MPC) 48-Pin	RX13T (MPC) 48-Pin
Multi-function timer unit 2 (RX130) / multi-function timer unit 3 (RX13T)	MTIOC0D (input/output)	PA3	○	×
		PB0	×	○
		PD6	×	○
	MTIOC1A (input/output)	PE4	○	×
		P93	×	○
		PA2	×	○
	MTIOC1B (input/output)	PB5	○	×
		PA3	×	○
		PB6	×	○
	MTIOC2A (input/output)	P26	○	×
		PB5	○	×
		PA3	×	○
		PB0	×	○
	MTIOC2B (input/output)	P27	○	×
		PA2	×	○
		P94	×	○
	MTIOC3A (input/output)	P14	○	×
		P17	○	×
		PC7	○	×
		P11	×	○
		PB6	×	○
	MTIOC3B (input/output)	P17	○	×
		PC5	○	×
		P71	×	○
	MTIOC3C (input/output)	P16	○	×
		PC6	○	×
		PB7	×	○
	MTIOC3D (input/output)	P16	○	×
		PC4	○	×
		P74	×	○
	MTIOC4A (input/output)	PB3	○	×
		PE2	○	×
		P72	×	○
	MTIOC4B (input/output)	P30	○	×
		PE3	○	×
		P73	×	○
	MTIOC4C (input/output)	PB1	○	×
		PE1	○	×
		P75	×	○
	MTIOC4D (input/output)	P31	○	×
		PE4	○	×
		P76	×	○
	MTIC5U (input)	PA4	○	×
		P24	×	○
		P94	×	○
	MTIC5V (input)	PA6	○	×
		P23	×	○
		P93	×	○

Module/ Function	Pin Function	Port Allocation	RX130 (MPC) 48-Pin	RX13T (MPC) 48-Pin
Multi-function timer unit 2 (RX130) / multi-function timer unit 3 (RX13T)	MTIC5W (input)	PB0	○	×
		P22	×	○
		PB1	×	○
	MTCLKA (input)	P14	○	×
		PA4	○	×
		PC6	○	×
		P11	×	○
		P94	×	○
		PB1	×	○
	MTCLKB (input)	P15	○	×
		PA6	○	×
		PC7	○	×
		P10	×	○
		PB0	×	○
	MTCLKC (input)	PA1	○	×
		PC4	○	×
		PB2	×	○
	MTCLKD (input)	PA3	○	×
		PC5	○	×
		PB7	×	○
	ADSM0 (output)	PB2		○
Port output enable 2 (RX130) / port output enable 3 (RX13T)	POE0# (input)	PC4	○	×
		P70	×	○
	POE1# (input)	PB5	○	
	POE2# (input)	PA6	○	
	POE3# (input)	PB3	○	
	POE8# (input)	P17	○	×
		P30	○	×
		PE3	○	×
		PB4	×	○
		P11	×	○
	POE10# (input)	PE2		○
8-bit timer	TMO0 (output)	PB3	○	
		PH1	○	
	TMCI0 (input)	PB1	○	
		PH3	○	
	TMRI0 (input)	PA4	○	
		PH2	○	
	TMO1 (output)	P17	○	
		P26	○	
	TMCI1 (input)	PC4	○	
	TMRI1 (input)	PB5	○	
	TMO2 (output)	P16	○	
		PC7	○	
	TMCI2 (input)	P15	○	
		P31	○	
		PC6	○	
	TMRI2 (input)	P14	○	
		PC5	○	

Module/ Function	Pin Function	Port Allocation	RX130 (MPC) 48-Pin	RX13T (MPC) 48-Pin
8-bit timer	TMCI3 (input)	P27	○	
		PA6	○	
	TMRI3 (input)	P30	○	
Serial communications interface	RXD1 (input) / SMISO1 (input/output) / SSCL1 (input/output)	P15	○	×
		P30	○	×
		PD5	×	○
		PB7	×	○
	TXD1 (output) / SMOSI1 (input/output) / SSDA1 (input/output)	P16	○	×
		P26	○	×
		PD3	×	○
		PB6	×	○
	SCK1 (input/output)	P17	○	×
		P27	○	×
		PD4	×	○
	CTS1# (input) / RTS1# (output) / SS1# (input)	P14	○	×
		P31	○	×
		PD6	×	○
	RXD5 (input) / SMISO5 (input/output) / SSCL5 (input/output)	PA3	○	×
		PB1	×	○
		PB7	×	○
		P24	×	○
	TXD5 (output) / SMOSI5 (input/output) / SSDA5 (input/output)	PA4	○	×
		PB2	×	○
		PB6	×	○
		P23	×	○
	SCK5 (input/output)	PA1	○	×
		PC4	○	×
		P93	×	○
		PB3	×	○
	CTS5# (input) / RTS5# (output) / SS5# (input)	PA6	○	×
		PA2	×	○
	RXD6 (input) / SMISO6 (input/output) / SSCL6 (input/output)	PB0	○	
	TXD6 (output) / SMOSI6 (input/output) / SSDA6 (input/output)	PB1	○	
	SCK6 (input/output)	PB3	○	
	RXD12 (input) / SMISO12 (input/output) / SSCL12 (input/output) / RXDX12 (input)	PE2	○ (The SMISO12 function is not available on 48-pin package products.)	×
		P94	×	○

Module/ Function	Pin Function	Port Allocation	RX130 (MPC) 48-Pin	RX13T (MPC) 48-Pin
Serial communications interface	TXD12 (output) / SMOSI12 (input/output) / SSDA12 (input/output) / TXDX12 (output) / SIOX12 (input/output)	PE1	○ (The SMOSI12 function is not available on 48-pin package products.)	×
		PB0	×	○
	SCK12 (input/output)	PB3	×*1	○
		P93	×*1	○
	CTS12# (input) / RTS12# (output) / SS12# (input)	PE3	○ (The SS12# function is not available on 48-pin package products.)	×
		PA3	×	○
I²C bus interface	SCL0 (input/output)	P16	○	×
		PB1	×	○
	SDA0 (input/output)	P17	○	×
		PB2	×	○
Serial peripheral interface	RSPCKA (input/output)	PB0	○	
		PC5	○	
	MOSIA (input/output)	P16	○	
		PA6	○	
		PC6	○	
	MISOA (input/output)	P17	○	
		PC7	○	
	SSLA0 (input/output)	PA4	○	
		PC4	○	
	SSLA2 (output)	PA1	○	
12-bit A/D converter	AN000 (input)*2	P40	○	○
	AN001 (input)*2	P41	○	○
	AN002 (input)*2	P42	○	○
	AN003 (input)	P43	×*1	○
	AN004 (input)	P44	×*1	○
	AN005 (input)*2	P45	○	○
	AN006 (input)*2	P46	○	○
	AN007 (input)*2	P47	○	○
	AN017 (input)*2	PE1	○	
	AN018 (input)*2	PE2	○	
	AN019 (input)*2	PE3	○	
	AN020 (input)*2	PE4	○	
	ADTRG0# (input)	P16	○	×
		P93	×	○
		PB5	×	○
	ADST0 (output)	PD6		○
Clock frequency accuracy measurement circuit	CACREF (input)	PC7	○	×
		PH0	○	×
		P23	×	○
		PB3	×	○
LVD voltage detection input	CMPA2 (input)*2	PE4	○	

Module/ Function	Pin Function	Port Allocation	RX130 (MPC) 48-Pin	RX13T (MPC) 48-Pin
Comparator B (RX130) / comparator C (RX13T)	CMPB0 (input)*2	PE1	○	
	CVREFB0 (input)*2	PE2	○	
	CMPB1 (input)*2	PA3	○	
	CVREFB1 (input)*2	PA4	○	
	CMPOB1 (output)	PB1	○	
	CMPC00 (input)	P40		○
	CMPC02 (input)	P43		○
	CMPC03 (input)	P46		○
	CMPC10 (input)	P41		○
	CMPC12 (input)	P44		○
	CMPC13 (input)	P47		○
	CMPC20 (input)	P42		○
	CMPC22 (input)	P45		○
	COMP0 (output)	P24		○
	COMP1 (output)	P23		○
	COMP2 (output)	P22		○
	CVREFC0 (input)	P11		○
Capacitive Touch Sensing Unit (CTSU)	TSCAP (—)	PC4	○	
	TS1 (input/output)	P31	○	
	TS2 (output)	P30	○	
	TS3 (output)	P27	○	
	TS4 (output)	P26	○	
	TS5 (output)	P15	○	
	TS6 (output)	P14	○	
	TS7 (output)	PH3	○	
	TS8 (output)	PH2	○	
	TS9 (output)	PH1	○	
	TS10 (output)	PH0	○	
	TS13 (output)	PC7	○	
	TS14 (output)	PC6	○	
	TS15 (output)	PC5	○	
	TS20 (output)	PB5	○	
	TS22 (output)	PB3	○	
	TS24 (output)	PB1	○	
	TS25 (output)	PB0	○	
	TS26 (output)	PA6	○	
	TS28 (output)	PA4	○	
	TS29 (output)	PA3	○	
	TS31 (output)	PA1	○	
	TS33 (output)	PE4	○	
	TS34 (output)	PE3	○	
	TS35 (output)	PE2	○	

Notes: 1. This function is not available on 48-pin package products in the RX130 Group.
2. When using this pin function on the RX130 Group, set the corresponding pin to general-purpose input. (Clear the PORT.PDR.Bm and PORT.PMR.Bm bits to 0.)

Table 2.30 Comparison of P0n Pin Function Control Register (P0nPFS)

Register	Bit	RX130 (MPC)	RX13T (MPC)
P0nPFS	—	P0n pin function select register (n = 3, 5, 7)	—

Table 2.31 Comparison of P1n Pin Function Control Register (P1nPFS)

Register	Bit	RX130 (MPC) (n = 2 to 7)	RX13T (MPC) (n = 0 and 1)
P10PFS	—	—	P10 pin function control register
P11PFS	—	—	P11 pin function control register
P12PFS	—	P12 pin function control register	—
P13PFS	—	P13 pin function control register	—
P14PFS	—	P14 pin function control register	—
P15PFS	—	P15 pin function control register	—
P16PFS	—	P16 pin function control register	—
P17PFS	—	P17 pin function control register	—

Table 2.32 Comparison of P2n Pin Function Control Register (P2nPFS)

Register	Bit	RX130 (MPC) (n = 0 to 7)	RX13T (MPC) (n = 2 to 4)
P20PFS	—	P20 pin function control register	—
P21PFS	—	P21 pin function control register	—
P22PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 00010b: MTCLKC 00101b: TMO0 01010b: SCK0	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 11110b: COMP2
P23PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 00010b: MTCLKD 01011b: CTS0#/RTS0#/SS0#	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00111b: CACREF 01010b: TXD5/SMOSI5/SDA5 11110b: COMP1
P24PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 00010b: MTCLKA 00101b: TMRI1	Pin function select bits 00000b: Hi-Z 00001b: MTIC5U 01010b: RXD5/SMISO5/SSCL5 11110b: COMP0
P25PFS	—	P25 pin function control register	—
P26PFS	—	P26 pin function control register	—
P27PFS	—	P27 pin function control register	—
P2nPFS	ISEL	—	Interrupt input function select bit

Table 2.33 Comparison of P3n Pin Function Control Register (P3nPFS)

Register	Bit	RX130 (MPC)	RX13T (MPC)
P3nPFS	—	P3n pin function select register (n = 0 to 4)	—

Table 2.34 Comparison of P4n Pin Function Control Register (P4nPFS)

Register	Bit	RX130 (MPC) (n = 0 to 7)	RX13T (MPC) (n = 0 to 7)
P4nPFS	ASEL	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000 (100/80/64/52/48-pin) P41: AN001 (100/80/64/52/48-pin) P42: AN002 (100/80/64/52/48-pin) P43: AN003 (100/80/64/52/48-pin) P44: AN004 (100/80/64/52/48-pin) P45: AN005 (100/80/64/52/48-pin) P46: AN006 (100/80/64/52/48-pin) P47: AN007 (100/80/64/52/48-pin)	Analog input function select bit 0: Used as other than as analog pin 1: Used as analog pin P40: AN000/CMPC00 (48/32-pin) P41: AN001/CMPC10 (48/32-pin) P42: AN002/CMPC20 (48/32-pin) P43: AN003/CMPC02 (48/32-pin) P44: AN004/CMPC12 (48/32-pin) P45: AN005/CMPC22 (48-pin) P46: AN006/CMPC03 (48-pin) P47: AN007/CMPC13 (48-pin)

Table 2.35 Comparison of P5n Pin Function Control Register (P5nPFS)

Register	Bit	RX130 (MPC)	RX13T (MPC)
P5nPFS	—	P5n pin function select register (n = 1, 2, 4, 5)	—

Table 2.36 Comparison of P7n Pin Function Control Register (P7nPFS)

Register	Bit	RX130 (MPC)	RX13T (MPC)
P7nPFS	—	—	P7n pin function control register (n = 0 to 6)

Table 2.37 Comparison of P9n Pin Function Control Register (P9nPFS)

Register	Bit	RX130 (MPC)	RX13T (MPC)
P9nPFS	—	—	P9n pin function control register (n = 3 and 4)

Table 2.38 Comparison of PAn Pin Function Control Register (PAnPFS)

Register	Bit	RX130 (MPC) (n = 0 to 7)	RX13T (MPC) (n = 2 and 3)
PA0PFS	—	PA0 pin function control register	—
PA1PFS	—	PA1 pin function control register	—
PA2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01010b: RXD5/SMISO5/SSCL5 01101b: SSLA3 11001b: TS30	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1A 00011b: MTIOC2B 01010b: CTS5#/RTS5#/SS5#
PA3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 00010b: MTCLKD 01010b: RXD5/SMISO5/SSCL5 11001b: TS29	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1B 00011b: MTIOC2A 01100b: CTS12#/RTS12#/SS12#
PA4PFS	—	PA4 pin function control register	—
PA5PFS	—	PA5 pin function control register	—
PA6PFS	—	PA6 pin function control register	—
PA7PFS	—	PA7 pin function control register	—
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA3: IRQ6 (100/80/64/48-pin) PA4: IRQ5 (100/80/64/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA2: IRQ4 (48-pin)
	ASEL	Analog function select bit	—

Table 2.39 Comparison of PBn Pin Function Control Register (PBnPFS)

Register	Bit	RX130 (MPC) (n = 0 to 7)	RX13T (MPC) (n = 0 to 7)
PB0PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 01011b: RXD6/SMISO6/SSCL6 01101b: RSPCKA 11001b: TS25	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 00010b: MTCLKB 00011b: MTIOC2A 01100b: TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12
PB1PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00010b: MTIOC4C 00101b: TMCI0 01011b: TXD6/SMOSI6/SSDA6 10000b: CMPOB1 11001b: TS24	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 00010b: MTCLKA 00011b: MTIC5W 01010b: RXD5/SMISO5/SSCL5 01111b: SCL0
PB2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01011b: CTS6#/RTS6#/SS6# 11001b: TS23	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 00010b: MTCLKC 00011b: ADSM0 00111b: TXD5/SMOSI5/SSDA5 01111b: SDA0
PB3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00010b: MTIOC4A 00101b: TMO0 00111b: POE3# 01011b: SCK6 11001b: TS22	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 00111b: CACREF 01010b: SCK5 01100b: SCK12
PB4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 01011b: CTS9#/RTS9#/SS9# 11001b: TS21	Pin function select bits 00000b: Hi-Z 00111b: POE8#

Register	Bit	RX130 (MPC) (n = 0 to 7)	RX13T (MPC) (n = 0 to 7)
PB5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC2A 00010b: MTIOC1B 00101b: TMRI1 00111b: POE1# 01010b: SCK9 11001b: TS20	Pin function select bits 00000b: Hi-Z 01001b: ADTRG0#
PB6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3D 01010b: RXD9/SMISO9/SSCL9 11001b: TS19	Pin function select bits 00000b: Hi-Z 00001b: MTIOC1B 00011b: MTIOC3A 01010b: TXD5/SMOSI5/SSDA5 01011b: TXD1/SMOSI1/SSDA1
PB7PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3B 01010b: TXD9/SMOSI9/SSDA9 11001b: TS18	Pin function select bits 00000b: Hi-Z 00001b: MTIOC3C 00010b: MTCLKD 01010b: RXD5/SMISO5/SSCL5 01011b: RXD1/SMISO1/SSCL1
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ4 (100/80/64/48-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB1: IRQ2 (48/32-pin) PB4: IRQ3 (48-pin) PB7: IRQ5 (48/32-pin)

Table 2.40 Comparison of PCn Pin Function Control Register (PCnPFS)

Register	Bit	RX130 (MPC)	RX13T (MPC)
PCnPFS	—	PCn pin function control register (n = 0 to 7)	—

Table 2.41 Comparison of PDn Pin Function Control Register (PDnPFS)

Register	Bit	RX130 (MPC) (n = 0 to 7)	RX13T (MPC) (n = 3 to 6)
PD0PFS	—	PD0 pin function select register	—
PD1PFS	—	PD1 pin function select register	—
PD2PFS	—	PD2 pin function select register	—
PD3PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00111b: POE8#	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0A 01010b: TXD1/SMOSI1/SSDA1
PD4PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00111b: POE3#	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0B 01010b: SCK1
PD5PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5W 00111b: POE2#	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0C 01010b: RXD1/SMISO1/SSCL1
PD6PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIC5V 00111b: POE1#	Pin function select bits 00000b: Hi-Z 00001b: MTIOC0D 01001b: ADST0 01010b: CTS1#/RTS1#/SS1#
PD7PFS	—	PD7 pin function select register	—
PDnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD0: IRQ0 (100/80-pin) PD1: IRQ1 (100/80-pin) PD2: IRQ2 (100/80-pin) PD3: IRQ3 (100-pin) PD4: IRQ4 (100-pin) PD5: IRQ5 (100-pin) PD6: IRQ6 (100-pin) PD7: IRQ7 (100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PD4: IRQ2 (48-pin) PD5: IRQ3 (48-pin) PD6: IRQ5 (48-pin)
	ASEL	Analog function select bit	—

Table 2.42 Comparison of PEn Pin Function Control Register (PEnPFS)

Register	Bit	RX130 (MPC) (n = 0 to 7)	RX13T (MPC) (n = 2)
PE0PFS	—	PE0 pin function control register	—
PE1PFS	—	PE1 pin function control register	—
PE2PFS	PSEL[4:0]	Pin function select bits 00000b: Hi-Z 00001b: MTIOC4A 01100b: RXD12/RXDX12/SMISO12/SSCL12 11001b: TS35	Pin function select bits 00000b: Hi-Z 00111b: POE10#
PE3PFS	—	PE3 pin function control register	—
PE4PFS	—	PE4 pin function control register	—
PE5PFS	—	PE5 pin function control register	—
PE6PFS	—	PE6 pin function control register	—
PE7PFS	—	PE7 pin function control register	—
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7 (100/80/64/48-pin) PE5: IRQ5 (100/80/64-pin) PE6: IRQ6 (100-pin) PE7: IRQ7 (100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ0 (48/32-pin)
	ASEL	Analog function select bit	—

Table 2.43 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX130 (MPC)	RX13T (MPC)
PHnPFS	—	PHn pin function control register (n = 0 to 3)	—

Table 2.44 Comparison of PJn Pin Function Control Register (PJnPFS)

Register	Bit	RX130 (MPC)	RX13T (MPC)
PJnPFS	—	PJn pin function control register (n = 1, 3, 6, 7)	—

2.15 Multi-Function Timer Pulse Unit 2/Multi-Function Timer Pulse Unit 3

Table 2.45 is a comparative overview of multi-function timer pulse units 2 and 3, and Table 2.46 is a comparison of the registers of multi-function timer pulse units 2 and 3.

Table 2.45 Comparative Overview of Multi-Function Timer Pulse Units 2 and 3

Item	RX130 (MTU2a)	RX13T (MTU3c)
Pulse input/output	Max. 16 lines	Max. 16 lines
Pulse input	3 lines	3 lines
Count clocks	8 or 7 clocks for each channel (4 clocks for MTU5)	11 clocks for each channel (14 clocks for MTU0, 12 clocks for MTU2, 10 clocks for MTU5, and four clocks for MTU1 and MTU2 (when LWA = 1))
Available operations	[MTU0 to MTU4] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 12-phase PWM output in combination with synchronous operation	[MTU0 to MTU4] • Waveform output at compare match • Input capture function (noise filter setting function) • Counter clear operation • Simultaneous writing to multiple timer counters (TCNT) • Simultaneous clearing by compare match or input capture • Simultaneous register input/output by synchronous counter operation • Up to 12-phase PWM output in combination with synchronous operation
	[MTU0, MTU3, MTU4] • Ability to specify buffer operation	[MTU0, MTU3, MTU4] • Ability to specify buffer operation
	[MTU1, MTU2] • Independent specification of phase counting mode • Cascade connection operation available	[MTU1, MTU2] • Independent specification of phase counting mode • Ability to specify 32-bit phase counting mode for interlocked operation of MTU1 and MTU2 (when TMDR3.LWA = 1) • Cascade connection operation available
	[MTU3, MTU4] • Ability to produce six-phase waveform output, which includes three phases each for positive and negative complementary PWM or reset PWM output, through interlocking operation	[MTU3, MTU4] • Ability to output in complementary PWM and reset PWM operation positive and negative signals in six phases through interlocked operation of MTU3 and MTU4 • Ability to transfer values from buffer registers to temporary registers at peaks and troughs of the timer counter or at writes to the buffer registers (MTU4.TGRD) in complementary PWM mode • Ability to select double-buffering in complementary PWM mode

Item	RX130 (MTU2a)	RX13T (MTU3c)
Available operations	[MTU3, MTU4] • Ability to select between two types of waveform output (chopping or level) by specifying a mode for driving AC synchronous motors (brushless DC motors) that uses complementary PWM output or reset PWM output	[MTU3, MTU4] • Ability to select between two types of waveform output (chopping or level) by specifying a mode for driving AC synchronous motors (brushless DC motors) that uses complementary PWM output or reset PWM output and interlocking with MTU0
	[MTU5] • Dead time compensation counter function • Input capture function (noise filter setting function) • Counter clear operation	[MTU5] • Ability to use the MTU5 as a dead-time compensation counter
Interrupt skipping function	A/D converter start trigger skipping function	Ability to skip interrupts at counter peaks and troughs and A/D conversion start triggers in complementary PWM mode
Interrupt sources	28 sources	28 sources
Buffer operation	Automatic transfer of register data	Automatic transfer of register data (transfer from buffer register to timer register)
Trigger generation	• Ability to generate A/D converter start trigger	• Ability to generate A/D converter start trigger • Ability to start A/D conversion at any desired timing and in synchronization with PWM output using A/D conversion start request delaying function
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.46 Comparison of Registers of Multi-Function Timer Pulse Units 2 and 3

Register	Bit	RX130 (MTU2a)	RX13T (MTU3c)
TCR2	—	—	Timer control register 2
TMDR (RX130) TMDR1 (RX13T)	MD[3:0]	Mode select bits b3 b0 0 0 0 0: Normal mode 0 0 0 1: Setting prohibited 0 0 1 0: PWM mode 1 0 0 1 1: PWM mode 2 0 1 0 0: Phase counting mode 1 0 1 0 1: Phase counting mode 2 0 1 1 0: Phase counting mode 3 0 1 1 1: Phase counting mode 4 1 0 0 0: Reset-synchronized PWM mode 1 0 0 1: Setting prohibited 1 0 1 x: Setting prohibited 1 1 0 0: Setting prohibited 1 1 0 1: Complementary PWM mode 1 (transfer at crest) 1 1 1 0: Complementary PWM mode 2 (transfer at trough) 1 1 1 1: Complementary PWM mode 3 (transfer at crest and trough)	Mode select bits b3 b0 0 0 0 0: Normal mode 0 0 0 1: Setting prohibited 0 0 1 0: PWM mode 1 0 0 1 1: PWM mode 2 0 1 0 0: Phase counting mode 1 0 1 0 1: Phase counting mode 2 0 1 1 0: Phase counting mode 3 0 1 1 1: Phase counting mode 4 1 0 0 0: Reset-synchronized PWM mode 1 0 0 1: Phase counting mode 5 1 0 1 x: Setting prohibited 1 1 0 0: Setting prohibited 1 1 0 1: Complementary PWM mode 1 (transfer at crest) 1 1 1 0: Complementary PWM mode 2 (transfer at trough) 1 1 1 1: Complementary PWM mode 3 (transfer at crest and trough)
TMDR2A	—	—	Timer mode register 2
TMDR3	—	—	Timer mode register 3
MTU0.TIER2	TTGE2	—	A/D conversion start request enable 2 bit
TSR	—	Timer status register Initial value after a reset differs.	Timer status register
TCNTLW	—	—	Timer longword counter
TGRALW TGRBLW	—	—	Timer longword general register
MTU.TSTR (RX130) MTU.TSTRA (RX13T)	—	Timer start register	Timer start register
TSYR (RX130) TSYRA (RX13T)	—	Timer synchronous register	Timer synchronous register
TCSYSTR	—	—	Timer synchronous start register
TRWER (RX130) TRWERA (RX13T)	—	Timer read/write enable register	Timer read/write enable register
TOER (RX130) TOERA (RX13T)	—	Timer output master enable register	Timer output master enable register
TOCR1 (RX130) TOCR1A (RX13T)	—	Timer output control register 1	Timer output control register 1
TOCR2 (RX130) TOCR2A (RX13T)	—	Timer output control register 2	Timer output control register 2
TOLBR (RX130) TOLBRA (RX13T)	—	Timer output level buffer register	Timer output level buffer register

Register	Bit	RX130 (MTU2a)	RX13T (MTU3c)
TGCR (RX130) TGCRA (RX13T)	—	Timer gate control register	Timer gate control register A
TCNTS (RX130) TCNTSA (RX13T)	—	Timer subcounter	Timer subcounter
TDDR (RX130) TDDRA (RX13T)	—	Timer dead time data register	Timer dead time data register
TCDR (RX130) TCDRA (RX13T)	—	Timer period data register	Timer period data register
TCBR (RX130) TCBRA (RX13T)	—	Timer period buffer register	Timer period buffer register
TITCR (RX130) TITCR1A (RX13T)	—	Timer interrupt skipping set register	Timer interrupt skipping set register 1
TITCNT (RX130) TITCNT1A (RX13T)	—	Timer interrupt skipping counter	Timer interrupt skipping counter 1
TBTER (RX130) TBTERA (RX13T)	—	Timer buffer transfer set register	Timer buffer transfer set register
TDER (RX130) TDERA (RX13T)	—	Timer dead time enable register	Timer dead time enable register
TWCR (RX130) TWCRA (RX13T)	—	Timer waveform control register	Timer waveform control register
NFCR (RX130) NFCRn (RX13T)	—	Noise filter control register	Noise filter control register n (n = 0 to 5)
MTU0.NFCRC	—	—	Noise filter control register C
TITMRA	—	—	Timer interrupt skipping mode register
TITCR2A	—	—	Timer interrupt skipping set register 2
TITCNT2A	—	—	Timer interrupt skipping counter 2
TADSTRGR0	—	—	A/D conversion start request select register 0

2.16 Port Output Enable 2/Port Output Enable 3

Table 2.47 is a comparative overview of port output enable 2 and 3, and Table 2.48 is a comparison of the registers of port output enable 2 and 3.

Table 2.47 Comparative Overview of Port Output Enable 2 and 3

Item	RX130 (POE2a)	RX13T (POE3C)
Pin status while output is disabled	High-impedance	High-impedance
High-impedance control target pins	MTU output pins • MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) • MTU3 pin (MTIOC3B, MTIOC3D) • MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D)	MTU output pins • MTU0 pin (MTIOC0A, MTIOC0B, MTIOC0C, MTIOC0D) • MTU3 pin (MTIOC3B, MTIOC3D) • MTU4 pin (MTIOC4A, MTIOC4B, MTIOC4C, MTIOC4D)
Conditions for generating high-impedance request	• Input pin change: Detection of signal input on POE0# to POE3# or POE8# • Short circuit between output pins: A match (short circuit) between the output signal levels (active level) over one or more cycles on any of the following combinations of pins [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D • SPOER register setting • Detection of oscillation stop by main clock oscillator	• Input pin change: Detection of signal input on POE0#, POE8#, or POE10# • Short circuit between output pins: A match (short circuit) between the output signal levels (active level) over one or more cycles on any of the following combinations of pins [MTU complementary PWM output pins] — MTIOC3B and MTIOC3D — MTIOC4A and MTIOC4C — MTIOC4B and MTIOC4D • SPOER register setting • Detection of oscillation stop by main clock oscillator • Detection of output from comparator C (CMPC)
Functions	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 clock cycles can be set for the POE0# to POE3# and POE8# input pins individually. • Pins for complementary PWM output from the MTU can be placed in the high-impedance state on detection of falling edges or sampling of the low level on the POE0# to POE3# pins. • MTU0 output pins can be placed in the high-impedance state on detection of falling edges or sampling of the low level on the POE8# pin. • Pins for complementary PWM output from the MTU and MTU0 output pins can be placed in the high-impedance state when oscillation by the clock generation circuit stops.	• Falling-edge detection or sampling of the low level 16 times at PCLK/8, PCLK/16, or PCLK/128 clock cycles can be set for the POE0#, POE8#, and POE10# input pins individually. • Output on all control target pins can be placed in the high-impedance state on detection of falling edges or sampling of the low level on the POE0#, POE8#, and POE10# pins. • Output on all control target pins can be placed in the high-impedance state when oscillation-stop by the clock generation circuit is detected.

Item	RX130 (POE2a)	RX13T (POE3C)
Functions	• The output level of the pins for MTU complementary PWM output can be compared and the pins placed in the high-impedance state if they simultaneously output an active level for one or more PCLK clock cycles. • The pins for MTU complementary PWM output and the MTU0 output pins can be placed in the high-impedance state by writing to the POE registers. • Interrupts can be generated by the input level detection result of the POE0# to POE3# and POE8# pins and by the output level comparison result of the pins for MTU complementary PWM output.	• The output level of the pins for MTU complementary PWM output can be compared and the pins placed in the high-impedance state if they simultaneously output an active level for one or more clock cycles. • All control target pins can be placed in the high-impedance state by comparator C (CMPC) output detection. • All control target pins can be placed in the high-impedance state by making settings to the POE registers. • Individual interrupts can be generated either by input level sampling or by the output level comparison result.

Table 2.48 Comparison of Registers of Port Output Enable 2 and 3

Register	Bit	RX130 (POE2a)	RX13T (POE3C)
ICSR1	POE1M[1:0]	POE1 mode select bits	—
	POE2M[1:0]	POE2 mode select bits	—
	POE3M[1:0]	POE3 mode select bits	—
	POE1F	POE1 flag	—
	POE2F	POE2 flag	—
	POE3F	POE3 flag	—
ICSR2 (RX130) ICSR3 (RX13T)	PIE2 (RX130) PIE3 (RX13T)	Port interrupt enable 2 bit	Port interrupt enable 3 bit
ICSR4	—	—	Input level control/status register 4
ICSR3 (RX130) ICSR6 (RX13T)	—	Input level control/status register 3	Input level control/status register 6
ALR1	—	—	Active level register 1
SPOER	CH34HIZ (RX130) MTUCH34HIZ (RX13T)	MTU3 and MTU4 output high-impedance enable bit	MTU3 and MTU4 pin high-impedance enable bit
	CH0HIZ (RX130) MTUCH0HIZ (RX13T)	MTU0 high-impedance enable bit (b1)	MTU0 pin high-impedance enable bit (b2)
POECR1	PE0ZE	MTIOC0A high-impedance enable bit	—
	PE1ZE	MTIOC0B high-impedance enable bit	—
	PE2ZE	MTIOC0C high-impedance enable bit	—
	PE3ZE	MTIOC0D high-impedance enable bit	—
	MTU0AZE	—	MTIOC0A (PB3) pin high-impedance enable bit
	MTU0BZE	—	MTIOC0B (PB2) pin high-impedance enable bit

Register	Bit	RX130 (POE2a)	RX13T (POE3C)
POECR1	MTU0CZE	—	MTIOC0C (PB1) pin high-impedance enable bit
	MTU0DZE	—	MTIOC0D (PB0) pin high-impedance enable bit
	MTU0A1ZE	—	MTIOC0A (PD3) pin high-impedance enable bit
	MTU0B1ZE	—	MTIOC0B (PD4) pin high-impedance enable bit
	MTU0C1ZE	—	MTIOC0C (PD5) pin high-impedance enable bit
	MTU0D1ZE	—	MTIOC0D (PD6) pin high-impedance enable bit
POECR2	—	Port output enable control register 2 POECR2 is an 8-bit register.	Port output enable control register 2 POECR2 is a 16-bit register.
	P3CZEA (RX130) MTU4BDZE (RX13T)	MTU port 3 high-impedance enable bit (b4)	MTIOC4B/MTIOC4D pin high-impedance enable bit (b8)
	P2CZEA (RX130) MTU4ACZE (RX13T)	MTU port 2 high-impedance enable bit (b5)	MTIOC4A/MTIOC4C pin high-impedance enable bit (b9)
	P1CZEA (RX130) MTU3BDZE (RX13T)	MTU port 2 high-impedance enable bit (b6)	MTIOC3B/MTIOC3D pin high-impedance enable bit (b10)
POECR4	—	—	Port output enable control register 4
POECR5	—	—	Port output enable control register 5
POECMPFR	—	—	Port output enable comparator output detection flag register
POECMPSEL	—	—	Port output enable comparator request select register

2.17 Compare Match Timer

Table 2.49 is a comparative overview of compare match timer.

Table 2.49 Comparative Overview of Compare Match Timer

Item	RX130 (CMT)	RX13T (CMT)
Count clocks	Four frequency dividing clocks: One clock among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.	Four frequency dividing clocks: One clock among PCLK/8, PCLK/32, PCLK/128, and PCLK/512 can be selected for each channel.
Interrupts	A compare match interrupt can be requested for each channel.	A compare match interrupt can be requested for each channel.
Event link function (output)	An event signal is output at CMT1 compare match.	—
Event link function (input)	• Ability to link to a specified module • Support for CMT1 count start, event counter, or count restart operation	—
Low power consumption function	Ability to specify module stop state	Ability to specify to module stop state

2.18 Serial Communications Interface

Table 2.50 is a comparative overview of the serial communications interfaces, and Table 2.51 is a comparison of serial communications interface channel specifications, and Table 2.52 is a comparison of serial communications interface registers.

Table 2.50 Comparative Overview of Serial Communications Interfaces

Item		RX130 (SCIg, SCIh)	RX13T (SCIg, SCIh)
Number of channels		• SCIg: 6 channels • SCIh: 1 channel	• SCIg: 2 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
Interrupt sources		Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	Transmit end, transmit data empty, receive data full, and receive error, completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Module stop state can be set for each channel.	Module stop state can be set for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly.
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).	• An internal or external clock can be selected. • Transfer rate clock input from the MTU can be used (SCI1, SCI5, and SCI12).

Item		RX130 (SCIg, SCIh)	RX13T (SCIg, SCIh)
Asynchronous mode	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/ reception.	CTSn# and RTSn# pins can be used in controlling transmission/ reception.
Smart card interface mode	Error processing	An error signal can be automatically transmitted when detecting a parity error during reception	An error signal can be automatically transmitted when detecting a parity error during reception
		Data can be automatically retransmitted when receiving an error signal during transmission	Data can be automatically retransmitted when receiving an error signal during transmission
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.
Simple I^{2}C mode	Communication format	I^{2}C bus format	I^{2}C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer rate	Fast mode is supported.	Fast mode is supported.
	Noise cancellation	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.	The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters, and the interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.

Item		RX130 (SCIg, SCIh)	RX13T (SCIg, SCIh)
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates
	I/O control function	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	Usable as reloading timer	Usable as reloading timer
Bit rate modulation function		Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)		• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output	—

Table 2.51 Comparison of Serial Communications Interface Channel Specifications

Item	RX130 (SCIg, SCIh)	RX13T (SCIg, SCIh)
Synchronous mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI12
Clock synchronous mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI12
Smart card interface mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI12
Simple I^2C mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI12
Simple SPI mode	SCI0, SCI1, SCI5, SCI6, SCI8, SCI9, SCI12	SCI1, SCI5, SCI12
Extended serial mode	SCI12	SCI12
TMR clock input (RX130)/ MTU clock input (RX13T)	SCI5, SCI6, SCI12	SCI1, SCI5, SCI12
Event link function	SCI5	—

Table 2.52 Comparison of Serial Communications Interface Registers

Register	Bit	RX130 (SCIg, SCIh)	RX13T (SCIg, SCIh)
SCR	CKE[1:0]	Clock enable bits When SCMR.SMIF bit = 0 (asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin is high-impedance. 0 1: On-chip baud rate generator A clock with the same frequency as the bit rate is output from the SCKn pin. 1 x: External clock or TMR clock*1 A clock with a frequency 16 times the bit rate should be input on the SCKn pin. A clock signal with a frequency eight times the bit rate should be input when the SEMR.ABCS bit is set to 1. The SCKn pin is high-impedance when using the TMR clock.*1 (Clock synchronous mode) b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.	Clock enable bits When SCMR.SMIF bit = 0 (asynchronous mode) b1 b0 0 0: On-chip baud rate generator The SCKn pin is high-impedance. 0 1: On-chip baud rate generator A clock with the same frequency as the bit rate is output from the SCKn pin. 1 x: External clock or MTU clock A clock with a frequency 16 times the bit rate should be input on the SCKn pin. A clock signal with a frequency eight times the bit rate should be input when the SEMR.ABCS bit is set to 1. The SCKn pin is high-impedance when using the MTU clock. (Clock synchronous mode) b1 b0 0 x: Internal clock The SCKn pin functions as the clock output pin. 1 x: External clock The SCKn pin functions as the clock input pin.

Register	Bit	RX130 (SCIg, SCIh)	RX13T (SCIg, SCIh)
SEMR	ACS0	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock 1: Logical AND of two compare matches output from TMR (valid for SCI5, SCI6, and SCI12 only) Available compare match output varies among SCI channels.	Asynchronous mode clock source select bit (Valid only in asynchronous mode) 0: External clock 1: Logical AND of two compare matches output from MTU

Note: 1. Only when SCI5, SCI6, or SCI12 is selected.

2.19 I²C Bus Interface

Table 2.53 is a comparative overview of I²C bus interface.

Table 2.53 Comparative Overview of I²C Bus Interface

Item	RX130 (RIICa)	RX13T (RIICa)
Number of channels	1 channel	1 channel
Communication format	• I²C bus format or SMBus format • Selectable between master mode and slave mode • Automatic securing of set-up times, hold times, and bus-free times to match the specified transfer speed	• I²C bus format or SMBus format • Selectable between master mode and slave mode • Automatic securing of set-up times, hold times, and bus-free times to match the specified transfer speed
Transfer speed	Up to 400 kbps	Support for fast mode (up to 400 kbps)
SCL clock	Ability to select duty cycle of SCL clock within range of 4% to 96% during master operation	Ability to select duty cycle of SCL clock within range of 4% to 96% during master operation
Issuing and detecting conditions	• Automatic generation of start, restart, and stop conditions • Ability to detect start conditions (including restart conditions) and stop conditions	• Automatic generation of start, restart, and stop conditions • Ability to detect start conditions (including restart conditions) and stop conditions
Slave address	• Ability to set up to three slave addresses • Support for 7- and 10-bit address formats (along with use of both at once) • Ability to detect general call addresses, device ID addresses, and SMBus host addresses	• Ability to set up to three different slave addresses • Support for 7- and 10-bit address formats (along with use of both at once) • Ability to detect general call addresses, device ID addresses, and SMBus host addresses
Acknowledgment	• Automatic loading of acknowledge bit during transmission — Ability to suspend the next data transfer automatically on detection of a not-acknowledge bit • Automatic transmission of acknowledge bit during reception — Support for software control of value of the acknowledge bit according to the received data when a wait between the eighth and ninth clock cycles is selected	• Automatic loading of acknowledge bit during transmission — Ability to suspend the next data transfer automatically on detection of a not-acknowledge bit • Automatic transmission of acknowledge bit during reception — Support for software control of value of the acknowledge bit according to the received data when a wait between the eighth and ninth clock cycles is selected
Wait function	• Ability to implement a wait by holding the SCL clock signal low — Wait between the eighth and ninth clock cycles — Wait between the ninth and first clock cycles (WAIT function)	• Ability to implement a wait by holding the SCL clock signal low — Wait between the eighth and ninth clock cycles — Wait between the ninth and first clock cycles
SDA output delay function	Ability to delay output timing of transmitted data, including the acknowledge bit	Ability to delay output timing of transmitted data, including the acknowledge bit

Item	RX130 (RIICa)	RX13T (RIICa)
Arbitration	• Multi-master support — Ability to synchronize operation with the clock of another master in cases of conflict with the SCL clock — Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a start condition issuance conflict occurs — Ability to detect loss of arbitration when a start transmit data mismatch occurs during master operation • Ability to detect loss of arbitration due to start condition issuance when the bus is busy (to prevent issuance of duplicate start conditions) • Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a not-acknowledge bit is sent • Ability to detect loss of arbitration when a data mismatch occurs during slave transmission	• Multi-master support — Ability to synchronize operation with the clock of another master in cases of conflict with the SCL clock — Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a start condition issuance conflict occurs — Ability to detect loss of arbitration when a start transmit data mismatch occurs during master operation • Ability to detect loss of arbitration due to start condition issuance when the bus is busy (to prevent issuance of duplicate start conditions) • Ability to detect loss of arbitration in case of an SDA line signal state mismatch when a not-acknowledge bit is sent • Ability to detect loss of arbitration when a data mismatch occurs during slave transmission
Timeout detection function	Ability to detect extended stopping of the SCL clock using built-in time-out function	Ability to detect extended stopping of the SCL clock using built-in time-out function
Noise cancellation	Built-in digital noise filters for SCL and SDA signals, and ability to adjust the noise cancellation width by software.	Built-in digital noise filters for SCL and SDA signals, and ability to adjust the noise cancellation width by software.
Interrupt sources	Four sources • Communication error/event occurrence (AL detection, NACK detection, timeout detection, start condition (including restart condition) detection, or stop condition detection) • Receive data full (including match with slave address) • Transmit data empty (including match with slave address) • Transmission complete	Four sources • Communication error/event occurrence, arbitration detection, NACK detection, timeout detection, start condition (including restart condition) detection, or stop condition detection • Receive data full (including match with slave address) • Transmit data empty (including match with slave address) • Transmission complete
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state
RIIC operating modes	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode	Four modes: • Master transmit mode • Master receive mode • Slave transmit mode • Slave receive mode

Item	RX130 (RIICa)	RX13T (RIICa)
Event link function (output)	Four sources (RIIC0) • Communication error/event occurrence, arbitration detection, NACK detection, timeout detection, start condition (including restart condition) detection, or stop condition detection • Receive data full (including match with slave address) • Transmit data empty (including match with slave address) • Transmission complete	—

2.20 12-Bit A/D Converter

Table 2.54 is a comparative overview of the 12-bit A/D converters, Table 2.55 is a comparison of 12-bit A/D converter registers, and Table 2.56 is a comparison of A/D conversion start trigger settings in the ADSTRGR register.

Table 2.54 Comparative Overview of 12-Bit A/D Converters

Item	RX130 (S12ADE)	RX13T (S12ADF)
Number of units	1 unit	1 unit (S12AD)
Input channels	24 channels	S12AD: 8 channels
Extended analog function	Temperature sensor output, internal reference voltage	Internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	1.4 μs per channel (when A/D conversion clock ADCLK = 32 MHz)	1.4 μs per channel (when A/D conversion clock ADCLK = 32 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLK and A/D conversion clock ADCLK can be set so that the frequency ratio should be one of the following. PCLK to ADCLK frequency ratio = 1:1, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.
Data register	• 24 registers for analog input and one for A/D-converted data duplication in double trigger mode • One register for temperature sensor output • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.	• 8 registers for analog input, one for A/D-converted data duplication in double trigger mode, and two for A/D-converted data duplication during extended operation in double trigger mode • One register for internal reference • One register for self-diagnosis • The results of A/D conversion are stored in 12-bit A/D data registers. • 12-bit accuracy output for the results of A/D conversion • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes): The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register.

Item	RX130 (S12ADE)	RX13T (S12ADF)
Data register	—	• Extended operation in double trigger mode (available for specific triggers): A/D-converted analog input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.
Operating modes	• Single scan mode: — A/D conversion is performed only once on the analog inputs of up to 24 channels arbitrarily selected. — A/D conversion is performed only once on the temperature sensor output. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of up to 24 channels arbitrarily selected. • Group scan mode: — Analog inputs of up to 24 arbitrarily selected channels are divided into group A and group B, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A and group B, allowing A/D conversion of the groups to start at different times. • Group scan mode (when group A is given priority): — If a group A trigger is input during A/D conversion on group B, A/D conversion on group B is stopped and A/D conversion is performed on group A.	• Single scan mode: — A/D conversion is performed only once on the analog inputs of the arbitrarily selected channels. — A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of the arbitrarily selected. • Group scan mode: — The number of groups used is selectable between two (groups A and B) and three (groups A, B, and C). (When two is selected as the number of groups, only group A and group B may be used in combination.) — Analog inputs of arbitrarily selected channels are divided into group A and group B, or group A, group B, and group C, and A/D conversion of the analog inputs selected on a group basis is performed only once. — Conversion start conditions (synchronous trigger) can be selected independently for group A, group B, and group C, allowing A/D conversion of the groups to start at different times. • Group scan mode (when a group is given priority): — If a trigger is input for a higher-priority group during A/D conversion on a lower-priority group, A/D conversion on the lower-priority group is stopped and A/D conversion is performed on the higher-priority group. — The order of priority is group A (highest) > group B > group C (lowest).

Item	RX130 (S12ADE)	RX13T (S12ADF)
Operating modes	— Restart (rescan) of A/D conversion on group B after completion of A/D conversion on group A can be enabled.	— Restart (rescan) of A/D conversion on the lower-priority group after completion of A/D conversion on the higher-priority group can be enabled. In addition, rescan can be set to start from the first of the selected channels or from the channels on which A/D conversion has not yet finished.
Conditions for A/D conversion start	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU) or event link controller (ELC) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.	• Software trigger • Synchronous trigger Trigger by the multi-function timer pulse unit (MTU) • Asynchronous trigger A/D conversion can be triggered by the external trigger ADTRG0# pin.
Functions	• Variable sampling state count • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • 16 ring buffers when the compare function is used	• Channel-dedicated sample-and-hold function (three channels) • Input signal amplification function using programmable gain amplifier (three channels) • Variable sampling state count (independently settable for each channel) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan.	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan.

Item	RX130 (S12ADE)	RX13T (S12ADF)
Interrupt sources	• In group scan mode, an A/D scan end interrupt request (S12ADI0) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI0) can be generated on completion of double scan of group A, whereas A/D scan end interrupt request (GBADI) specially for group B can be generated on completion of group B scan. • The S12ADI and GBADI interrupts can activate the data transfer controller (DTC).	• In group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of group A scan, whereas an A/D scan end interrupt request (GBADI) for group B can be generated on completion of group B scan. A dedicated group C scan end interrupt request (GCADI) can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan of group A. A dedicated group B or dedicated group C scan end interrupt request (GBADI or GCADI) can be generated on completion of group B or group C scan, respectively. • The S12ADI, GBADI, and GCADI interrupts can activate the data transfer controller (DTC).
Event link function	• An ELC event is generated on completion of scans other than group B scan in group scan mode. • An ELC event is generated on completion of group B scan in group scan mode. • An ELC event is generated on completion of all scans. • Scan can be started by a trigger output by the ELC. • An ELC event is generated according to the event conditions of the window compare function in single scan mode.	—
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state

Table 2.55 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX130 (S12ADE)	RX13T (S12ADF)
ADDRy	—	A/D data register y (y = 0 to 7, 16 to 31)	A/D data register y (y = 0 to 7)
ADDBLDRA	—	—	A/D data duplication register A
ADDBLDRB	—	—	A/D data duplication register B
ADCSR	ADHSC	A/D conversion select bit	—
ADANSA1	—	A/D channel select register A1	—
ADANSB1	—	A/D channel select register B1	—
ADANSC0	—	—	A/D channel select register C0
ADADS1	—	A/D-converted value addition/ average channel select register 1	—

Register	Bit	RX130 (S12ADE)	RX13T (S12ADF)
ADEXICR	TSSAD	Temperature sensor output A/D converted value addition/average mode select bit	—
	TSSA	Temperature sensor output A/D conversion select bit	—
ADGCTRGR	—	—	A/D group C trigger select register
ADSSTRn	—	A/D sampling state register n (n = 0 to 7, L, T, O)	A/D sampling state register n (n = 0 to 7, O)
ADSHCR	—	—	A/D sample and hold circuit control register
ADELCCR	—	A/D event link control register	—
ADGSPCR	LGRRS	—	Restart channel select bit
ADCMPCR	—	A/D compare function control register	—
ADCMPANSR0	—	A/D compare function window A channel select register 0	—
ADCMPANSR1	—	A/D compare function window A channel select register 1	—
ADCMPANSER	—	A/D compare function window A extended input select register	—
ADCMPLR0	—	A/D compare function window A comparison condition setting register 0	—
ADCMPLR1	—	A/D compare function window A comparison condition setting register 1	—
ADCMPLER	—	A/D compare function window A extended input comparison condition setting register	—
ADCMPDR0	—	A/D compare function window A lower-side level setting register	—
ADCMPDR1	—	A/D compare function window A upper-side level setting register	—
ADCMPSR0	—	A/D compare function window A channel status register 0	—
ADCMPSR1	—	A/D compare function window A channel status register 1	—
ADCMPSER	—	A/D compare function window A extended input channel status register	—
ADHVREFCNT	—	A/D high-potential/low-potential reference voltage control register	—
ADWINMON	—	A/D compare function window A/B status monitor register	—
ADCMPBNSR	—	A/D compare function window B channel select register	—
ADWINLLB	—	A/D compare function window B lower-side level setting register	—
ADWINULB	—	A/D compare function window B upper-side level setting register	—
ADCMPBSR	—	A/D compare function window B channel status register	—
ADBUFn	—	A/D data storage buffer register n (n = 0 to 15)	—

Register	Bit	RX130 (S12ADE)	RX13T (S12ADF)
ADBUFEN	—	A/D data storage buffer enable register	—
ADBUFPTR	—	A/D data storage buffer pointer register	—
ADPGACR	—	—	A/D programmable gain amplifier control register
ADPGAGS0	—	—	A/D programmable gain amplifier gain setting register 0

Table 2.56 Comparison of A/D Conversion Start Trigger Settings in ADSTRGR Register

Bit	RX130 (S12ADE)	RX13T (S12ADF)
TRSB[5:0]	A/D conversion start trigger select bits for group B b5 b0 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 1: TRG0AN 0 0 0 0 1 0: TRG0BN 0 0 0 0 1 1: TRGAN 0 0 0 1 0 0: TRG0EN 0 0 0 1 0 1: TRG0FN 0 0 0 1 1 0: TRG4AN 0 0 0 1 1 1: TRG4BN 0 0 1 0 0 0: TRG4ABN 0 0 1 0 0 1: ELCTRG0	A/D conversion start trigger select bits for group B b5 b0 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN
TRSA[5:0]	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 0: ADTRG0# 0 0 0 0 0 1: TRG0AN 0 0 0 0 1 0: TRG0BN 0 0 0 0 1 1: TRGAN 0 0 0 1 0 0: TRG0EN 0 0 0 1 0 1: TRG0FN 0 0 0 1 1 0: TRG4AN 0 0 0 1 1 1: TRG4BN 0 0 1 0 0 0: TRG4ABN 0 0 1 0 0 1: ELCTRG0	A/D conversion start trigger select bits b13 b8 1 1 1 1 1 1: Trigger source deselection state 0 0 0 0 0 0: ADTRG0# 0 0 0 0 0 1: TRGA0N 0 0 0 0 1 0: TRGA1N 0 0 0 0 1 1: TRGA2N 0 0 0 1 0 0: TRGA3N 0 0 0 1 0 1: TRGA4N 0 0 1 0 0 0: TRG0N 0 0 1 0 0 1: TRG4AN 0 0 1 0 1 0: TRG4BN 0 0 1 0 1 1: TRG4AN or TRG4BN 0 0 1 1 0 0: TRG4ABN

2.21 D/A Converter / D/A Converter for Generating Comparator C Reference Voltage

Table 2.57 is a comparative overview of the D/A converters, and Table 2.58 is a comparison of D/A converter registers.

Table 2.57 Comparative Overview of D/A Converters

Item	RX130 (DAa)	RX13T (DA)
Resolution	8 bits	8 bits
Output channels	2 channels	1 channel
Measure against mutual interference between analog modules	Measure against interference between D/A and A/D conversion • D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal from the 12-bit A/D converter. Therefore, degradation of A/D conversion accuracy due to interference is reduced by controlling, by means of the enable signal, the timing of when the 8-bit D/A converter inrush current occurs.	—
Low power consumption function	Ability to transition to module stop state	Ability to transition to module stop state
Event link function (input)	D/A conversion on channel 0 can be started when an event signal is input.	—

Table 2.58 Comparison of D/A Converter Registers

Register	Bit	RX130 (DAa)	RX13T (DA)
DADRm	—	D/A data register m (m = 0 and 1)	D/A data register m (m = 0)
DACR	DAOE1	D/A output enable 1 bit	—
DADPR	—	DADRm format select register (m = 0 and 1)	Data register format select register
DAADSCR	—	D/A A/D synchronous start control register	—

2.22 Comparator B/Comparator C

Table 2.59 is a comparative overview of comparator B and comparator C, and Table 2.60 is a comparison of comparator B and comparator C registers.

Table 2.59 Comparative Overview of Comparator B and Comparator C Modules

Item	RX130 (CMPBa)	RX13T (CMPC)
Number of channels	2 channels (comparator B0, comparator B1)	3 channels (comparator C0 to comparator C2)
Analog input voltage	Input voltage to CMPBn pin (n = 0 and 1)	Input voltage to CMPCnm pin (n = channel number; m = 0 to 3)
Reference input voltage	Input voltage to CVREFBn pin or internal refalence voltage (n = 0 and 1)	Input voltage to CVREFC0 pin or on-chip D/A converter 0 output voltage
Comparison result	• Read from the CPBFLG.CPBnOUT flag (n = 0 and 1) • Comparison result can be output on CMPOBn pin (n = 0 and 1).	• The comparison result can be output externally.
Digital filter function	• Whether the digital filter is enabled or not, and the sampling frequency, are selectable.	• One of three sampling periods can be selected. • The filter function can also be disabled. • A noise-filtered signal can be used to generate interrupt request output and POE source output, and comparison results can be read from registers.
Interrupt request	• When comparator B0 comparison result changes • When comparator B1 comparison result changes	• An interrupt request is generated upon detection of a valid edge of the comparison result. • The rising edge, falling edge, or both edges of the comparison result can be selected as valid edges.
Timing of event generation to ELC	• When comparator B0 comparison result changes • When comparator B0 or comparator B1 comparison result changes	—
Selectable functions	• Window function Whether the window function is enabled or disabled (low-side reference (VRFL)) < CMPBn (n = 0 or 1) < high-side reference (VRFH)) can be selected. • Comparator B response speed Selectable between high-speed mode and low-speed mode.	—
Low power consumption function	Ability to specify module stop state	Ability to transition to module stop state

Table 2.60 Comparison of Comparator B and Comparator C Registers

Register	Bit	RX130 (CMPBa)	RX13T (CMPC)
CPBCNT1	—	Comparator B control register 1	—
CPBCNT2	—	Comparator B control register 2	—
CPBFLG	—	Comparator B flag register	—
CPBINT	—	Comparator B interrupt control register	—
CPBF	—	Comparator B filter select register	—
CPBMD	—	Comparator B mode select register	—
CPBREF	—	Comparator B reference input voltage select register	—
CPBOCR	—	Comparator B output control register	—
CMPCTL	—	—	Comparator control register
CMPSEL0	—	—	Comparator input switching register
CMPSEL1	—	—	Comparator reference voltage select register
CMPMON	—	—	Comparator output monitor register
CMPIOC	—	—	Comparator external output enable register

2.23 Data Operation Circuit

Table 2.61 is a comparative overview of data operation circuit.

Table 2.61 Comparative Overview of Data Operation Circuit

Item	RX130 (DOC)	RX13T (DOC)
Data operation functions	16-bit data comparison, addition, and subtraction	16-bit data comparison, addition, and subtraction
Low power consumption function	Ability to specify module stop state	Ability to specify module stop state
Interrupts	• When compared values either match or mismatch • When the result of data addition is greater than FFFFh • When the result of data subtraction is less than 0000h	• When compared values either match or mismatch • When the result of data addition is greater than FFFFh • When the result of data subtraction is less than 0000h
Event link function (output)	• When compared values either match or mismatch • When the result of data addition is greater than FFFFh • When the result of data subtraction is less than 0000h	—

2.24 RAM

Table 2.62 is a comparative overview of RAM.

Table 2.62 Comparative Overview of RAM

Item	RX130	RX13T
RAM capacity	Max. 48 KB	12 KB
RAM address	• RAM capacity 48 KB RAM0: 0000 0000h to 0000 BFFFh • RAM capacity 32 KB RAM0: 0000 0000h to 0000 7FFFh • RAM capacity 16 KB RAM0: 0000 0000h to 0000 3FFFh • RAM capacity 10 KB RAM0: 0000 0000h to 0000 27FFh	• RAM capacity 12 KB RAM0: 0000 0000h to 0000 2FFFh
Access	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.	• Single-cycle access is possible for both reading and writing. • On-chip RAM can be enabled or disabled.
Low power consumption function	Ability to specify module stop	Ability to specify module stop state for RAM0

2.25 Flash Memory

Table 2.63 is a comparative overview of flash memory.

Table 2.63 Comparative Overview of Flash Memory

Item	RX130	RX13T (FLASH)
Memory capacity	• User area: Up to 512 KB • Data area: 8 KB • Extra area: Stores the start-up area information, access window information, and unique ID	• User area: Up to 128 KB • Data area: 4 KB • Extra area: Stores the start-up area information, access window information, and unique ID
Addresses	• Products with capacity of 512 KB FFF8 0000h to FFFF FFFFh • Products with capacity of 384 KB FFFA 0000h to FFFF FFFFh • Products with capacity of 256 KB FFFC 0000h to FFFF FFFFh • Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh • Products with capacity of 64 KB FFFF 0000h to FFFF FFFFh	• Products with capacity of 128 KB FFFE 0000h to FFFF FFFFh • Products with capacity of 64 KB FFFF 0000h to FFFF FFFFh
Software commands	• The following software commands are implemented: Program, blank check, block erase, and unique ID read • The following commands are implemented for programming the extra area: Start-up area information program and access window information program	• The following software commands are implemented: Program, blank check, block erase, and unique ID read • The following commands are implemented for programming the extra area: Start-up area information program and access window information program
Value after erasure	• ROM: FFh • E2 DataFlash: FFh	• ROM: FFh • E2 DataFlash: FFh
Interrupt	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.	An interrupt (FRDYI) is generated upon completion of software command processing or forced stop processing.
On-board programming	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous communication. — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program.	• Boot mode (SCI interface) — Channel 1 of the serial communications interface (SCI1) is used for asynchronous communication. — The user area and data area can be programmed. • Boot mode (FINE interface) — The FINE interface is used. — The user area and data area can be programmed. • Self-programming (single-chip mode) — The user area and data area can be programmed using a flash programming routine in a user program.

Item	RX130	RX13T (FLASH)
Off-board programming	The user area and data area can be programmed using a flash programmer compatible with the MCU.	The user area and data area can be programmed using a flash programmer compatible with the MCU.
ID codes protection	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.	• Connection with a serial programmer can be controlled using ID codes in boot mode. • Connection with an on-chip debugging emulator can be controlled using ID codes.
Start-up program protection function	This function is used to safely program blocks 0 to 15.	This function is used to safely program blocks 0 to 15.
Area protection	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.	During self-programming, this function enables programming only of specified blocks in the user area and disables programming of the other blocks.
Background operation (BGO) function	Programs in the ROM can run while the E2 DataFlash is being programmed.	Programs in the ROM can run while the E2 DataFlash is being programmed.

2.26 Packages

As indicated in Table 2.64, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.64 Packages

Package Type	Renesas Code	
	RX130	RX13T
100-pin LFQFP	○	×
80-pin LFQFP	○	×
64-pin LQFP	○	×
64-pin LFQFP	○	×
32-pin LQFP	×	○
32-pin HWQFN	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 48-Pin Package

Table 3.1 is a comparative listing of the pin functions of 48-pin package products.

Table 3.1 Comparative Listing of 48-Pin Package Pin Functions

48-Pin	RX130 (48-Pin LFQFP/HWQFN)	RX13T (48-Pin LFQFP/HWQFN)
1	VCL	VCL
2	MD/FINED	MD/FINED
3	RES#	RES#
4	XTAL/P37	XTAL/P37
5	VSS	VSS
6	EXTAL/P36	EXTAL/P36
7	VCC	VCC
8	P35/NMI	PE2/POE10#/NMI/IRQ0
9	P31/MTIOC4D/TMCI2/CTS1#/RTS1#/SS1#/TS1/IRQ1	PD6/MTIOC0D/CTS1#/RTS1#/SS1#/IRQ5/ADST0
10	P30/MTIOC4B/TMRI3/POE8#/RXD1/SMISO1/SSCL1/TS2/IRQ0	PD5/MTIOC0C/RXD1/SMISO1/SSCL1/IRQ3
11	P27/MTIOC2B/TMCI3/SCK1/TS3	PD4/MTIOC0B/SCK1/IRQ2
12	P26/MTIOC2A/TMO1/TXD1/SMOSI1/SSDA1/TS4	PD3/MTIOC0A/TXD1/SMOSI1/SSDA1
13	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/SCK1/MISOA/SDA0/IRQ7	PB7/MTIOC3C/MTCLKD/RXD1/SMISO1/SSCL1/RXD5/SMISO5/SSCL5/IRQ5
14	P16/MTIOC3C/MTIOC3D/TMO2/TXD1/SMOSI1/SSDA1/MOSIA/SCL0/IRQ6/ADTRG0#	PB6/MTIOC1B/MTIOC3A/TXD1/SMOSI1/SSDA1/TXD5/SMOSI5/SSDA5
15	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/SMISO1/SSCL1/TS5/IRQ5	PB5/ADTRG0#
16	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/RTS1#/SS1#/TS6/IRQ4	PB4/POE8#/IRQ3
17	PH3/TMCI0/TS7	PB3/MTIOC0A/CACREF/SCK5/SCK12
18	PH2/TMRI0/TS8/IRQ1	PB2/MTIOC0B/MTCLKC/ADSM0/TXD5/SMOSI5/SSDA5/SDA0
19	PH1/TMO0/TS9/IRQ0	PB1/MTIOC0C/MTIC5W/MTCLKA/RXD5/SMISO5/SSCL5/SCL0/IRQ2
20	PH0/TS10/CACREF	PB0/MTIOC0D/MTIOC2A/MTCLKB/TXD12/TXDX12/SIOX12/SMOSI12/SSDA12
21	PC7/MTIOC3A/TMO2/MTCLKB/MISOA/TS13/CACREF	PA3/MTIOC1B/MTIOC2A/CTS12#/RTS12#/SS12#
22	PC6/MTIOC3C/MTCLKA/TMCI2/MOSIA/TS14	PA2/MTIOC1A/MTIOC2B/CTS5#/RTS5#/SS5#/IRQ4
23	PC5/MTIOC3B/MTCLKD/TMRI2/RSPCKA/TS15	P94/MTIOC2B/MTIC5U/MTCLKA/RXD12/RXDX12/SMISO12/SSCL12/IRQ1
24	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/SCK5/SSLA0/TSCAP	P93/MTIOC1A/MTIC5V/SCK5/SCK12/IRQ0/ADTRG0#
25	PB5/PC3*1/MTIOC2A/MTIOC1B/TMRI1/POE1#/TS20	P76/MTIOC4D

48-Pin	RX130 (48-Pin LFQFP/HWQFN)	RX13T (48-Pin LFQFP/HWQFN)
26	PB3/PC2*1/MTIOC0A/MTIOC4A/TMO0/POE3#/SCK6/TS22	P75/MTIOC4C
27	PB1/PC1*1/MTIOC0C/MTIOC4C/TMCI0/TXD6/SMOSI6/SSDA6/TS24/IRQ4/CMPOB1	P74/MTIOC3D
28	VCC	P73/MTIOC4B
29	PB0/PC0*1/MTIC5W/RXD6/SMISO6/SSCL6/RSPCKA/TS25	P72/MTIOC4A
30	VSS	P71/MTIOC3B
31	PA6/MTIC5V/MTCLKB/TMCI3/POE2#/CTS5#/RTS5#/SS5#/MOSIA/TS26	P70/POE0#/IRQ5
32	PA4/MTIC5U/MTCLKA/TMRI0/TXD5/SMOSI5/SSDA5/SSLA0/TS28/IRQ5/CVREFB1	VCC
33	PA3/MTIOC0D/MTCLKD/RXD5/SMISO5/SSCL5/TS29/IRQ6/CMPB1	VSS
34	PA1/MTIOC0B/MTCLKC/SCK5/SSLA2/TS31	P24/MTIC5U/RXD5/SMISO5/SSCL5/IRQ3/COMP0
35	PE4/MTIOC4D/MTIOC1A/TS33/AN020/CMPA2/CLKOUT	P23/MTIC5V/CACREF/TXD5/SMOSI5/SSDA5/IRQ4/COMP1
36	PE3/MTIOC4B/POE8#/CTS12#/RTS12#/TS34/AN019/CLKOUT	P22/MTIC5W/IRQ2/COMP2
37	PE2/MTIOC4A/RXD12/RXDX12/SSCL12/TS35/IRQ7/AN018/CVREFB0	P47*2/AN007/CMPC13
38	PE1/MTIOC4C/TXD12/TXDX12/SIOX12/SSDA12/AN017/CMPB0	P46*2/AN006/CMPC03
39	P47*2/AN007	P45*2/AN005/CMPC22
40	P46*2/AN006	P44*2/AN004/CMPC12
41	P45*2/AN005	P43*2/AN003/CMPC02
42	P42*2/AN002	P42*2/AN002/CMPC20
43	P41*2/AN001	P41*2/AN001/CMPC10
44	VREFL0/PJ7*2	P40*2/AN000/CMPC00
45	P40*2/AN000	AVCC0
46	VREFH0/PJ6*2	AVSS0
47	AVCC0	P11/MTIOC3A/MTCLKA/POE8#/IRQ1/CVREFC0
48	AVSS0	P10/MTCLKB/IRQ0

Notes: 1. On the RX130 Group PC0 to PC3 are enabled only when the port switching function is selected.
2. The power supply of the I/O buffer for these pins is AVCC0.

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX13T Group and the RX130 Group. 4.1, Notes on Functional Design, presents information regarding the software.

4.1 Notes on Functional Design

Some software that runs on the RX130 Group is compatible with the RX13T Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX13T Group and RX130 Group are as follows:

For differences between modules and functions, refer to 2, Comparative Overview of Specifications. For further information, refer to the User's Manual: Hardware of each MCU group, listed in 5, Reference Documents.

4.1.1 Exception Vector Table

On the RX130 Group the vector addresses are relocatable using the value set in the exception table register (EXTB) as the start address, but addresses allocated in the vector table are fixed on the RX13T Group.

4.1.2 Port Direction Register (PDR) Initialization

PDR register initialization differs even between products with the same pin count.

4.1.3 PB1 Pin Input Level

On the RX13T Group the input level of the PB1 pin is TTL when the SCL function is selected by PB1PFS.PSEL and SMBus is selected by the ICMR3.SMBS bit in the RIIC. Therefore, the input level of both PB1 port reads and IRQ2 is TTL.

4.1.4 MTIOC Pin Output Level when Counter Operation Stopped

During operation with the MTIOC pin in the output state, writing 0 to the CSTn bit in TSTRA or TSTR causes counter operation to stop. At this point, in complementary PWM mode or reset-synchronized PWM mode on the RX13T Group, the initial output level set in the TOCR1A or TOCR2A register is output on the MTIOC pin.

In other than complementary PWM mode or reset-synchronized PWM mode, the output compare output level is maintained on the MTIOC pin.

4.1.5 Conversion Start Requests in Complementary PWM Mode

In complementary PWM mode on the RX13T Group, compare match detection to generate PWM waveforms is performed not only between MTU4.TGRA and MTU4.TCNT, but MTU3.TCNT or TCNTSA as well. Therefore, TRGA4N is also generated when a compare match occurs with MTU3.TCNT or TCNTSA.

To generate A/D conversion start requests when MTU3 or MTU4 is operating in complementary PWM mode, use A/D conversion start request generation by compare match between MTU4.TCNT and MTU4.TADCORA or MTU4.TADCORB.

4.1.6 Pulse Width of Count Clock Source

The pulse width of the MTU's count clock source differs between the RX130 Group and the RX13T Group. Refer to Table 4.1 for details. Note that using a pulse width less that that listed below can interfere with correct operation.

Table 4.1 Comparison of Pulse Width of Count Clock Source

Item		RX130	RX13T
Single edge		1.5 PCLK or more	3 PCLKB or more
Both edges		2.5 PCLK or more	5 PCLKB or more
Phase counting mode	Phase difference, overlap	1.5 PCLK or more	3 PCLKB or more
	Pulse width	2.5 PCLK or more	5 PCLKB or more

4.1.7 High-Impedance Control when MTU Pins Deselected

On the RX13T Group, when high-impedance control is enabled for MTU pins in the POECR1 or POECR2 register and the control condition is met, the MPU function drives the output of multiplexed pins high-impedance, regardless of whether the MPU function is selected or not.

4.1.8 A/D Scan Conversion End Interrupt Generation

On the RX13T Group, when a scan is started by a software trigger and the ADCSR.ADIE bit has been set to 1, an A/D scan conversion end interrupt is generated when the scan ends, even if double trigger mode is selected.

4.1.9 A/D Conversion Start Trigger in Group Scan Mode

On the RX130 Group it is not possible to use an asynchronous trigger as the group A A/D conversion start trigger in group scan mode, but on the RX13T Group it is possible to use an asynchronous trigger for this purpose.

4.1.10 A/D Conversion Start Bit

On the RX13T Group, when using single scan continuous mode (ADGSPCR.GBRP bit = 1) while the 12-bit A/D converter's group priority operation mode is enabled (ADCSR.ADCS[1:0] bits = 01b and ADGSPCR.PGS bit = 1), the value of the ADCSR.ADST bit is maintained as 1.

4.1.11 Scan Conversion Time of 12-bit A/D Converter

The scan conversion time differs between the RX130 Group and RX13T Group. The scan conversion time (t_{SCAN}) for the two groups of a single scan where the number of selected channels is n is expressed by the equations below. For details, refer to the description of the 12-bit A/D converter analog input sampling time and scan conversion time in the User's Manual: Hardware of the RX130 Group and RX13T Group, listed in 5, Reference Documents.

RX130: $t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

RX13T: $t_{SCAN} = t_D + t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

t_D: Scan conversion start delay time

t_{SPLSH}: Channel-dedicated sample and hold circuit processing time

t_{DIS}: Disconnection detection assistance processing time

t_{DIAG}: Self-diagnostic conversion time

t_{CONV}: A/D conversion processing time

t_{ED}: Scan conversion end delay time

4.1.12 D/A Converter Settings

On the RX13T Group when using the D/A converter output as the reference input voltage of the comparator, C make sure to make D/A converter settings and wait for the D/A converter output to stabilize (D/A conversion time: t_{DCONV}) before enabling comparator C operation. When changing D/A converter settings, first stop comparator operation before making setting changes, and wait for the D/A converter output to stabilize before enabling comparator operation again.

4.1.13 Comparator

The comparator registers on the RX13T Group differ significantly from those on the RX130 Group. Note that this reduces software compatibility.

4.1.14 Comparator C Operation in Module Stop State

On the RX13T Group the analog circuits of comparator C do not stop operating if a transition to the module stop state is made while comparator C is operating, so the analog power current associated with comparator C remains unchanged. If it is necessary to reduce analog power current consumption in the module stop state, stop operation of comparator C by clearing the CMPCTL.HCMPON bit to 0.

4.1.15 Comparator C Operation in Software Standby Mode

On the RX13T Group the analog circuits of comparator C do not stop operating if a transition to software standby mode is made while comparator C is operating, so the analog power current associated with comparator C remains unchanged. If it is necessary to reduce analog power current consumption in software standby mode, stop operation of comparator C by clearing the CMPCTL.HCMPON bit to 0.

4.1.16 Comparator C Operation with 12-Bit A/D Converter in Module Stop State

On the RX13T Group the programmable gain amplifier (PGA) and 12-bit A/D converter are controlled by the same module stop signal, so comparison of the following PGA outputs is not possible while the 12-bit A/D converter is in the module stop state:

- PGA output on AN000 pin
- PGA output on AN001 pin
- PGA output on AN002 pin

The following analog pins are connected to the comparator directly, so comparison is possible even when the 12-bit A/D converter is in the module stop state:

- AN000 pin
- AN001 pin
- AN002 pin
- AN003 pin
- AN004 pin
- AN005 pin
- AN006 pin
- AN007 pin

5. Reference Documents

User's Manual: Hardware

RX130 Group User's Manual: Hardware Rev.3.00 (R01UH0560EJ0300)
(The latest version can be downloaded from the Renesas Electronics website.)

RX13T Group User's Manual: Hardware Rev.1.00 (R01UH0822EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News

(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

There are no applicable technical updates.

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	Apr. 7, 2020	—	First edition issued
1.10	Nov. 5, 2021	74	2.26 Table 2.64 Packages revised
		75	Table 3.1 Comparative Listing of 48-Pin Package Pin Functions expressions revised

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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