Application Note

DA1469x Application Hardware Design Guidelines

AN-B-066

Abstract

This document provides the minimal reference schematic, circuit explanation, and design guidelines for Bluetooth® Low Energy applications based on the SoC of DA1469x family.

DA1469x Application Hardware Design Guidelines

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1 Terms and Definitions

ADC	Analog-to-Digital Converter
BOD	Brown-Out Detection
CS	Chip Select
DCDC	DC/DC (buck) Converter
DK PRO	PRO Development Kit
GPIO	General Purpose Input Output
JEITA	Japan Electronics and Information Technology Industries Association
LDO	Low Dropout (voltage regulator)
MAC	Media Access Controller
OTP	One-Time Programmable
OVP	Over-Voltage Protection
PCB	Printed Circuit Board
PDC	Power Domain Controller
PMU	Power Management Unit
PTH	Plated Through-Hole
PWM	Pulse Width Modulation
SDK	Software Development Kit
SIMO	Single Inductor Multiple Outputs (DCDC converter type)
SoC	System on Chip
QSPI	Quad Serial Peripheral Interface
RDC	DC Resistance
SDADC	Sigma-Delta ADC
SRAM	Static Random-Access Memory
SWD	Serial Wire Debug
UART	Universal Asynchronous Receiver/Transceiver
USB	Universal Serial Bus
VFBGA	Very thin profile Fine-pitch Ball Grid Array (chip package)

2 References

[1] DA1469x, Datasheet, Dialog Semiconductor

[2] AN-B-027, Designing Printed Antennas for Bluetooth Low Energy, Application Note, Dialog Semiconductor

[3] UM-B-093, DA1469x PRO Development Kit, User Manual, Dialog Semiconductor

[4] IPC/JEDEC J-STD-020E (http://www.jedec.org)

3 Introduction

The DA1469x is a family of multi-core wireless microcontrollers combining the newest Arm® Cortex®-M33 application processor with floating point unit, advanced power management functionality, a cryptographic security engine, analog and digital peripherals, a dedicated sensor node controller and a software configurable protocol engine (based on the Arm® Cortex®-M0+ processor) accompanied by a radio compliant to the Bluetooth® Low Energy 5.1 standard.

The application processor executes code from the embedded memory (RAM) or an external QSPI Flash via a 16 kB 4-way associative cache controller, which is capable of on-the-fly decrypting without extra wait states. Sensor node controller allows sensor node operations and data acquisition without CPU intervention.

Bluetooth® Low Energy connectivity is achieved by a new software-configurable Bluetooth® Low Energy protocol engine (MAC) with an ultra-low-power radio transceiver which is capable of +6 dBm output power, -97 dBm sensitivity, offering a total link budget of 103 dB.

An advanced power management unit provides the capability to run from primary and secondary batteries and to supply external devices through the integrated SIMO DCDC and integrated LDOs. The JEITA-compliant charger allows rechargeable batteries to be charged over USB.

The differentiation between the members of the DA1469x product family is presented in Table 1.

The DA14693, the automotive qualified SoC, is treated in a dedicated application note.

Table 1: DA1469x Product Family Differentiation

Features	DA14691	DA14695	DA14697	DA14699
Available RAM	384 kB	512 kB	512 kB	512 kB
Charger	x	√	√	√
LCD Controller	x	√	√	√
LEDs	x	x	√	√
QSPI RAM Controller	x	√	√	√
Motor Controller	x	x	x	√
GPIOs	44	44	55	55
USB	√	√	√	√
Audio (processing unit)	√	√	√	√
Rest of the features	√	√	√	√

There are two available packages for the DA1469x: VFBGA100 and VFBGA86, Figure 1. The VFBGA100 package is available for the DA14699 and the DA14697, whereas the VFBGA86 is used for the DA14691 and the DA14695. See Table 2.

Table 2: DA1469x Family Chip Options

Chip	Package	Number of Pins	Size (mm)	Ordering Information
DA14691	VFBGA86	86	6 × 6 × 0.9	DA14691-00000HQ2
DA14695	VFBGA86	86	6 × 6 × 0.9	DA14695-00000HQ2
DA14697	VFBGA100	100	5 × 5 × 0.9	DA14697-00000HR2
DA14699	VFBGA100	100	5 × 5 × 0.9	DA14699-00000HR2

The purpose of this document is to present the minimum necessary circuit required for a proper operation of the DA1469x, so that system designers can build their Bluetooth® LE products or

applications using the DA1469x SoC. Recommended schematics, chip interfaces, surrounding components, and PCB layout guidelines of the DA1469x SoC family are covered in this document.

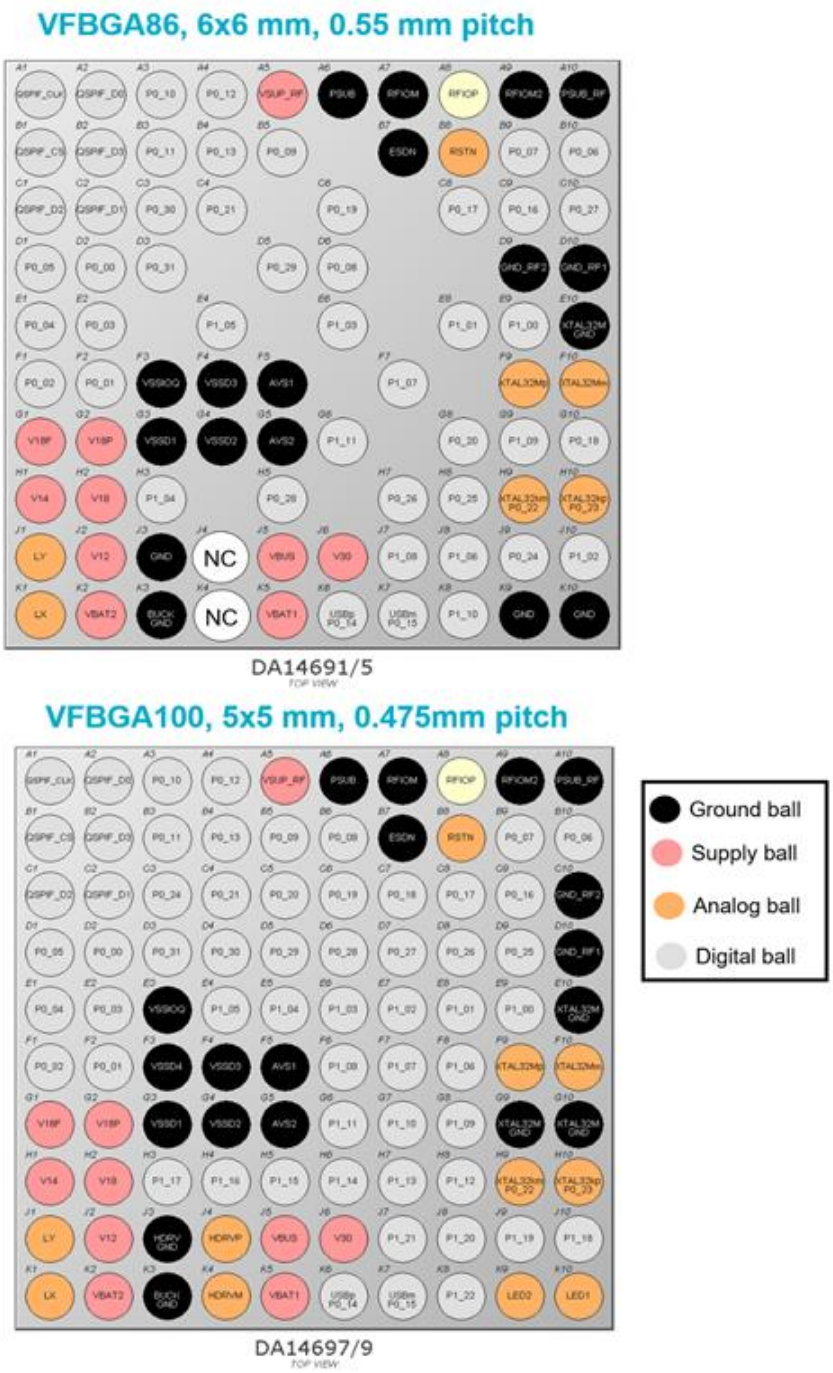


Figure 1: DA1469x Packages Comparison

4 Device Revision Numbering and Marking

The revision number of the chip can be read from the device by reading the Arm Cortex-M33 registers in Table 3 and Table 4. The chip's commercial version number is a combination of such information and can be read from Table 5.

Table 3: CHIP_REVISION_REG (0x50040214)

Bit	Mode	Symbol	Description	Reset
7:0	R	CHIP_REVISION	Chip version, corresponds with type number in ASCII 0x41 = 'A', 0x42 = 'B'.	-

Table 4: CHIP_TEST1_REG (0x500402F8)

Bit	Mode	Symbol	Description	Reset
7:0	R	CHIP_LAYOUT_REVISION	Chip layout version, corresponds with type number in ASCII	-

Table 5: Chip Revision Numbering

Commercial Number	CHIP_REVISION_REG (0x50040214)	CHIP_TEST_REG (0x500402f8)
DA14691-00 DA14695-00	0x41 (A) 0x41 (A)	0x42 (B) 0x42 (B)
DA14697-00 DA14699-00	0x41 (A) 0x41 (A)	0x42 (B) 0x42 (B)

5 Minimal Design for DA1469x SoC

The DA1469x SoC requires a minimum number of external components for a proper operation. The necessary sections required for the minimal system operation are:

- Power section
- Crystals
- UART
- JTAG
- Radio section
- Flash memory

The block diagram of the DA1469x minimal design and the basic schematics for the two packages, VFBGA100 and VFBGA86, are presented in Figure 2, Figure 3, and Figure 4 respectively.

Optional extra functionalities like GPIOs, LEDs, and Haptic have been added to indicate the main differences between the two packages on an application level: Figure 2.

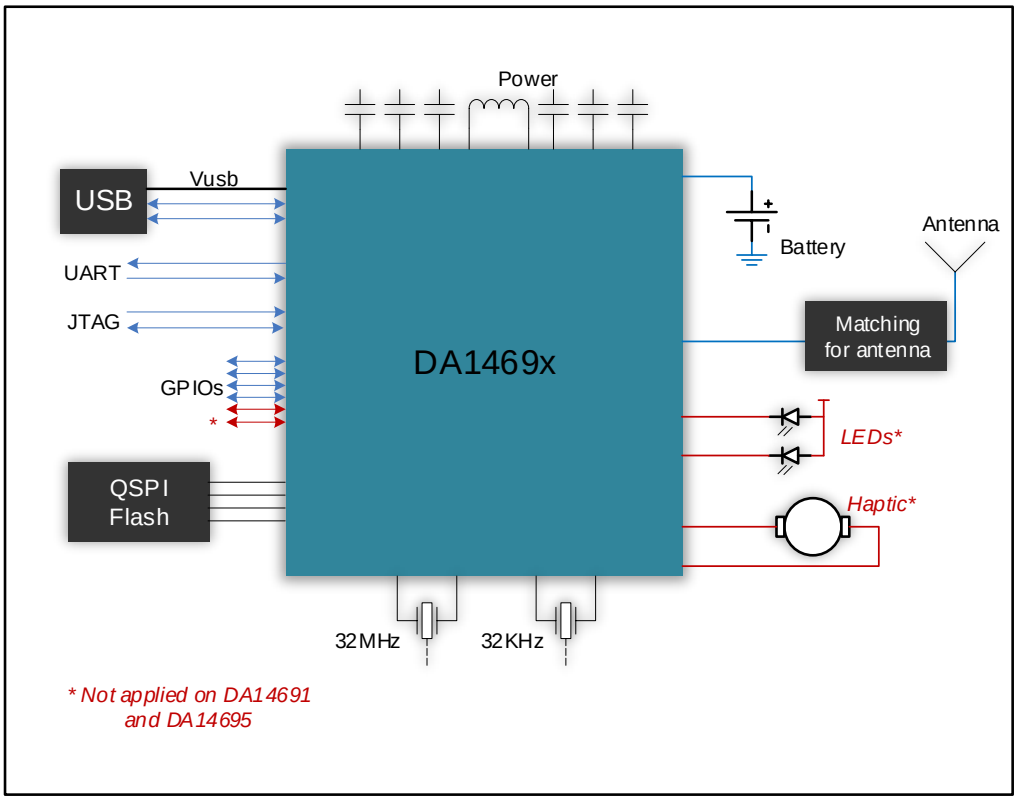


Figure 2: Block Diagram of DA1469x Minimal Design

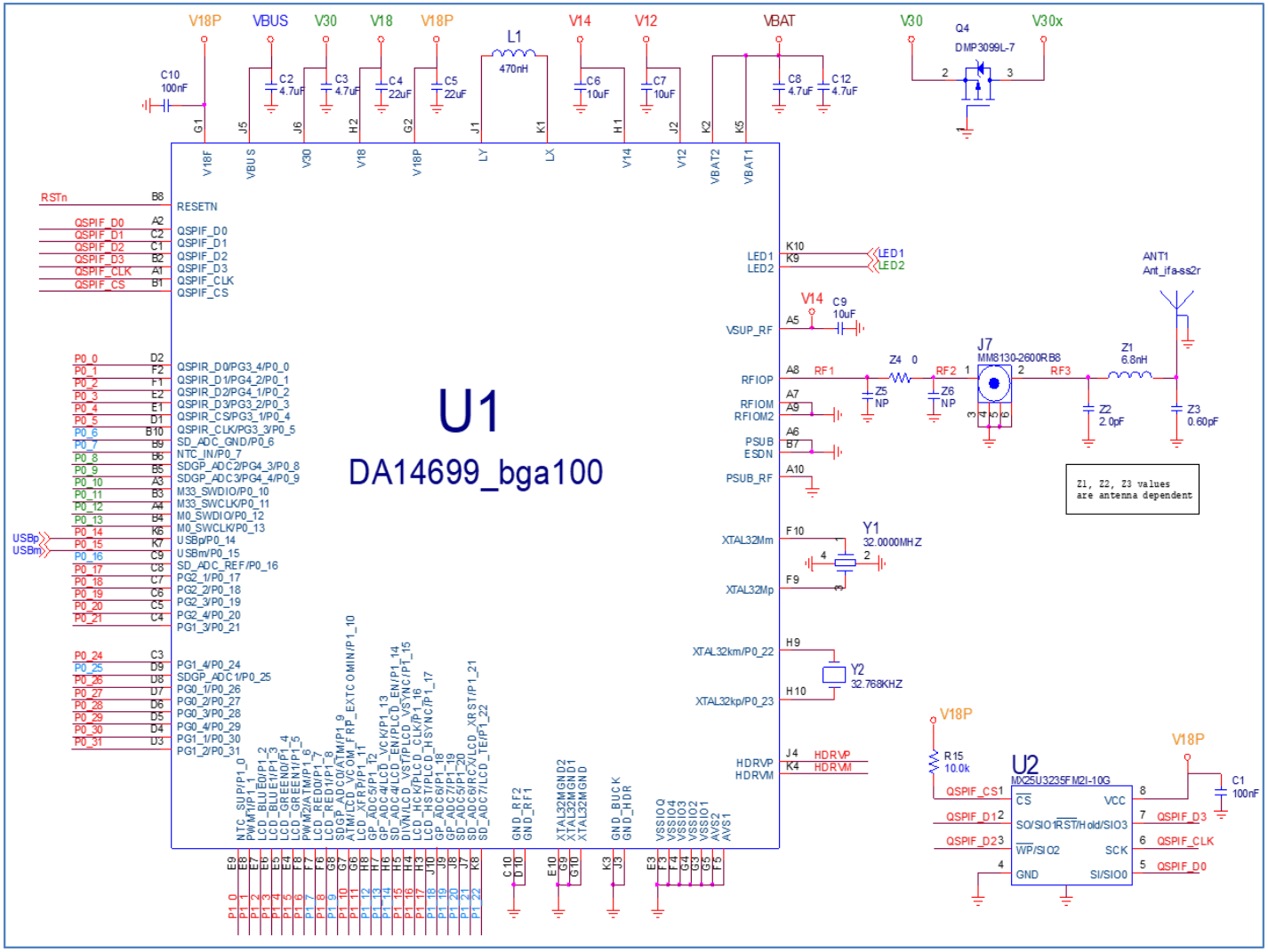


Figure 3: Minimal Design for VFBGA100 Package

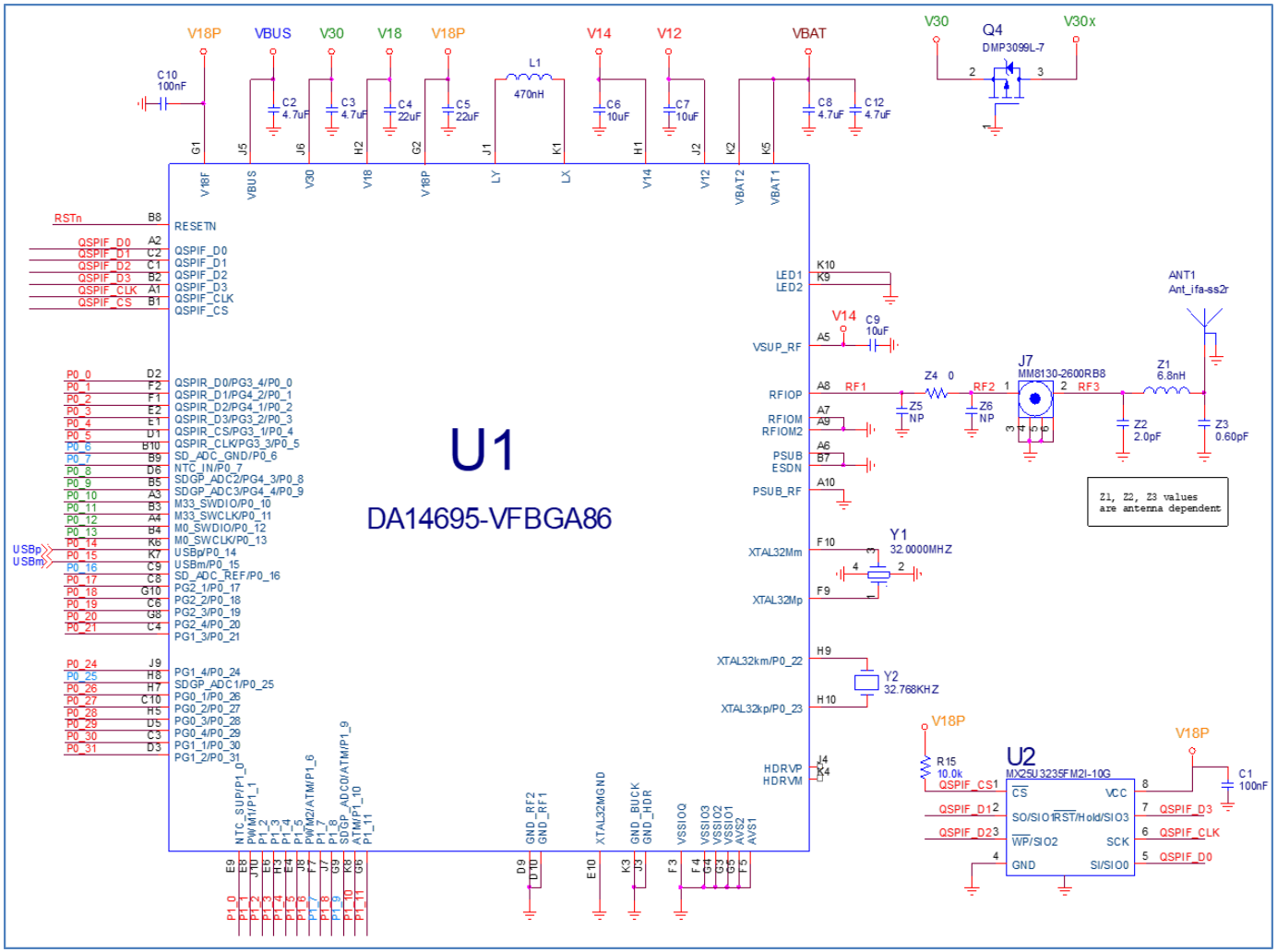


Figure 4: Minimal Design for VFBGA86 Package

5.1 Power Section of DA1469x

There are three main power inputs, namely, VBUS, VBAT1, and VBAT2. The VBUS is connected when a battery is being charged through the USB connector. VBAT1 should be shorted with VBAT2 externally and supplies the LDOs, while VBAT2 supplies the SIMO DCDC converter.

There are certain parts of the power management unit (PMU) which are always powered. They are marked red in Figure 5. The always-on power circuitry consists of two clamps and LDO_SLEEP, which provides the necessary voltage when the system is in extended sleep, deep sleep, or hibernation mode. When the system wakes up, many of the PMU blocks are activated automatically (in green). Finally, software is responsible for activating the SIMO DCDC and the blocks marked in black in Figure 5.

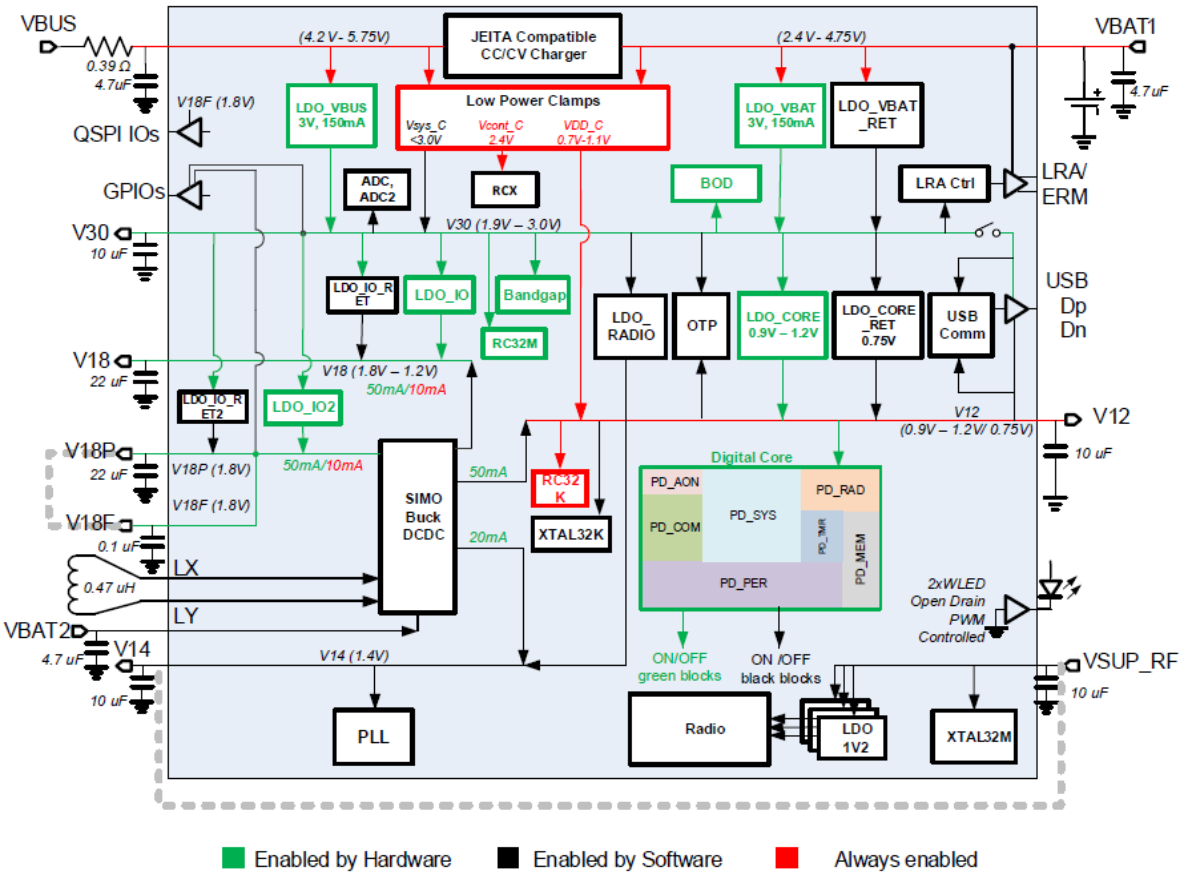


Figure 5: DA1469x Power Management Unit Block Diagram

Note that, all the capacitor values in above Figure 5 are the nominal, rated values. When a power source is available on the VBUS pin, the DA1469x system is supplied by the LDO_VBUS. This is independent on whether a battery is connected to the VBAT pin, unless the VBUS voltage drops below 4 V and the VBAT voltage is higher than the VBUS voltage.

The DA1469x SoC contains internally all power management for proper and safe system operation. Figure 6 shows the required external components, like the decoupling capacitors and the power inductor.

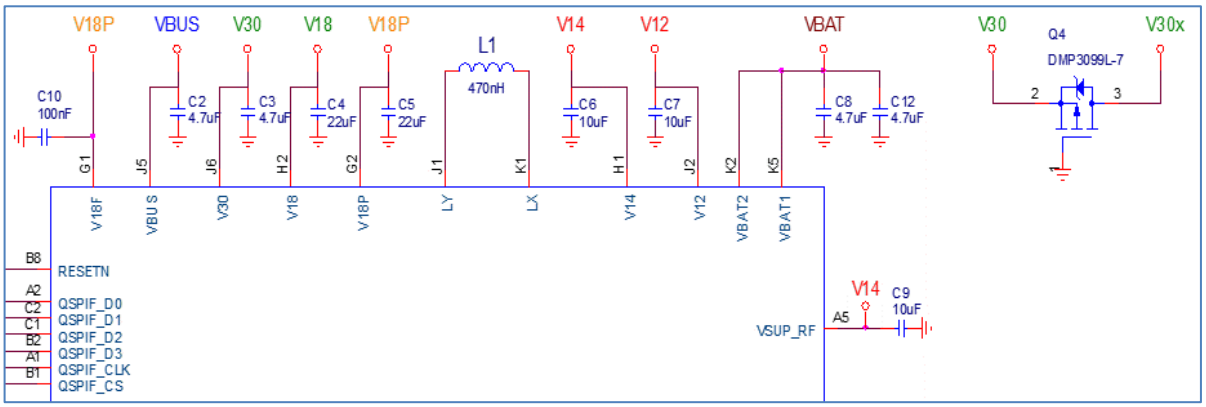


Figure 6: Power Section of DA1469x SoC

VBUS: This is the JEITA-compatible, battery constant current/constant voltage (CC/CV) charger input as well as the USB bus voltage. It supplies the 3 V LDO (LDO_VBUS), providing power to the V30 rail. As the USB power input, a decoupling capacitor of 10 µF maximum must be placed close to the VBUS pin. The absolute maximum operating voltage for the VBUS pin is 6.5 V.

A significant challenge on product level that designers need to deal with is the use of commercially available chargers for charging. The output voltage of these chargers can be as high as 20 V! To prevent damages to the DA1469x SoC or other low voltage system components, the addition of an external over-voltage protection (OVP) circuit is recommended (see Section 5.10.3). The DK Pro daughterboard uses a discrete OVP circuit. A ceramic capacitor of 4.7 µF/10 V (C2) should be placed as close as possible to the VBUS pin of DA1469x SoC. To avoid an unnecessary voltage drop in the VBUS supply, it's advised to not use a series resistor in the VBUS line when having an OVP circuit.

In a standard USB topology (no OVP circuit) though, it is strongly advised to apply a 10 µF/10 V capacitor (location C2) and a 0.39 Ω resistor in series with the VBUS pin for cable damping and limiting the inrush current: Figure 18. For the theory behind this, see Section 5.10.2.

VBAT1: The battery is connected to this pin and supplies the 3 V VBAT LDO. A 4.7 µF/10 V decoupling capacitor (C8) is required to be placed close to the pin (0402 package). The voltage range for VBAT1 is 2.4 V to 4.75 V.

VBAT2: This is the input supply pin for the SIMO DCDC buck converter. VBAT2 must be connected externally to **VBAT1** (Figure 6). A 4.7 µF/10 V decoupling capacitor (C12) is required to be placed near the VBAT2 pin (0402 package).

V30: This is the 3 V LDO output rail with programmable output of 3.0 V (default), 3.3 V or 3.45 V. It is supplied by the VBAT1 or the VBUS pin. A ceramic X5R decoupling capacitor having a rated value of at least 4.7 µF/10 V (C3) should be present (0402 package). The V30 voltage rail can deliver up to 150 mA in active mode and maximum 10 mA in sleep mode. When the GPIOs are set to the 3 V supply, they are supplied by this V30 rail. The V30 rail may not and cannot be turned off because it is supplying some essential system blocks (e.g. bandgap) and the retention LDOs.

SIMO DCDC buck converter: Its outputs when active are V18P, V18, V14, and V12. The inductor needed for the DCDC operation is connected externally. The inductor L1 (470 nH) having a low DC resistance, is connected to the LX/ LY pins. Preferably the inductor should be a shielded type.

V18 and V18P: These supply rails can deliver power to external devices, even when the system is in sleep mode. The ceramic decoupling capacitors C4 and C5 (22 µF/6.3 V in 0603 package) must be placed as close as possible to the V18 and the V18P pins. The V18 rail may be used for supplying external devices like sensors or a RF power amplifier. The V18P rail is used to supply the GPIOs when these are set to 1.8 V. The V18P rail also delivers 1.8 V to the **V18F** rail, through an internal MOSFET switch, which is supplying the external QSPI FLASH and the QSPI I/Os connected to the FLASH. The current delivery capability of the V18 and V18P power rails is 50 mA in active mode and 10 mA in sleep mode. The latter is handled by the 1.8 V retention LDOs (LDO_IO_RET(2)). Note that, the V18P and V18 power rails can be turned off when not being used.

V18F: This is the QSPI Flash supply and the QSPI interface voltage from the **V18P** rail through an internal switch. As this MOSFET switch may present a high resistance at higher temperatures, it is advised to short the V18P and V18F rails externally, bypassing the internal switch (Figure 5). The decoupling capacitor C10 (100 nF) at the V18F pin may be omitted after shorting the V18F pin and the adjacent V18P pin on the PCB and placing C5 (22 µF) close to the V18F pin. A 100 nF decoupling capacitor (C1 in Figure 3, Figure 4) near the Flash supply pin is required.

V12: This power rail supplies the digital core of the DA1469x and delivers up to 50 mA at 1.2 V when in active mode. This rail should not be used for supplying external devices. A 4.7 µF/10 V decoupling capacitor (C7) is required (0402 package).

V14: This supply rail delivers up to 20 mA at 1.4 V and should not be used for supplying external devices. This rail connects to **VSUP_RF** (radio supply). A 10 µF/6.3 V decoupling capacitor (C6) is required to be placed close to the V14 pin.

VSUP_RF (V14_RF): The radio supply pin. VSUP_RF must be connected to the **V14** rail externally (Figure 5) and it powers the RF circuits via several dedicated internal LDOs. A 10 µF/6.3 V decoupling capacitor (C9) is required to be placed as close to the VSUP_RF pin as possible for the best and most stable RF performance.

Table 6: Suggested Decoupling Capacitors for the Power Section

Reference	Description	Value	Package, height	Part Number
C2, C3, C8, C12	CAP CER ±20% 10 V X5R	4.7 µF	1005M, H 0.6 mm	GRM155R61A475MEAAD
C6, C7, C9	CAP CER ±20% 6.3 V X5R	10 µF	1005M, H 0.7 mm	GRM155R60J106ME15D
C4, C5 (V18/P)	CAP CER ±20% 6.3 V X5R	22 µF	1608M, H 1.0 mm	GRM188R60J226MEA0D
C1, C10 (V18F)	CAP CER 6.3 V	100 nF	1005M (0402)	not critical, e.g. muRata GCM155R71C104KA55D

The ceramic capacitors are to be placed as close as possible to the pins of the chip to reduce the parasitic inductance and to improve performance. If available, a small package (0402) is used.

The selected capacitor values and working voltages are higher than the required ones because of the capacitance derating phenomenon when a DC bias voltage is applied to the ceramic capacitor.

The capacitance de-rating is highly dependent on the rated voltage, the dielectric type (for example, X5R vs. X7R) and the size of the multi-layer ceramic capacitor. Figure 7 presents the capacitance de-rating for two different packages, 0402 and 0603, of a 4.7 µF/6.3 V/X5R muRata ceramic capacitor. Similar differences can be observed for a 0402 sized 4.7 µF/X5R capacitor with rated voltage of 6.3 V or 10 V: the effective capacitance values at 5 V are 1 µF and 2 µF respectively. To compensate or reduce the negative effect of this DC-bias de-rating, it is advised to apply either a capacitor having a larger size (0603 instead of 0402), a type with a higher rated voltage (10 V instead of 6.3 V), or just a capacitor with a larger nominal capacitance value.

To achieve an effective capacitance value of at least 10 µF on the V18P/V18 voltage rails, the chosen capacitance needs to be of a much higher nominal value, for example, 22 µF/6.3 V (Figure 8).

Finally, to complete the system, a 470 nH power inductor is used for the SIMO DCDC buck converter. The DC resistance affects the efficiency and the ripple of the DCDC converter outputs. A shielded inductor with R_{DC} of maximum 0.1 Ω guarantees a good performance. For the DA1469x DK PRO, a muRata inductor with a saturation current of 3.6 A and DC resistance of 0.032 Ω is used (Table 7). The table shows five suitable inductor examples. The given height is the maximum thickness or height of the inductor according the information of the manufacturers.

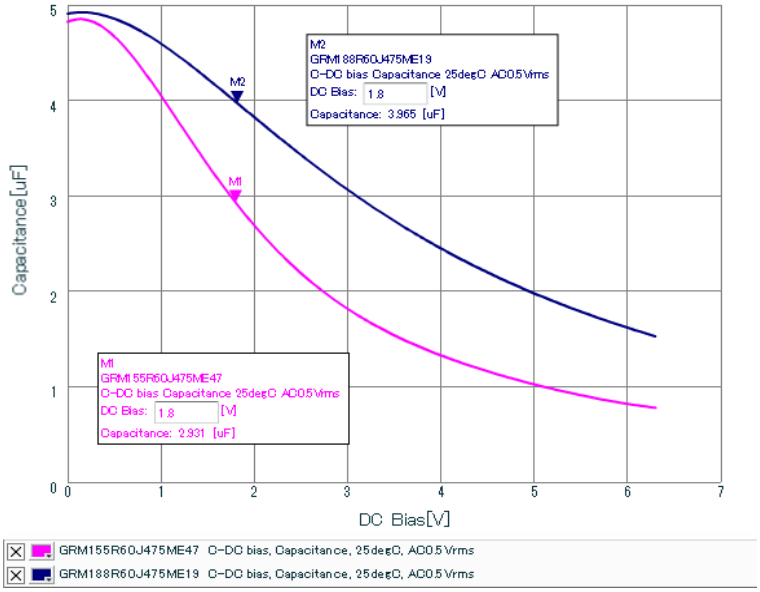


Figure 7: 4.7µF/6.3V: Capacitance Change 0402 Package (Purple) and 0603 Package (Blue)

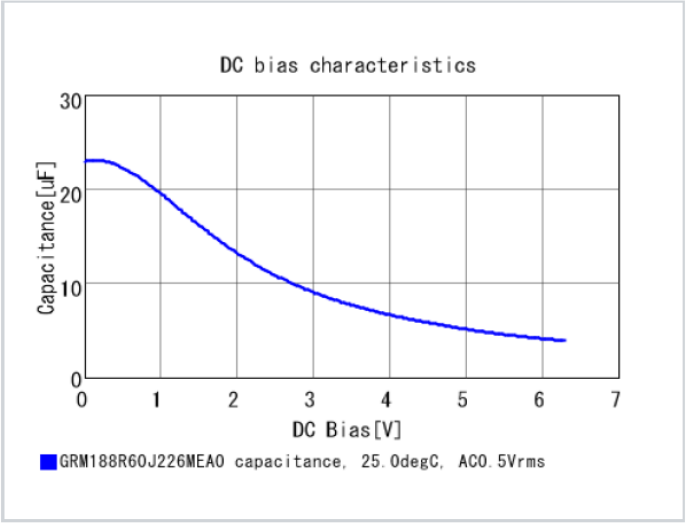


Figure 8: 22µF/6.3V: Effective Capacitance @ 1.8 V ~14 µF (> 10 µF)

Table 7: SIMO DCDC Inductor Examples and Characteristics

Manufacturer	Description, properties	Value	Package	Part Number
muRata	Shielded, 3.6 A, R_{DC} 32 mΩ max.	470 nH	2016M, H 1 mm	DFE201610E-R47M=P2
Inpaq Techn.	Shielded, 3.9 A, R_{DC} 40 mΩ max.	470 nH	2016M, H 1 mm	WIP201610P-R47ML
Samsung EM	4.0 A, R_{DC} 43 mΩ max.	470 nH	2012M, 0.8 mm	CIGT201208EMR47MNE
SunLord	Shielded, 2.0 A, R_{DC} 86 mΩ max.	470 nH	2012M, 0.6 mm	MPM201206SR47
Panasonic	Shielded, 1.2 A, R_{DC} 0.1 Ω max.	470 nH	2012M, H 1mm	ELGTEAR47NA

5.1.1 Supplying External Loads

There are different ways to supply external loads from the DA1469x SoC:

- V30 power rail: the V30 voltage is generated from VBUS or VBAT using the internal 3.0 V LDOs. External loads up to 150 mA can be supplied by the V30 supply. In sleep mode the V30 power capability is 10 mA. During wake-up, initially the V30 rail must charge the other supply rails. This causes a voltage dip on the V30 rail. This is no problem for the DA1469x SoC itself, but when having, for example, sensors on this rail that are sensitive to supply voltage variations, it could be needed to decrease the voltage dip in the V30 rail by applying a decoupling capacitor (C3) that has a rated value and voltage of 10 µF/10 V instead of the default 4.7 µF/10 V. On the DA1469x DK PRO the voltage dip in the V30 rail typically will be approximately 100 mV with a duration of about 50 µs when applying a 10µF/10V capacitor. If needed, larger capacitance values may be applied
  - A severe instability issue may occur when large current transients are drawn from the V30 rail. Peak currents higher than 150 mA for longer than 200 µs, or 300 mA for 50 µs or longer, may cause the system to crash when the V30 rail voltage becomes lower than 1.5 V
  - As a solution, a P-Ch MOSFET (Q4) having a gate-source threshold voltage of about -2 V to -1.5 V may be added in series with the V30 rail to power the external loads. This prevents the V30 rail voltage will drop below 1.5 V. See Figure 6
- V18 and V18P power rail: the V18P rail is used for supplying the QSPI memories (via V18F). The V18 rail is used to supply peripherals like sensors. The current capability of these rails is 50 mA in active mode and 10 mA in sleep mode (Table 8)
- The GPIO's supply-rail can be individually configured to 1.8 V or 3.0 V. When the supply rail is set to 1.8 V, the corresponding GPIO is supplied from the V18P rail. When the supply rail is set to 3.0 V, the corresponding GPIO is supplied from the V30 rail
- The GPIO's output current capability is 5 mA. The power delivered to the load needs to be taken into consideration when determining the power budget of the total system. GPIOs can be used to supply light loads, like a LED, NTC resistor network, or a low-power sensor. The maximum current they can sink, or source is 5 mA. System designers must also consider the current capability of the voltage rails that supplies the GPIOs when the system is in sleep mode

Table 8: DA1469x Voltage Rails

Voltage Rail	Voltage (V)	Current Active/Sleep (mA)	Notes
V30	3.0 or 3.3	150/10	Hibernation: 2.4 V/1 mA (clamp)
V18	1.8 or 1.2	50/10	Supply for external devices
V18P/V18F	1.8	50/10	Supply for GPIOs and FLASH
V14	1.4	20/0	Internal use only
V12	0.9 and 1.2	50/1	Internal use only/0.75 V in sleep

5.1.2 Supplying the DA1469x with VBAT Voltages Lower than 3.3 V

When supplying the DA1469x SoC with fixed VBAT supply voltages of 3.3 V or lower, it is advised to connect the VBAT1, VBAT2 and the V30 rails together to avoid a possible small LDO_VBAT (Figure 5) drop-out voltage from the VBAT1 supply to the V30 rail.

Having the V30 rail shorted to the VBAT rails (Figure 9), the LDO_VBAT is by-passed and the voltage on the V30 rail is the same as the VBAT supply voltage.

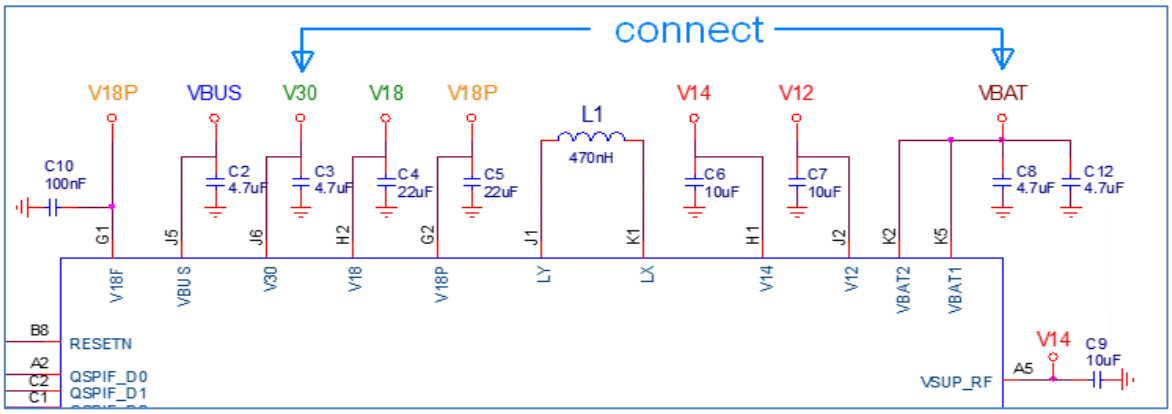


Figure 9: Low VBAT Voltage Power Connection

With the LDO_VBAT being bypassed, this V30 LDO is not loaded anymore. As such the external P-Ch MOSFET to protect the LDO_VBAT against large overload currents is not required anymore. Q4 shown in Figure 6 can be omitted. This V30 to VBAT connection method is strongly advised for VBAT supply voltages lower than 2.4 V, down to 1.9 V which is the minimum allowed supply voltage for the V30 rail. For VBAT voltages higher than 3.3 V, this connection method does not have an advantage anymore, and it is advised to connect the DA1469x SoC in the standard way as shown in Figure 6. The VBAT BOD (BOD_VBAT_EN) may be disabled, since the system still is protected by the BOD on the V30 rail which has the same voltage as the VBAT supply. The VBAT BOD must be disabled when the VBAT supply voltage is equal to or lower than 2.4 V, or when it can be expected that the VBAT voltage could drop below 2.4 V. If the V30 rail voltage can become lower than 2.0 V, the level value of the V30 BOD (BOD_LVL_V30) must be adapted to comply with the lower V30 rail voltage.

5.2 Reset Pin (RSTn)

The DA1469x family of chips, unlike other Dialog Bluetooth® Low Energy chip families (DA1458x and DA1468x), have an active-low reset pin (RSTn pad). It contains an RC filter for spike suppression with a resistor of 400 kΩ and a capacitor of 2.8 pF. It also contains a 25 kΩ pull-up resistor. If the RSTn pad needs to be driven externally, it can be done with the use of a single N-Ch MOSFET or a simple button-switch connected to ground. The typical latency of the RSTn pad is around 2 µs.

5.3 Brown-Out Detector (BOD)

5.3.1 BOD Operation

The brown-out detector (BOD) is a voltage monitoring circuit that triggers an HW reset if LDOs or supply voltages go below a certain threshold.

The BOD is periodically active in either Active or Sleep mode with a programmable interval (PMU_SLEEP_REG [BOD_SLEEP_INTERVAL]) [1].

The BOD can help to prevent malfunction in case of dips in the supply voltage. This could be useful in applications using replaceable batteries with weak spring contacts.
An HW reset might be more acceptable than for instance Flash memory corruption.

The rails that can be monitored are: VBAT, V30, V18, V18P, V18F, V14, and V12 (VDD). Seven in total with a fixed sequence.

Because the V18P and V18F rails are shorted externally, one may be skipped by disabling the BOD for that rail. For example, V18F.

The default BOD clock frequency is 1 MHz, and each rail voltage is checked during one BOD clock cycle that lasts 1 µsec.

The BOD circuit uses a reference voltage 1.2 V. A scaled down voltage of the monitored rail is compared to this BOD reference voltage using a multiplexor and a comparator.

The voltages of the monitored rails are scaled down by a programmable gain amplifier to be compared to the 1.2 V reference voltage. The scale down factor is synchronously adapted for each monitored rail.

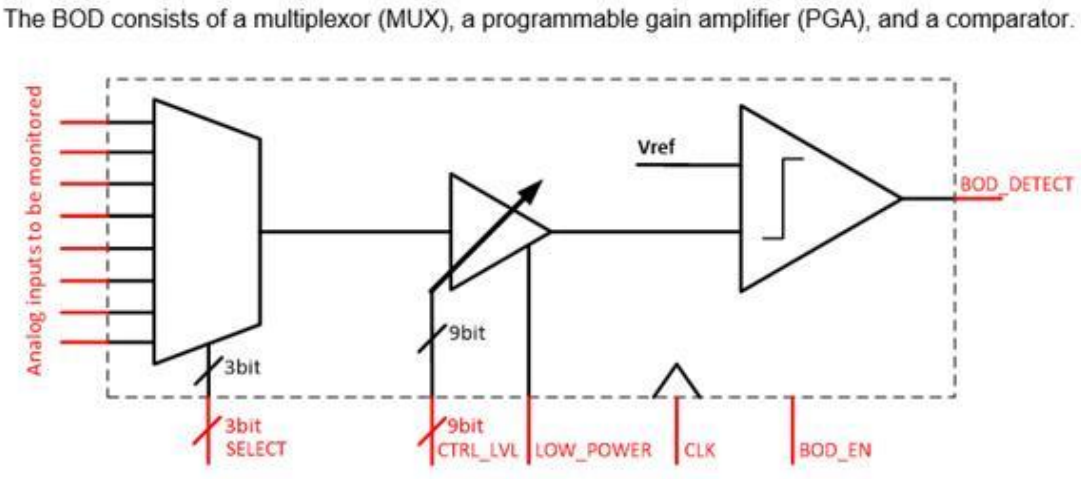


Figure 10: BOD Circuit Operation

Example: the V18P default BOD trigger level is 1.65 V. If the V18P voltage drops below 1.65 V, the BOD must trigger an HW reset.

The scaled down voltage of the V18P rail is compared to the 1.2 V BOD reference voltage and if the scaled down voltage of the V18P rail is above 1.2 V, the BOD should not be triggered. But when dropping below 1.2 V, the BOD must trigger. Thus, the V18P rail voltage must be scaled down by a factor of 1.65 ÷ 1.2 = 1.375 to meet this condition.
For nominal V18P = 1.8 V, the scaled-down voltage at the comparator input is approximately 1.3 V.

The BOD trigger thresholds are programmable per supply rail.

For the 1.8 V rails, the required value to be programmed into the BOD threshold level (*BOD_LVL*) can be calculated as follows: *VTH_BOD = 1.65 V = 1.2 * (BOD_LVL+1)/192*.

For (*BOD_LVL+1)/192 = 1.375*, the value of *BOD_LVL* must be: 263 (0x107).
The value 0x107 must be programmed to *BOD_LVL_V18P* in the *BOD_LVL_CTRL1_REG*.

The same formula is valid for all the other rails, except for VBAT.

5.3.2 BOD Usage

Sometimes the BOD can cause false triggers which means that the monitored supply rails do not show a reason for a BOD event, but the BOD is triggered and the application resets. Thus, the users should decide if they want to enable this feature (option) in the production version.

There are evidences that the false triggering is caused by noise on the internal supply lines. This depends on the load on the chip's supply rails, grounding strategy of the chip and its decoupling caps. When the ground connections of the chip and its decoupling capacitors are suboptimal, the chances of false BOD triggers are higher.
A solid grounding of the chip and its decoupling capacitors will result in a stable DCDC operation, stable supply voltages and a reliable chip operation.
For information on PCB layout design, see Section 5.16.

During the development phase it is suggested to enable the full BOD functionality. At this stage, the BOD might help to find design weaknesses such as a bad grounding of the chip, bad grounding or big distance of the decoupling capacitors, soldering quality and so on. If one of these is affecting the

stability of the chip's supply voltages, the BOD circuit will detect it. Actions should be taken to improve the hardware application.

During the production phase of the product, assuming all design weaknesses identified have been corrected, it is advised to only partially enable the BOD functionality to avoid false triggers. However, it is strongly advised to keep the BOD enabled on the V14 rail.
This rail is important in that it supplies the 32 MHz crystal oscillator (XTAL32M system clock), and it should be detected when the V14 rail-voltage is dropping to prevent un-expected system behavior.

Additionally, the application should have the watchdog enabled that will make sure the product recovers from other system interruptions.

The BOD can be enabled by the following macro in the configuration file:
#define dg_configUSE_BOD (1).

When during debugging BOD, resets are not wanted but still it's important to know whether the BOD detects low rail-voltage situations, the BOD resets may be masked.
For example, the V18P rail: *BOD_V18P_EN* in *BOD_CTRL_REG* must be enabled (0x1), but the *BOD_V18P_RST_EN* bit in the same register must be disabled by setting it to 0x0.
This can be done per rail in the */* Generate Reset on a BOD event */* section in the *hw_bod_da1469x.c* file.
The presence of possibly occurred BOD events can be checked in the *BOD_STATUS_REG*.

5.3.3 POR Circuits

Besides the BOD circuit for monitoring the supply rails, there are two POR circuits implemented in the SoC that will result in a Power-On Reset as well when the supply voltage and the core voltage drop down to critical levels. These POR circuits are fast and are triggered on very short voltage interrupts and voltage drops:

- POR circuit on the core supply VDD (V12) triggered at 0.6 V
  This POR circuit cannot be disabled, it is always on
- POR circuit in VBAT1: POR_VBAT triggered at 1.6 V
  The POR_VAT can be masked or disabled, but It's strongly advised to keep it enabled
  POR_VBAT_CTRL_REG [POR_VBAT_ENABLE]

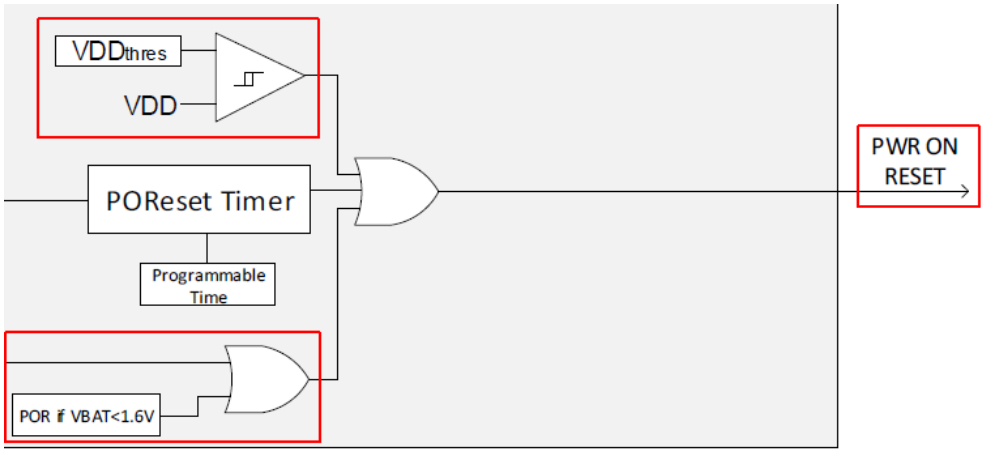


Figure 11: POR Circuits in the DA1469x SoC

5.4 Digital I/O Pins

The DA1469x has a software configurable I/O pin assignment organized into ports Port-0 and Port-1. All pins are available in the VFBGA100 package; the VFBGA86 package lacks some Port-1 GPIOs. The following information about the I/O pins characteristics is very useful for system designers:

- Port 0: 32 pins and Port 1: 23 pins (including M33_SWCLK, M33_SWDIO, CMAC_SWCLK, and CMAC_SWDIO)

- Fully programmable pin assignment (PPA)
- Selectable 25 kΩ pull-up or pull-down resistors per pin. Exceptions: P0_00 ~ P0_05
- Programmable open-drain functionality
  Note that, the input voltage should not exceed the voltage of the V18P or the V30 rail, depending on the used rail for that GPIO. When applying external pull-up resistors, only connect these to the V18P or the V30 rail. Do not connect them to the supply voltage or other rails
- Output voltage and pull-up voltage is configurable per pin: V30 or V18P
  Exceptions: P0_00 ~ P0_05, P0_14 and P0_15
- P0_00 to P0_05 GPIOs (QSPI RAM pins): these pins can be used at 1.8 V (V18F) only, cannot be used at 3 V. These six GPIOs have pull-up and pull-down resistors with a value of 40 KΩ
- P0_14 and P0_15 (USB pins): when these are to be used in GPIO mode, USBPAD_REG[USBPAD_EN] must be set. These GPIOs can be supplied solely by the V30 rail Allowed output levels are the V30 voltage and 0 V, 1.8 V output is not possible. If the 1.8 V rail would be selected as the supply for P0_14 and P0_15, a current of 150 µA is to be expected Moreover, these two GPIOs should not be used in sleep mode because the USBPAD_REG belongs to the system power domain and is powered off in all sleep modes. It means that these pins do not support state retention during power down
- Fixed assignment for analog pins, motor controller and LCD controller pins
- Pins can retain their last state by using always-on latches when system enters the extended, deep sleep, or hibernation mode (except P0_14 and P0_15)
- There is the reduced driving strength (RDS) functionality on 13 pins (Table 9). The GPIOs and strength can be accessed/modified from register PAD_WEAK_CTRL_REG (0x50020B00). These pins are available for both packages. This mode should be coupled with the selection of the V18P supply rail for these pins. When selecting the V30 rail as supply, the RDS functionality is not supported.

Table 9: DA1469x GPIOs with RDS Functionality

Port	Pins
0	P0_06, P0_07, P0_16, P0_17, P0_18, P0_25, P0_26, P0_27
1	P1_00, P1_01, P1_02, P1_06, P1_09

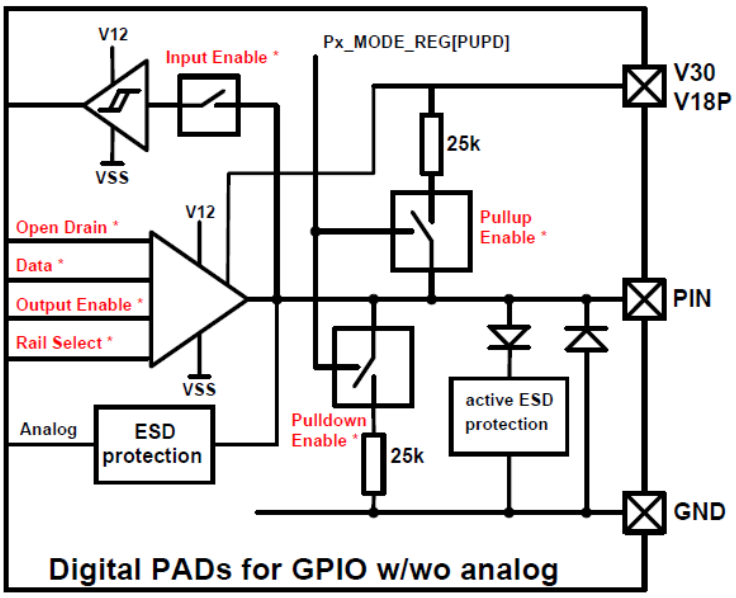


Figure 12: PAD I/O Configuration and Signals Latching (in Red)

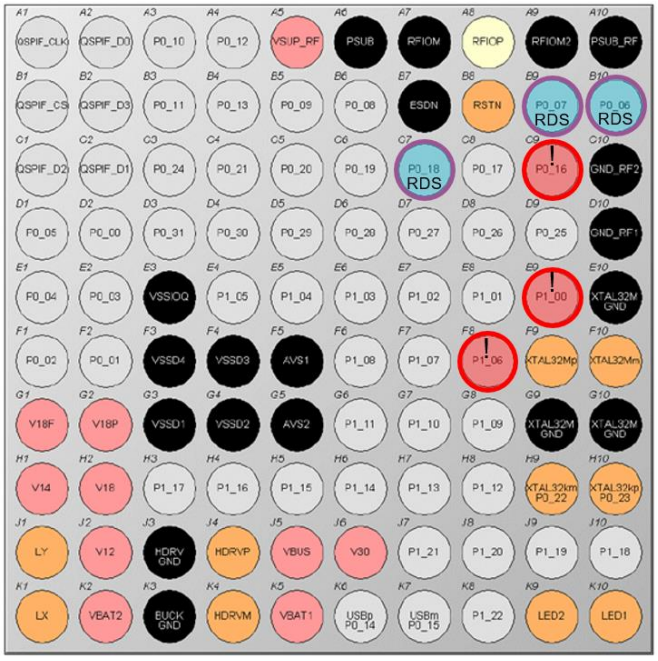
5.4.1 Interference to XTAL32MHz from GPIOs

The fast toggling of some GPIOs causes an increased packet error rate (PER [%]) during Bluetooth LE reception. It is suggested to use them for low speed or static signals (for example, buttons).

Please follow the guidelines below when using the GPIOs:

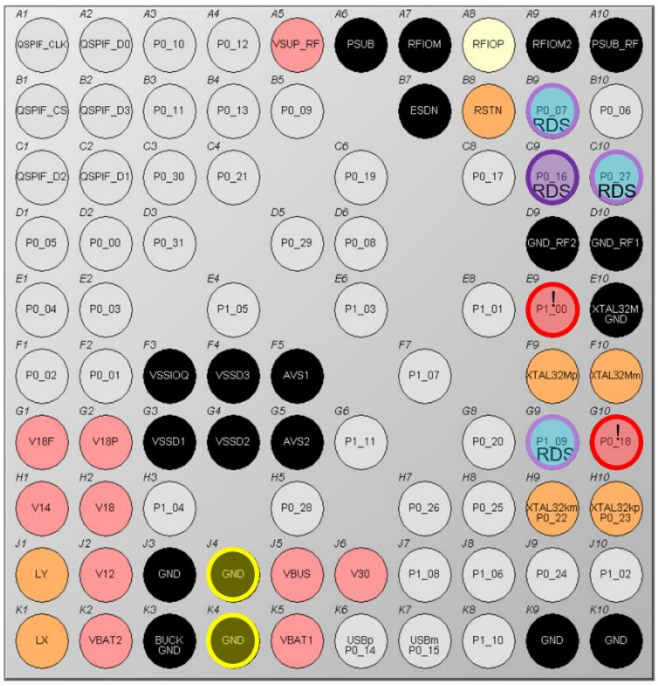
- P0_18, P0_16, P1_00, P0_07, P1_09, P0_27 (VFBGA86) and P0_16, P1_00, P1_06, P0_18, P0_06, P0_07 (VFBGA100) might affect radio and XTAL32MHz crystal oscillator performance when being toggled while a RF activity occurs or XTAL32MHz oscillates. It is recommended to use them at low speed and not to use them while radio is active. If these pins are used as outputs, users should select the weak-drive capability. Note that, not all GPIOs have the capability of reducing the driving strength
- P1_12, P1_18, and P1_19 might affect XTAL32k performance when being toggled at high frequencies while XTAL32k is used. It is recommended to use them at low speed when these pins are set as outputs

Table 10: Interfering GPIOs on DA14697 and DA14699 (VFBGA100)

GPIO	Notes	VFBGA100 Pins Location
P1_06 P0_16	Do not toggle them fast for both input or output state when the radio is active.	
P1_00	Bad performance as input. When it operates as an output, its performance is improved by enabling RDS (Note 1).	
P0_06 P0_07 P0_18	These can be used as an input without problem. They have a minor impact on packet error rate when operating as an output. Performance is much improved by enabling RDS (Note 1)	

Note 1 Reduced driving strength (RDS) functionality is applied on 13 pins by setting the register PAD_WEAK_CTRL_REG (0x50020B00). Such pins are presented in Table 9.

Table 11: Interfering GPIOs on DA14691 and DA14695 (VFBGA86)

GPIO	Notes	VFBGA87 Pins Location	
P0_18 P1_00	Fast toggling of these pins in either input or output state results in interference on XTAL32M and/or RF. Do not toggle when the radio is active.		
P1_09 P0_27 P0_07	They can be used as input without problems. As output, performance is improved much by enabling RDS (Note 1).		
P0_16	P0_16 can NOT be used as input. It can only be used as output when RDS is enabled (Note 1).		

Note 1 Reduced driving strength (RDS) functionality is applied on 13 pins by setting the register PAD_WEAK_CTRL_REG (0x50020B00). Pins are presented in Table 9.

5.5 Crystals and Clocks

The DA1469x SoC is equipped with two Digitally Controlled Crystal Oscillators (DCXO), one at 32 MHz (XTAL32M) and the other at 32.768 kHz (XTAL32K). XTAL32K has no trimming capabilities and is used as the low power clock for the extended/deep sleep modes. XTAL32M can be trimmed by using the internal capacitor bank.

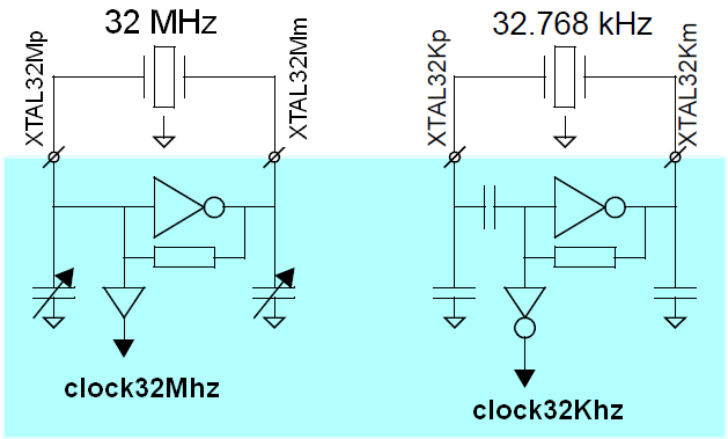


Figure 13: XTAL32M and XTAL32K Oscillator Circuits

5.5.1 32 MHz Clock

The DA1469x needs an accurate 32 MHz clock for proper operation. The clock can be generated either by an external 32 MHz crystal or by applying an external 32 MHz clock signal.

The XTAL32M crystal oscillator can be trimmed. No external components are required other than the crystal itself. If the crystal has a case connection, it is advised to connect the case to ground (Figure 15). Register CLK_FREQ_TRIM_REG controls the trimming of XTAL32M. The trimming range of the internal capacitor bank is from the lowest capacitance – being roughly 4 pF – to the highest capacitance which approximately is 10.5 pF. The lowest available capacitance offered to the 32 MHz crystal is affected by the board stray capacitance. The value of 4 pF is measured in the DA1469x Pro-DK board. Other designs may show larger stray capacitance to the XTAL32M pins, which in turn might increase the lowest available trim capacitance a bit.

The CLOAD value (C_L) of the used 32 MHz crystal preferably would be 6 pF typical. Check out the notes on C_L below. The crystal's ESR must not exceed 100 Ω. See Table 12.

Table 12: XTAL32M Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
F_{XTAL}(32M)	Crystal oscillator frequency			32		MHz
ESR(32M)	Equivalent series resistance				100	Ω
C_L(32M)	Load capacitance	No external capacitors are required	4	6	8	pF
C_0(32M)	Shunt capacitance				3	pF
Δf_{XTAL}(32M)	Crystal frequency tolerance	After optional trimming; including aging and temperature drift (Note 1)	-20		+20	ppm
Δf_{XTAL}(32M) UNT (Note 2)	Crystal frequency tolerance	Untrimmed; including aging and temperature drift	-40		+40	ppm
Drive Level	Maximum Allowable Power		100			µW

Note 1 Using the internal capacitor bank, a wide range of crystals can be trimmed to the required tolerance.

Note 2 This is the maximum allowed frequency tolerance for compensation by the internal capacitor bank trimming mechanism and using a typical 32 MHz crystal having a C_L value of 6 pF.

Some notes on the crystal trimming range when applying 32 MHz crystal with various C_L values:

- A 32 MHz crystal having C_L = 6 pF can be fully trimmed over the specified ±40 ppm, typically 100 ppm in total over the complete capacitor bank range. This is the advised crystal to be applied
- A 32 MHz crystal having C_L = 8 pF faces a limited trim range towards larger trim capacitances. The typical overall frequency trim range for a crystal having a C_L = 8 pF is -30 ppm to +70 ppm. It is advised to apply a frequency tolerance of maximum ±20 ppm for crystals having C_L = 8 pF
- 32 MHz crystals having C_L = 4 pF (these are rare) is far from optimal: such a crystal cannot be trimmed towards smaller load capacitances, because the lowest value of the capacitor bank is about 4 pF. It is advised to not use crystals having C_L = 4 pF, unless their frequency tolerance is equal to or better than ±10 ppm. As such, the cap-bank trim value should be set to 0, which results in applying the minimum trim capacitance - being about 4 pF - to that crystal. Bottom line: it is not advised to use this type of 32 MHz crystal with the DA1469x.

The CLK_FREQ_TRIM_REG register controls the trimming of the XTAL32M oscillator. The frequency is trimmed by two on-chip variable capacitor banks. Both capacitor banks are controlled by the same register, CLK_FREQ_TRIM_REG[XTAL32M_TRIM]:

- CLK_FREQ_TRIM_REG[XTAL32M_TRIM] = 0x2BF: the maximum capacitance and thus the minimum oscillation frequency is selected
- CLK_FREQ_TRIM_REG[XTAL32M_TRIM] = 0x000: the minimum capacitance and thus the maximum oscillation frequency is selected

The ten least significant bits of CLK_FREQ_TRIM_REG register (XTAL32M_TRIM bit field) directly control the ten binary weighted capacitors (Figure 14).

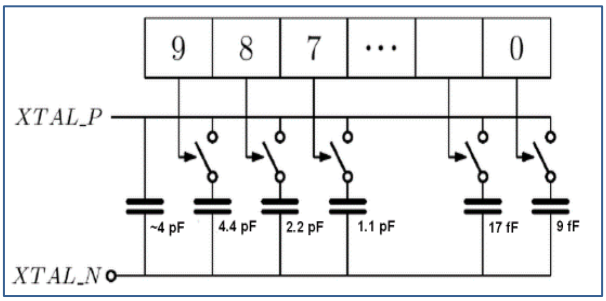


Figure 14: XTAL32M Frequency Trimming

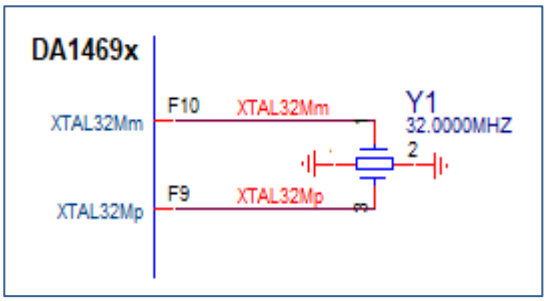


Figure 15: Physical Connection of XTAL32M

Table 13 presents some examples of 32 MHz crystals which can be used for the DA1469x and meet the specification described above. The listed muRata XRCGB32M type is used in DK PRO.

Table 13: 32 MHz Crystal Examples and Characteristics

	muRata	TXC	KDS	Seiko Epson
Part Number	XRCGB32M000F1H00R0	8Q32070005	DSX1210A	FA-1280004300
Frequency	32 MHz	32 MHz	32 MHz	32 MHz
Freq. Tolerance	±10 ppm	±10 ppm	±15 ppm	±10 ppm
Load Cap. (C_L)	6 pF	6 pF	6 pF	6 pF
Shunt Cap (C_0)	-	2.0 pF max.	1.0 pF max.	3.0 pF max.
Equiv. Series Res. (ESR)	60 Ω max.	60 Ω max.	60 Ω max.	60 Ω max.
Drive Level (PD)	300 µW max.	100 µW	100 µW	100 µW
Temperature Range	-30 °C ~ +85 °C	-30 °C ~ +85 °C	-30 °C ~ +85 °C	-40 °C ~ +85 °C
Temp. Freq. Drift	±10 ppm	±10 ppm	±20 ppm	±20 ppm
Size L × W × H (mm)	2.0 × 1.6 × 0.65	1.6 x 1.2 x 0.35	1.2 x 1.0 x 0.30	2.0 x 1.6 x 0.50

5.5.2 32.768 kHz Clock

The DA1469x utilizes a low power, low frequency clock for extended and deep sleep modes. This can be achieved with either the XTAL32K oscillator (using an external 32.768 kHz crystal) or the internal RCX oscillator, which has a frequency accuracy of ±500 ppm maximum.

When the RCX oscillator is used, no external crystal is needed. Using an external 32.768 kHz crystal provides tighter timing due to a higher accuracy (±50 ppm) but requires additional board space and adds the cost of the crystal.

The XTAL32K cannot be trimmed. The crystal is connected to the pins XTAL32Kp and XTAL32Km. External load capacitors are not required for a crystal with a load capacitor of 6 pF or 7 pF. When applying a crystal which requires, for instance, 9 pF load capacitance, additional capacitors must be added, one at each XTAL32K pin to ground.

The external 32.768 kHz crystal must meet the recommended operating conditions of a 32.768 kHz crystal oscillator (Table 14).

Table 14: XTAL32K Recommended Operating Conditions

Parameter	Description	Conditions	Min	Typ	Max	Unit
$f_{CLK\_EXT\_32K}$	External clock frequency	At pin XTAL32KP/P0_23 in GPIO mode	31		33	kHz
f_{XTAL_32K}	Crystal oscillator frequency			32.768		kHz
ESR32K	Equivalent series resistance				100	kΩ
C_{L_32K}	Load capacitance	No external capacitors are required for a 6 pF or 7 pF crystal	6	7	9	pF
C_{0_32K}	Shunt capacitance			1	2	pF
Δf_{XTAL_32K}	Crystal frequency tolerance (including aging)	Timing accuracy is dominated by crystal accuracy. A much smaller value is preferred.	-250		+250	ppm
$P_{DRV\_MAX\_32\ K}$	Maximum driver power	Note 1	0.1			µW

Note 1 Select a crystal that can handle a drive level of at least this specification.

Table 15 presents two examples for a 32.768 kHz crystal. Both meet specification described above. The ABS07 type is used in DA1469x DK PRO.

Table 15: 32.768 kHz Crystal Examples and Characteristics

Reference Designator	Abracon Corp.	Seiko Epson Corp.
Part Number	ABS07-32.768KHZ-7-T	FC1610AN
Frequency	32.768 kHz	32.768 kHz
Accuracy @ +25 °C	±20 ppm	±20 ppm
Load Capacitance (CL)	7 pF typ.	7 pF typ.
Shunt Capacitance (C0)	0.9 to 1.2 pF	1.2 pF typ.
Equiv. Series Resist. (ESR)	70 KΩ max	90 KΩ max
Drive Level (PD)	0.5 µW max.	0.5 µW max.
Temperature range:	-40 °C ~ +85 °C	-40 °C ~ +85 °C
Temperature Coefficient:	-0.036 ppm/°C^2 typ. (+25 °C)	-0.04 ppm/°C^2 max. (+25 °C)
Size L × W × H (mm)	3.2 × 1.5 × 0.9	1.65 x 1.05 x 0.50

5.5.2.1 Providing DA1469x with a 32.768 kHz Square Wave Clock

Follow the procedure below to apply a 32.768 kHz square wave clock signal from an external source (for example, microprocessor control unit) to the P0_23 pin of the DA1469x.

1. Set P0_23 into GPIO function by setting P0_23_MODE_REG [PID] = 0x0.
2. Set the direction of the pin to input by setting P0_23_MODE_REG [PUPD] = 0x0.
3. Set the low power clock to select the external clock signal by setting CLK_CTRL_REG [LP_CLK_SEL] = 0x3.

   Note that, XTAL32K oscillator must be disabled: CLK_32K_REG [XTAL32K_ENABLE] = 0x0.

5.5.3 Generating a Clock Output from DA1469x

The DA1469x SoC can output clock signals at a time, the output port selection is flexible. There are two methods.

Method 1:

- Select a free GPIO, set it as output (PUPD = 0x3), and set its PID to 0x2A (42): Clock

Table 16: Clock Output, Pxy_MODE_REG – PUPD and PID Selection

Bit	Mode	Symbol	Description	Reset
10	R/W	PPOD	0: Push pull 1: Open drain	0x0
9:8	R/W	PUPD	00 = Input, no resistors selected 01 = Input, pull-up selected 10 = Input, pull-down selected 11 = Output, no resistors selected In ADC mode, these bits are don't care	0x2
			27: USB (dedicated pins P0_14 and P0_15) 28: PCM_DI 29: PCM_DO 30: PCM_FSC 31: PCM_CLK 32: PDM_DATA 33: PDM_CLK 34: COEX_EXT_ACT0 35: COEX_SMART_ACT 36: COEX_SMART_PRI 37: PORT0_DCF 38: PORT1_DCF 39: PORT2_DCF 40: PORT3_DCF 41: PORT4_DCF 42: CLOCK (see also GPIO_CLK_SEL_REG for the dedicate pins mapping of the supported clocks) 43: PG (dedicated pins, see also the "Input/Output Ports" section of the Datasheet) 44: LCD (dedicated pins)	

- Select which clock to output. Only one clock signal can be output:
  - GPIO_CLK_SEL_REG:
    - Bit 3, FUNC_CLK_EN: 0x1
    - Bit 2:0, FUNC_CLK_ SEL: for example, 0x0: XTAL32K; 0x2: RCX; 0x3: XTAL32M

Table 17: GPIO_CLK_SEL_REG (0x50020AFC)

Bit	Mode	Symbol	Description	Reset
3	R/W	FUNC_CLOCL_EN	If set, it enables the mapping of the selected clock signal, according to FUNC_CLOCL_SEL bit-field.	0x0
2:0	R/W	FUNC_CLOCL_SEL	Select which clock to map when PID = FUNC_CLOCK. 0x0: XTAL32K 0x1: RC32K 0x2: RCX 0x3: XTAL32M 0x4: RC32M 0x5: DIVN 0x6: Reserved 0x7: Reserved	0x0

Method 2:

By setting GPIO_CLK_SEL_REG bits 4 to 9, system clocks are mapped to specific GPIOs (Table 17). Note that, this does not work directly for all outputs, since some pins are reserved for other functions, such as USB, SD-ADC, or SWD M0 (Table 18). The advantage of this method is that multiple clocks can be output at the same time. However, the GPIO assignment is fixed.

Table 18: System Clocks Mapping to Fixed GPIOs

GPIOs	Clock Signal	Other Function	Comments
P0_12	XTAL32M	CMAC_SWDIO	Cannot be used if the Arm Cortex-M0+ JTAG is used
P0_13	RC32M	CMAC_SWCLK	
P0_14	XTAL32K	USBp	Cannot be used if USB interface is used
P0_15	DIVN	USBm	
P0_16	RCX	SDADC_REF	Cannot be used if ΣΔ ADC is used
P0_17	RC32K	-	

Table 19: GPIO_CLK_SEL_REG (0x50020AFC)

Bit	Mode	Symbol	Description	Reset
9	R/W	DIVN_OUTPUT_EN	DIVN output enables bit-field. When set, it enables the mapping of DIVN clock on dedicated GPIO (P0_15). The specific GPIO must be configured as GPIO output.	0X0
8	R/W	RC32M_OUTPUT_EN	RC32M output enables bit-field. When set, it enables the mapping of RC32M clock on dedicated GPIO (P0_13). The specific GPIO must be configured as GPIO output.	0X0
7	R/W	XTAL32M_OUTPUT_EN	XTAL32M output enables bit-field. When set, it enables the mapping of XTAL32M clock on dedicated GPIO (P0_12). The specific GPIO must be configured as GPIO output.	0X0

Bit	Mode	Symbol	Description	Reset
6	R/W	RCX_OUTPUT_EN	RCX output enables bit-field. When set, it enables the mapping of RCX clock on dedicated GPIO (P0_16). The specific GPIO must be configured as GPIO output.	0X0
5	R/W	RC32K_OUTPUT_EN	RC32K output enables bit-field. When set, it enables the mapping of D RC32K clock on dedicated GPIO (P0_17). The specific GPIO must be configured as GPIO output.	0X0
4	R/W	EXTAL32K_OUTPUT_EN	EXTAL32K output enables bit-field. When set, it enables the mapping of EXTAL32K clock on dedicated GPIO (P0_14). The specific GPIO must be configured as GPIO output.	0X0

NOTE

The DA1469x SoC can only output clock signals in active mode using the two methods discussed above. To output a clock while the system is in sleep, use a timer with a PWM output.

Timers suitable for this task are Timer1 (if not used by the operating system) and Timer2, which can output a PWM signal to pins P1_01 and P1_06, respectively. These pads remain active while the system is in extended sleep mode. Since the PWM counter needs a minimum count of 1, the maximum frequency that can be output during sleep is LP_CLOCK/2.

In deep Sleep and Hibernation mode, there are no clock outputs (no RAM retained, no clocks in hibernation).

5.6 UART

The UART section consists of the UTX and URX signals, which are assigned to P0_09 and P0_08 GPIOs pins, respectively. Note that, although UART signals can be assigned to any pins, for the DA1469x SoC this pin pair assignment is the ONLY one supported for booting from UART. The baud rate during boot is set to 115.2Kbd. UART hardware flow control (UCTS, URTS) is available as well. By default, these are assigned to P0_07 and P1_00 respectively.

NOTE

The NTC circuit also uses P0_07 and P1_00 (Figure 29). Assign UCTS and URTS to other unused GPIOs.

Table 20: UART Pins

	Function	Pin name	VFBGA86	VFBGA100
UART	UART transmit (UTX)	P0_09	B5	B5
	UART receive (URX)	P0_08	D6	B6
	UART cts (UCTS)	P0_07	B9	B9
	UART rts (URTS)	P1_00	E9	E9

5.7 SWD (JTAG)

There are two debug interfaces available on DA1469x SoC, one for every core.

Pins P0_10 and P0_11 are assigned to SWDIO and SWCLK signals, respectively, for the M33 core. The SWD signals mapping is defined by SYS_CTRL_REG[DEBUGGER_ENABLE]. To use these pins as GPIOs, disable the debugger.

Table 21: JTAG Pins for M33 Core

	Function	Pin name	VFBGA86	VFBGA100
JTAG M33	JTAG data (M33_SWDIO)	P0_10	A3	A3
	JTAG clock (M33_SWCLK)	P0_11	B3	B3

P0_12 and P0_13 are assigned to SWDIO and SWCLK signals respectively, for the CMAC. The SWD signals mapping is defined by SYS_CTRL_REG[CMAC_DEBUGGER_ENABLE]. By default, the CMAC debugger is disabled and P0_12 and P0_13 are used as GPIOs.

Table 22: JTAG Pins for CMAC

	Function	Pin name	VFBGA86	VFBGA100
JTAG CMAC	JTAG data (CMAC_SWDIO)	P0_12	A4	A4
	JTAG clock (CMAC_SWCLK)	P0_13	B4	B4

5.8 QSPI Flash Memory

The DA1469x family uses an external low power Quad-SPI FLASH which is used to directly execute code (using the CPU cache).

The QSPI FLASH is driven from dedicated pins which are supplied from V18F. The QSPI Flash cannot be supplied from 3.0 V. The QSPI pins of the DA1469x cannot be used as GPIOs. Consequently, DA1469x only supports 1.8 V Flash devices.

The recommended QSPI FLASH, also used on the DA1469x DK Pro, is the MX25U3235F, 32 Mbit, QSPI FLASH memory, in a SOIC208 package. This is a power efficient QSPI FLASH with a supply voltage of 1.8 V.

As the maximum operating frequency of the QSPI interface in the DA1469x SoC is 96 MHz, it is recommended to use a QSPI Flash memory that can operate at this clock frequency for the best performance. The following flashes (Table 23) have been tested successfully and are supported.

Table 23: Supported QSPI Flash

Part Number	Capacity	Provider
MX25U3235F	32 Mbit	Macronix
GD25LE32D	32 Mbit	Giga Device
W25Q32FW	32 Mbit	Winbond

To avoid signal integrity issues, keep the distance between the processor and the QSPI FLASH memory as short as possible, try to have the length of the traces as equal as possible, and route with enough spacing to avoid crosstalk.

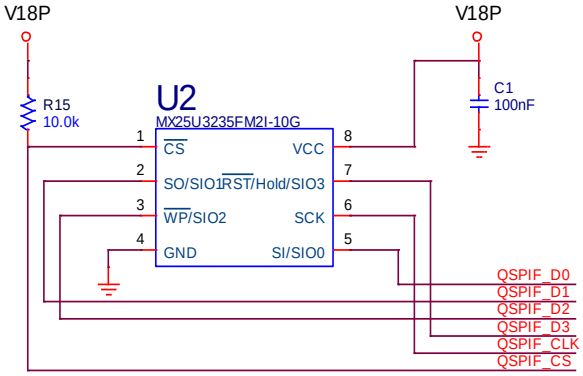


Figure 16: QSPI Flash Memory Used in DA1469x DK PRO

If needed, apply 47 Ω to 56 Ω series resistors in all six QSPI lines. The 10k pull-up resistor (R15) in Figure 16 is not mandatory. The DA1469x QSPI_CS port also pulls up the chip select (/CS) line.

5.9 QSPI RAM Memory

A second Quad SPI controller (QSPIC2), available in all DA1469x except DA14691, provides a low pin count interface to serial QSPI RAM (or FLASH – not bootable) memory devices. The dedicated pins used for connecting the memory are P0_00 to P0_05.

Note that, these pins can be configured as either QSPI RAM signals or GPIOs and can be used at 1.8 V only. These pins cannot be used at 3.0 V.

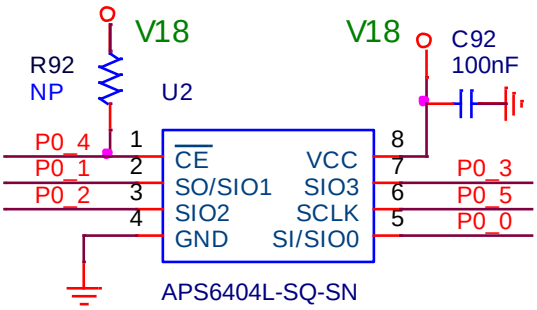


Figure 17: QSPI RAM Used in DA1469x DK PRO

Figure 17 presents the QSPI-RAM component (64 Mbit) and connectivity applied to DA1469x DK PRO. Note that, by default the QSPI RAM is not populated on the DA1469x DK PRO.

5.10 USB and VBUS

The USB interface in DA1469x is an integrated USB controller compatible with the USB 1.1 FS specification. It is advised not to apply series termination resistors in the DA1469x USBP and USBN data lines. Although using such resistors is a common practice, DA1469x does not need these resistors and they affects the USB signal integrity, deteriorating the rise and fall times too much when longer cables are used.

The USB transceiver module is accessed through the USBP (D+) and USBN (D-) signals which are multiplexed with the P0_15 and P0_14 GPIOs, respectively, for both packages.

It is important to configure P0_14 and P0_15 as USB pins before the USB block is enabled. Otherwise the USB block may be damaged if a voltage is applied to the pins which are still configured as GPIOs. To use P0_14 and P0_15 in GPIO mode, set USBPAD_REG [USBPAD_EN]. As already mentioned in the GPIO section, users need to be aware of the following characteristics:

- Only a voltage of 0 V or the V30 rail voltage is allowed on P0_14 and P0_15 in GPIO mode. If 1.8 V is selected as the pin supply, a leakage current of 150 µA is to be expected
- Do not use these pins in any sleep modes, because the USBPAD_REG belongs to the system power domain and is powered off in sleep modes. It means that these pins do not support state retention during power down

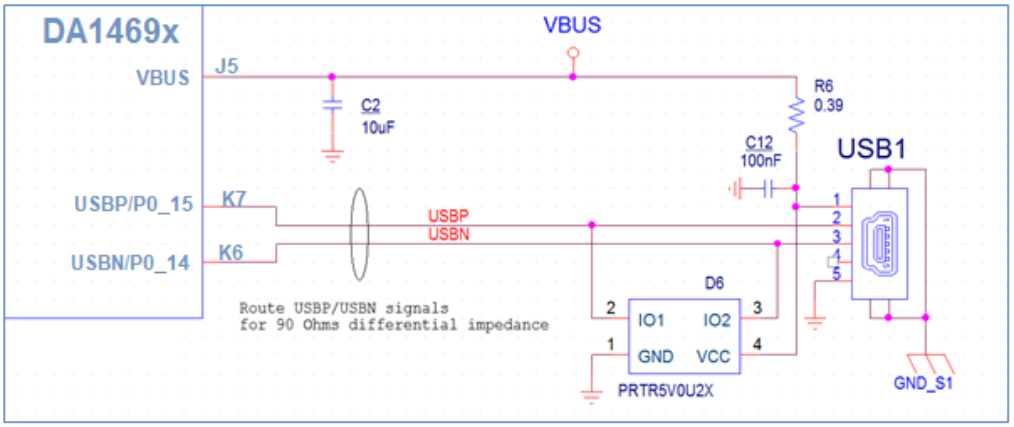


Figure 18: Recommended Topology for USB Functionality

Figure 18 presents a recommended topology for the USB section of the DA1469x SoCs. Note that, on this implementation, VBUS is supplied directly from the USB connector (J1) through resistor R6. On the DA1469x DK PRO, an overvoltage protection (OVP) circuit is used.

5.10.1 USB ESD Measures

For the USB section of DA1469x SoC, an ESD protection circuit like the ESD diode PRTR5V0U2X (Figure 18) must be in place for ESD protection of the USB lines. A discrete component solution, which has been applied to DA1469x DK PRO, can also be used (Figure 19).

If in the USB section the USB functionality is not required but only the charging functionality is used, charger contact pins can be applied in the application to provide +5 V to the VBUS pin of the DA1469x device. For ESD reasons, make sure an ESD protection device is applied directly between the two charger pins. Make sure to have a solid ground connection to the ground terminal of the ESD protection device.

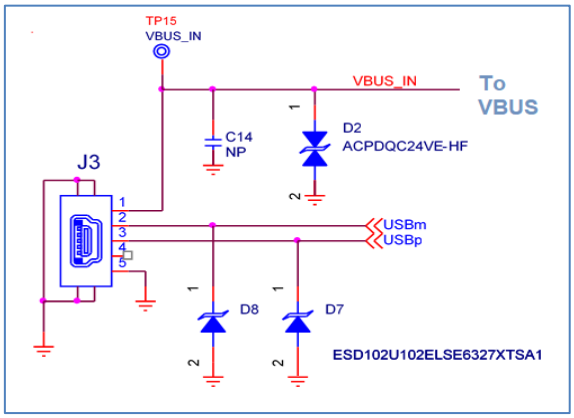


Figure 19: ESD Protection Components on DA1469x DK PRO

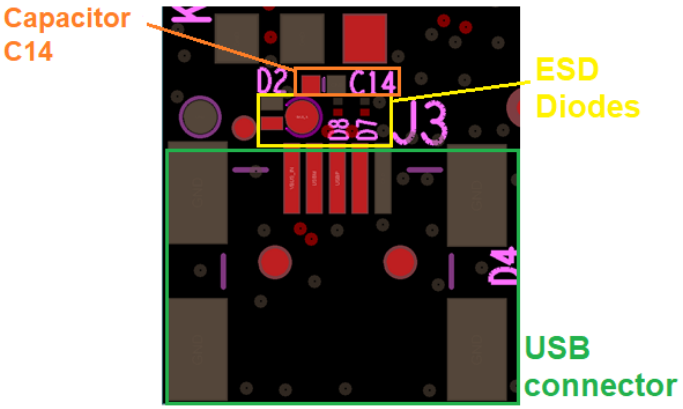


Figure 20: PCB Layout of ESD Protection Components on DA1469x DK PRO

5.10.2 VBUS Circuitry

The USB port is used for the charger supply and the USB cable provides power to VBUS pin of the DA1469x SoC. The USB cable can be approximated by an inductor (L, value is related to the length of the cable). At the VBUS pin of the DA1469xSoC, there is a ceramic supply decoupling capacitor (C2). When the USB cable is plugged in at the connector, a step voltage is applied to the LC series resonator. Depending on the quality of this resonator, a voltage of twice the initial USB voltage can be present on this VBUS pin (2 × 5 V = 10 V). This can result in damaging the components inside the DA1469x and must therefore be avoided.

A way of protecting the DA1469x against high peak voltages during USB cable plug-in is to lower the Q factor of the resonator by adding a series resistor in the line (R2). This series resistor increases the “Damping” of the LC circuit. For an LC series circuit, the damping is defined as:

$$Damping = \frac{R6}{2}\ x\ \sqrt{\frac{C2}{L}} \quad (1)$$

It is beneficial to have a large capacitor on the VBUS pin. A larger capacitor results in a lower value series resistor when a certain amount of damping is required.

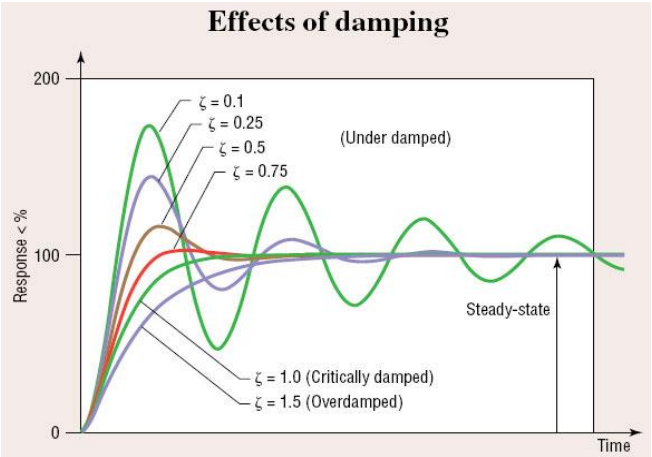


Figure 21: Relation between Damping and the Step Response of a Series LC Resonator

When the inductance increases because of a longer cable and the series resistance is not adapted, the step response will show more ringing (with a higher amplitude). Figure 22, Figure 23, and Figure 24 show that when a damping network of 0.39 Ω and 10 µF is applied to VBUS, with the length of a non-USB cable increasing, the damping effect enough for a 60 cm cable connection is reduced and leads to larger overshoots. Next plots are taken from a system with sufficient damping

for a 60 cm cable connection, whereas, when the length of the cable is increased to 150 cm, the damping reduces leading to larger overshoots. The pink colored traces show the VBUS voltage and the blue traces show the VBUS current. When a non-USB cable of 300 cm is used, the ringing and overshoots get even worse.

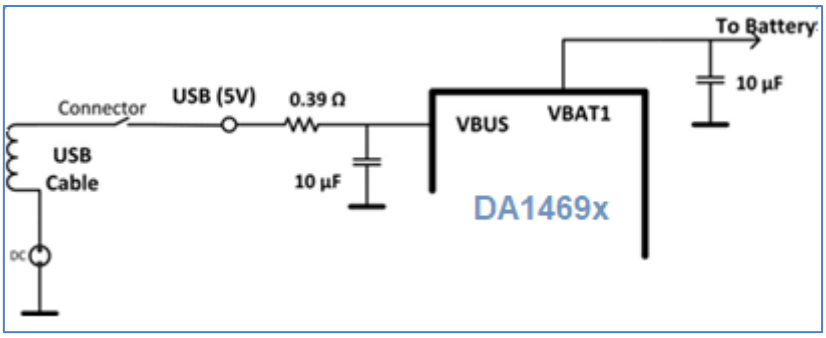


Figure 22: USB Circuit Used for Testing

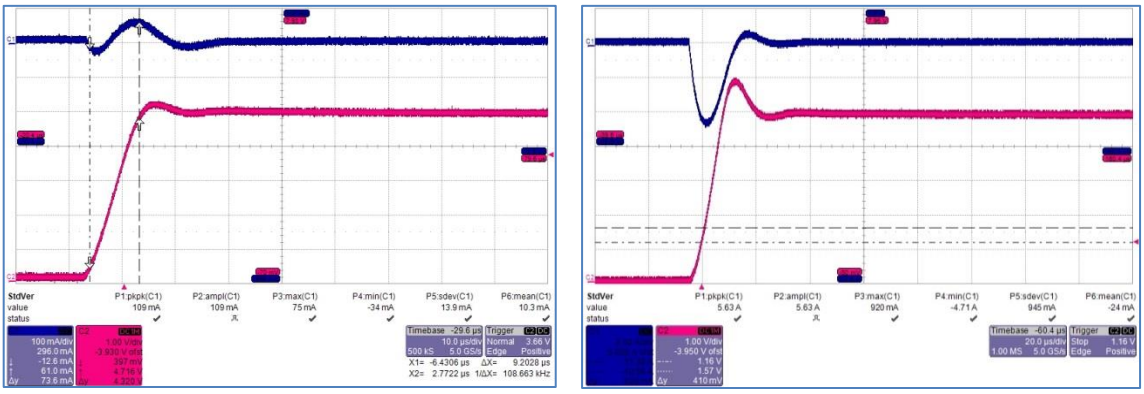


Figure 23: Step Responses for 60 cm Cable (Left) and 150 cm Cable (non USB-Cable, Right). A Damping Network of 0.39 Ω Resistor and 10 µF Capacitor on VBUS is used

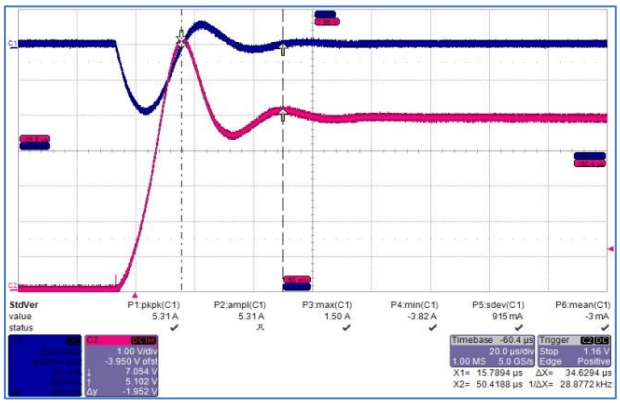


Figure 24: Step Response for 300 cm Cable (non USB-Cable) and Damping Network of 0.39 Ω Resistor and 10 µF Capacitor on VBUS is used

The construction of a USB cable (where the positive and negative wires are close together) is much better regarding the inductance. When a 150 cm USB cable is used in the same situation as above, it gives the step response shown in Figure 25.

In summary, a 0.39 Ω series resistor and a 10 µF capacitor on the VBUS line gives enough damping for short to medium length USB-cables. This configuration is recommended for typical cases.

When longer cables are used, higher resistor values might be needed to achieve enough damping. Maximum charge current and the allowed voltage drop over the series resistor can limit the amount of damping in that case.

Users need to select the resistor values carefully. With a high value resistor, the input VBUS voltage could be decreased to such a level that it cannot reach the specified charging target. Also, in high current peak (for example, due to motor vibration) it may cause a sudden drop on the VBUS input and trigger an unexpected USB detach interrupt.

Alternatively, besides a 0.39 Ω resistor and a 10 µF capacitor, a 0.56 Ω resistor and a 4.7 µF capacitor, or a 0.47 Ω resistor and a 6.8 µF capacitor can also be used. These R-C combinations results in the same damping value. The capacitors should preferably have a working voltage of 10 V.

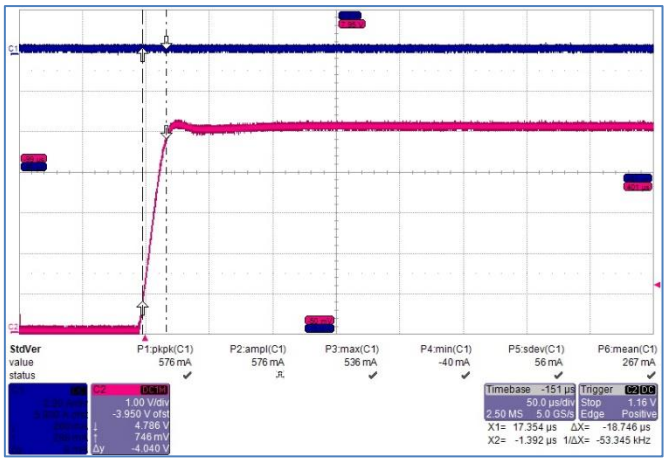


Figure 25: Step Response of VBUS with 0.39 Ω and 10 µF for a 150 cm USB Cable

5.10.3 Over Voltage Protection Circuit (OVP)

A common way for protecting the circuit from surges or incorrect input voltages caused by USB/charging cables and adapters is to add an overvoltage protection circuit (OVP). A low-cost, discrete OVP circuit has been implemented on the DA1469x DK PRO (Figure 26).

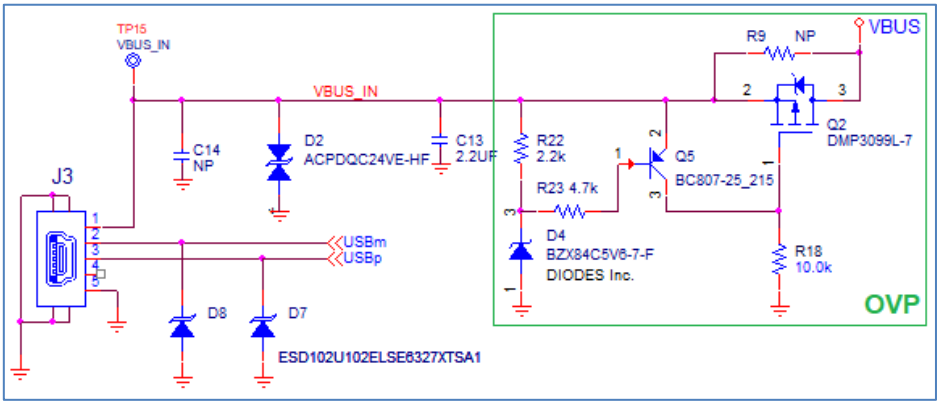


Figure 26: OVP Applied on DA1469x DK PRO

The OVP circuit supplies the DA1469x circuit if the applied voltage from an external power source is lower than a set VBUS trip voltage. The OVP circuit of the DA1469x DK PRO can provide power to the circuit for input voltages up to about 5.6 V. This guarantees smooth operation within the whole range of the USB 1.1 voltage specification (4.75 V to 5.25 V), while at the same time the voltage remains safely below the absolute maximum specifications of the DA1469x (VBUS absolute maximum voltage is 6.5 V).

The operation of the OVP circuit is based on Zener diode D4, and its response time is therefore very fast. Figure 27 presents the OVP responses for input voltages of 5 V and 20 V through a 3 m long power cable. Such a long power cable causes ringing and overvoltage. In both cases, the overvoltage of 19 V and 34 V, respectively, is rejected by the circuit. The 20 V input is also rejected by the circuit (right).

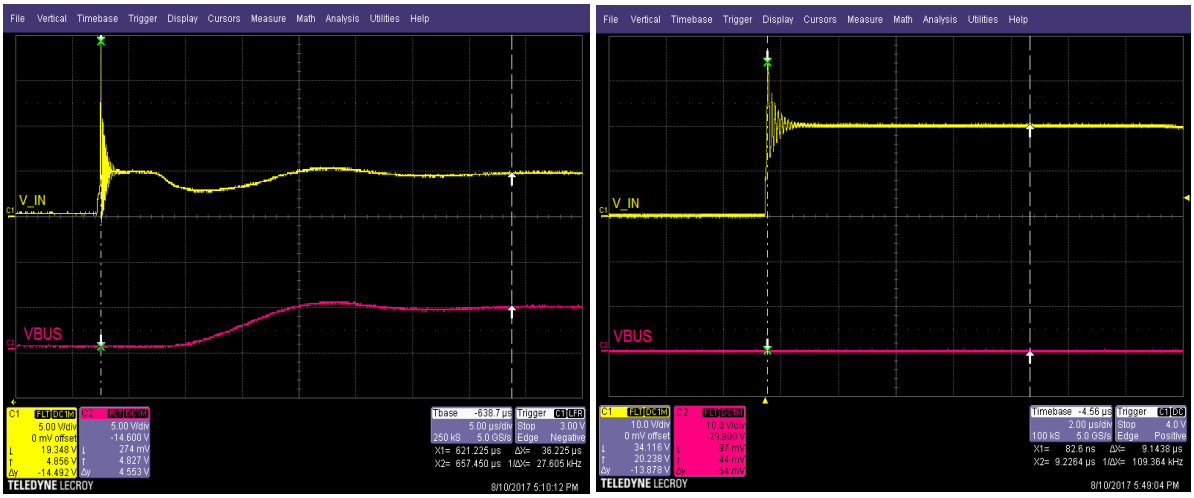


Figure 27: Vin = 5 V (Left) and Vin = 20 V (Right). Ringing Caused by Long Power Cable

There is no need for a VBUS series resistor (R2 in Figure 6) when the OVP circuit is used.

Capacitor C13 of 2.2 µF needs to be added to meet the USB certification – that is the bypass capacitor test. As per USB specification the value of the input capacitor must be from 1 µF to 10 µF. 2.2 µF has been chosen to ensure positive testing results.

This OVP circuit does not support reverse input polarity protection. A possible solution is to replace Q2 with back to back MOSFETs (Figure 28):

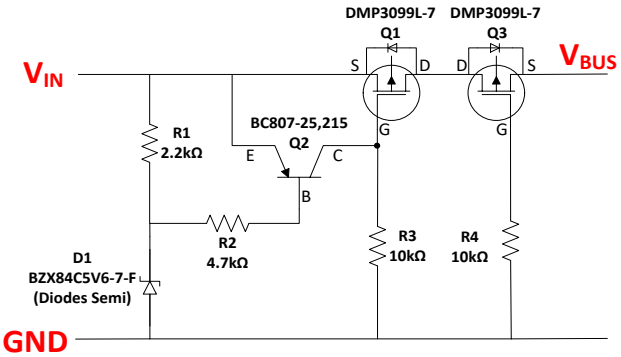


Figure 28: Reverse Polarity Protection Circuit Provided from Q3 P-Ch MOSFET

5.11 JEITA-Compliant Battery Charger

The integrated battery charger of the DA1469x SoC is suitable for several different battery chemistries (NiMH, Li-Co, Li-Mn, Li-phosphate, or NMC). It has a CC-CV (constant current, constant voltage) architecture and supports charge levels between 2.8 V and 4.9 V and charging currents from 5 mA to 560 mA. Enabling, disabling, and functional states of the charger are controlled by a HW state machine, while exceptions and error handling is done via software. The software can take over control during the charging sequence. The charger is fully integrated and requires only a buffer capacitor and optionally an NTC temperature sensor, connected on P1_00 and P0_07 for battery temperature sensing. Connections for the NTC and the suggested resistor values for charging in the temperature range of -10°C to +53°C are shown in Figure 29.

NOTE
There is no mechanism to protect the JEITA charger registers from wrong write accesses.

All essential measurements needed for the charger control (VBAT and battery temperature) are implemented in hardware without the need of utilizing ADC channels and/or SW resources. Protections for die temperature, battery temperature, overvoltage, and timeouts for the constant current, constant voltage and the total charge phases ensure a reliable and safe operation.

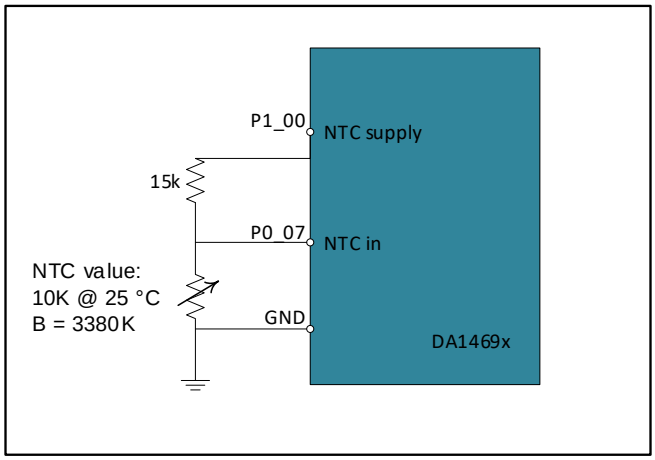


Figure 29: NTC Connections for Battery Temperature Monitoring and Suggested Values

NOTE
By default, P1_00 and P0_07 are used for UART hardware flow control: URTS and UCTS (Table 20). Assign these to other GPIOs when using the NTC. And, in the DA1469x Pro-DK board switches 3 (URTS) and 4 (UCTS) of S1 must be set to off, the lower position.

5.11.1 Charger Headroom Effect on the Charger Current

The DA1469x charger current in CC mode will increase when the charger headroom voltage drops below 0.7V (the voltage across the charger, VBUS voltage minus VBAT1 voltage). This phenomenon is called the charger headroom effect. The charger headroom effect is defined as the difference between the measured charge current at VBUS – VBAT1 > 0.7 V and the measured charge current at VBUS – VBAT1 < 0.7 V. The former measured charge current value will be close to the selected charger CC current value: *I_Charge.*

The charge current increase can be as high as 14% for charger headroom voltages down to 0.5 V and becomes important at the end of the CC charging stage, at which point the battery voltage reaches its maximum level. After switching to CV mode, the charge current gradually will decrease. Figure 30 directly below shows what is meant by the charger headroom voltage: the voltage difference between the VBUS pin and the VBAT1 pin.

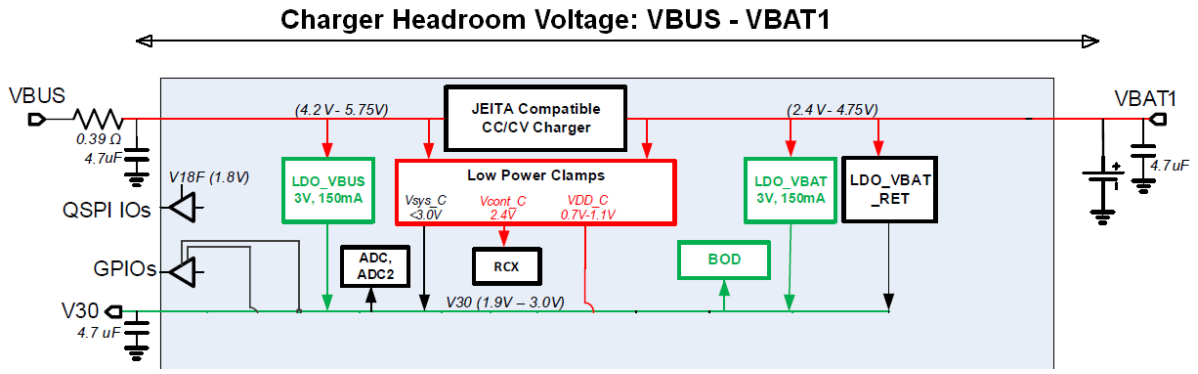


Figure 30: Charger Headroom Voltage

The headroom effect is bigger for large charge currents than for small charge currents. Find the charger headroom effect for various charge current settings in Figure 31. To keep the increase of the charger current below a few percent, the VBUS voltage must be kept above 5 V for a battery charge voltage = 4.3 V.

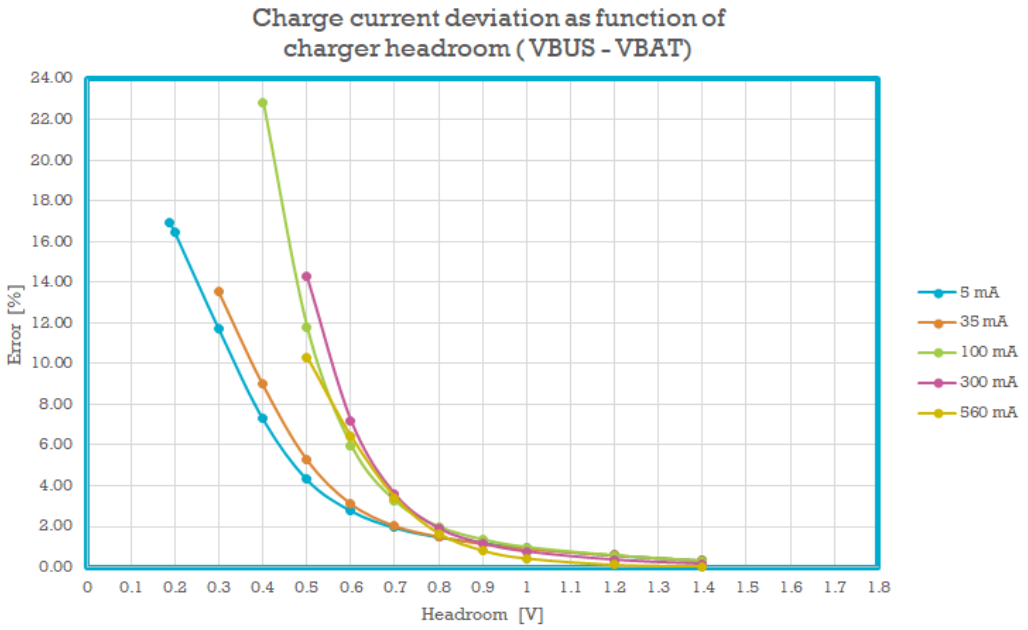


Figure 31: Charger Current Increase as Function of Charger Headroom

Knowing the charger headroom effect now, what can be done in the application to avoid a too big increase of the charge current which might lead to exceeding the battery's maximum charge current?

- Try to maintain a charger headroom voltage of at least 0.7 V
  For most Li-Ion/Li-Po batteries this means the VBUS voltage should be 5 V minimum
- Apply a lower charge current setting if possible. The headroom effect is less for small charge current values. The total charge time will increase of course
- Reduce the charge current (*I_Charge*) setting by one step, or maybe two steps, when detecting that the charger headroom becomes low and the charge current will have increased

  The applied VBUS voltage in the application is often generated by a standard third-party USB wall adaptor. Because the VBUS voltage cannot be measured directly in the DA1469x, the application software must anticipate for a worst-case voltage and switch to a lower charge current when the charger headroom voltage VBUS – VBAT1 becomes smaller than 0.7 V. A voltage of 4.5 V could be considered as the worst case VBUS voltage

For example, it could be decided to reduce the charge current (*I_Charge*) by e.g. one step, to compensate for the charge current increase, when the battery voltage VBAT reaches 4 V

The battery voltage can be measured internally (at VBAT1) by the GP-ADC and the SD-ADC in the DA1469x

5.12 Hibernation Mode and Wakeup

For shipment purposes, devices with DA1469x SoC can be put into hibernation mode, which is also called “shipping mode”. In this ultra-low power mode, there is no RAM retained, no clocks running (so no RTC), and all domains are off to minimize power consumption and to avoid discharging the onboard battery. V30 and V12 power rails are supplied from low power clamps which are programmable and can be lowered during hibernation to reduce power dissipation as much as possible.

The system can wake up from hibernation by HW Reset, Power-On Reset (POR) or Wake-Up controller (GPIO trigger).

- **HW Reset:** it is triggered by setting RSTn pin low
- **Power-On Reset (POR):** it can be triggered upon a POR timer expiration (defined on POR_TIMER_REG [POR_Time]). POR generation from GPIO is not available when DA1469x is in hibernation mode. POR generation is done from reset pad (RSTn) in hibernation mode
- **Using Wake-Up Controller (GPIO Trigger):** the Wake-Up Controller can be programmed to wake up the DA1469x from extended/deep sleep (clocked) mode as well as from hibernation (clockless) mode. It can generate three different interrupt signals:
  - KEY_WKUP_GPIO_IRQ: this interrupt signal is directed to the Power Domain Controller (PDC), as a triggering event, and the Cortex-M33 NVIC. This is a debounced IO trigger
  - PORT0_to_PDC: this interrupt signal is directed to the PMU. This is a non-debounced IO indicating a wake-up trigger from an IO toggle on Port 0
  - PORT1_to_PDC: this interrupt signal is directed to the PMU. This is a non-debounced IO indicating a wake-up trigger from an IO toggle on Port 1
  - The device wakes up from hibernation when a triggering event appears (rising or falling edge on GPIO) and starts execution as if a HW reset has occurred, since there is no retained memory. The GPIOs can be latched to any configurations (input, input pull-up, or input pull-down) and retains their states during hibernation. The wake-up can occur from different sources, such as buttons or an external controller

The wake-up controller can also be used for waking up DA1469x when a USB cable is plugged in to the device. In this case, a resistor divider from VBUS is used and the circuit schematic is shown in Figure 32. When the USB cable is plugged in to the device, the GPIO state changes (via voltage divider) from Low to High and the device wakes up from Hibernation mode (Figure 33). The voltage divider (R1 = R2 = 620 kΩ) divides USB voltage by two in hibernation mode where the GPIO is configured as input. Since this is intended to be a one-time wakeup, when the system exits hibernation mode, the application must either disable the wakeup controller on that GPIO or configure the GPIO as input pull-down (adding the internal 25 kΩ resistor in parallel to R2). This reduces the voltage divider output (below 0.2 V) and prevents the device from waking up (Figure 34) every time a USB cable is plugged in.

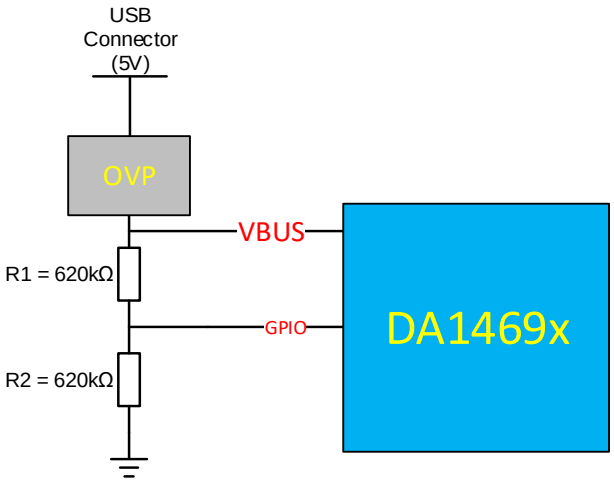


Figure 32: Wakeup from Hibernation by USB Cable Being Plugged in, Using GPIO Trigger

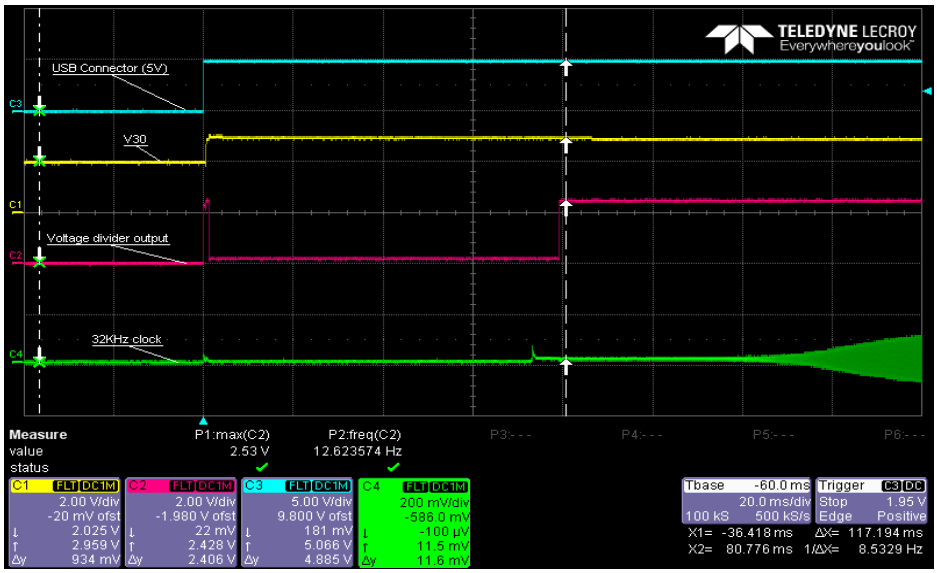


Figure 33: Set GPIO as Input

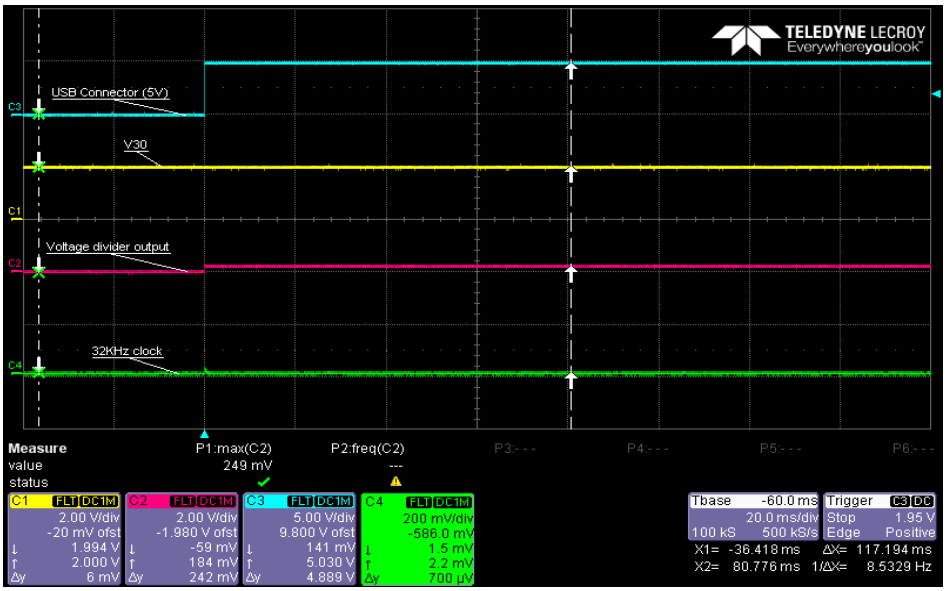


Figure 34: Set GPIO as Input Pull-Down

Note that, the DA1469x GPIO input levels are referenced to V12 (V12= 0.7 V to 0.8 V at hibernation, Table 24). When interfacing with external circuitry, avoid applying levels between V_{IH} and V_{IL} for proper operations.

Table 24: GPIO – DC Characteristics

Parameter	Description	Conditions	Min	Type	Max	Unit
V_{IH}	HIGH level input voltage	V12 = 1.2 V	0.7*V12			V
V_{IL}	LOW level input voltage	V12 = 1.2 V			0.3*V12	V

5.13 LED Driver

Two LED drivers are available on the DA14697 and the DA14699 (VFBGA100) on pins K9 and K10. They are not available on the DA14691 and the DA14695 (VFBGA86). Note that, the pins K9 and K10 for the DA14691 and the DA14695 are ground pins.

The LED driver features two matched white LED outputs with an absolute accuracy of ±5 %. It supports two solutions for brightness dimming: a selectable output load current and PWM dimming. A selectable output load changes the brightness by modifying/reducing the maximum output current. The setting is a minimum of 2.5 mA and a maximum of 20 mA with steps of 2.5 mA, meaning eight output possibilities.

PWM dimming changes the brightness by modulating the output current from 0 % to 100 % duty-adjustable pulse. The LED brightness is controlled by adjusting the relative ratios of the on and off times. The PWM operation is possible for all eight load settings instead of just for the maximum setting. The block diagram of the LED driver is presented in Figure 35. Two of these are instantiated in the system.

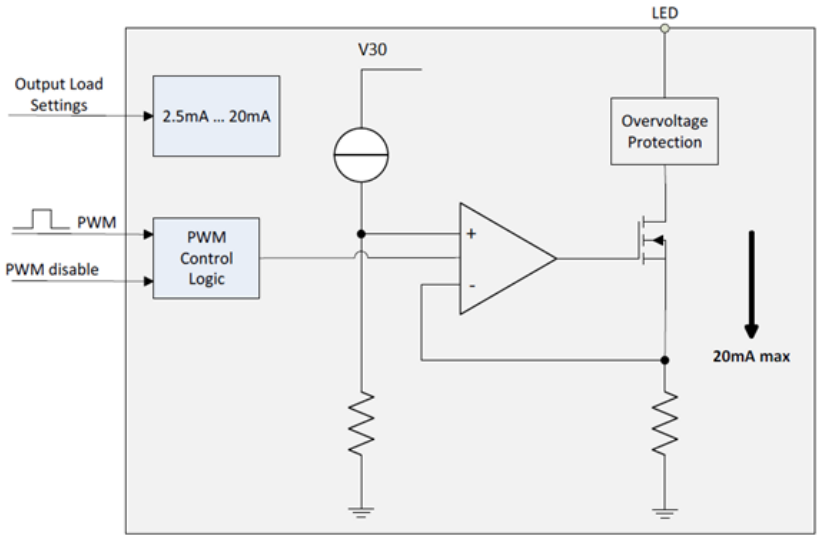


Figure 35: LED Driver Block Diagram

5.14 ΣΔ-ADC Converter

The Sigma-Delta ADC (SD-ADC) converter with 14-bit precision runs on a 1 MHz clock by default. The best dynamic range and the best accuracy is obtained by using an oversampling rate (SD-ADC_OSR) of 1024, so that the sample time is about 1 ms or about 1000 samples/sec.

The number of SD-ADC input channels depends on the chip version and package:

- DA14691/695, VFBGA86: four single-ended (SE) channels or two differential channels
- DA14697/699, VFBGA100: eight single-ended (SE) channels or four differential channels

For differential mode [SDADC_SE = 0x0], two SD-ADC inputs can be freely selected by using the registers SDADC_INP_SEL and SDADC_INN_SEL. For example, SD-ADC5 (P1_20) and SD-ADC0 (P1_09) can be selected by using [SDADC_INP_SEL = 0x5] and [SDADC_INN_SEL = 0x0].

The reference voltage can be selected to the internal 1.2 V reference or to an external voltage reference. By default, the internal reference voltage is used. The SD-ADC input voltage at the VINP input needed for a SD-ADC Full Scale (FS) reading is 1.20 V. Applying a clean and accurate external reference voltage results in a bigger dynamic range and more accurate SD-ADC results than using the internal reference voltage.

The battery voltage VBAT [SDADC_INP_SEL = 0x8] can be measured internally by applying the internal 4× attenuator which has a total resistance value of 650 kΩ. This attenuator is disconnected from VBAT when not used. Maximum allowed battery voltage for the SD-ADC input is 4.8 V.

Since the settling time increases much when the 4× attenuator is used, the SD-ADC clock frequency must be reduced to 250 kHz, which is the lowest possible SDADC_CLK_FREQ setting (SDADC_CLK_FREQ = 0x0). If the SD-ADC clock frequency is not adjusted, the SD-ADC readings will result in too low VBAT values, since the measured voltage did not have enough time to charge the internal capacitor.

5.14.1 How to Measure Input Voltages Higher than 1.2 V

There are two methods to measure an input voltage above 1.2 V:

- Method 1
  - Apply an external resistor divider, dividing higher voltages to 1.2 V maximum. The advised maximum total resistance of the divider is 100 kΩ, because an external divider with a higher resistance value and the presence of the internal parasitic capacitance would result in too long settling times

- Set the SDADC_CLK_FREQ value to the lowest possible setting: 250 kHz. Because this external divider has a relatively low resistance, it is strongly advised to disconnect the divider, or not to supply it, when it is not used and when the system is in sleep mode. The divider could be disconnected by a field-effect transistor controlled by a GPIO

- Method 2
  - Apply an external reference voltage to the SD-ADC. GPIO P0_16 is the SD-ADC external reference voltage input, VREFP, and GPIO P0_06 is the external reference negative input, VREFN, which normally is connected to ground
  - Set SDADC_VREF_SEL to 0x1 to select GPIO P0_16 and P0_06 to use the external reference voltage. For example, when an external reference voltage of 1.5 V is applied to VREFP, the SD-ADC Full Scale (FS) reading becomes VINP = VREFP = 1.5 V. No attenuator required
  - Leave the SDADC_CLK_FREQ setting at the default value of 1 MHz

  The VREFP pin allows to apply an external reference voltage up to 1.8 V. It's expected that the chip's lifetime and its reliability will not be degraded or affected for voltages up to 1.8 V. But note that, the SD-ADC characteristics and performance are guaranteed for a 1.2 V reference voltage only.

  The external reference voltage input also can be used for accurate temperature measurements using an NTC network (Figure 36). The supply voltage of the NTC network is also fed to the SD-ADC external reference voltage input. It results in accurate NTC temperature measurements, because the measurement is not dependent on the actual level of the supply voltage. For a certain temperature, the ratio of the NTC value and the RT value is always the same, and so is the ratio of VINP and VREFP. Thus, at the same temperature, the SD-ADC reading is always the same: the ratio of VINP/VREFP, even when the NTC supply voltage varies.

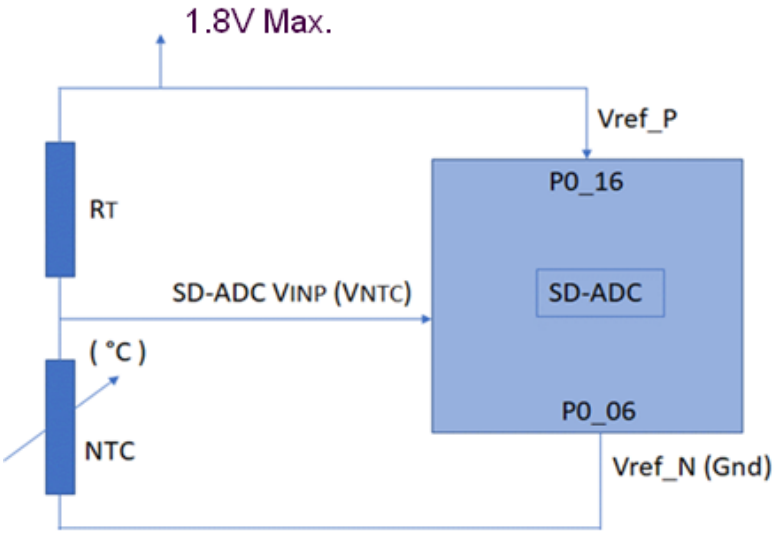


Figure 36: Accurate NTC Temperature Measurement with the SD-ADC

5.15 RFIO Port

The DA1469x provides a single ended RFIO port matched to 50 Ω. The RFIO port consists of the RFIOp and RFIOm pins, where RFIOm is connected to ground.

A copper trace with a characteristic impedance of 50 Ω connects the RF port and the antenna.

Figure 37: RF Matching Circuit must be Placed as Close as Possible to the Antenna

A pi-network (Z2, Z1, Z3) is added for antenna matching purposes (Figure 38). This antenna matching-network must be placed near the antenna feed point.

An additional, optional pi-network (Z5, Z4, Z6) placed near the RFIO port is added for TX harmonics filtering when the TX output power is set to +6 dBm. In some cases, it might be needed to apply such a low-pass filter, although the DA1469x chip has been trimmed for a minimum second harmonic level.

RF-connector J7 can be used for conducted RF tests, using the muRata RF-cable MXHS83QE3000.

Some recommendations to minimize transmission losses between radio IC and antenna in the PCB layout:

- Minimize the transmission line length between radio IC and antenna
- The characteristic impedance of the transmission line should match the required radio impedance (50 Ω)
- Place antenna matching components (Z1, Z2, Z3) as close as possible to the feed point of the antenna
- Make sure that the component's GND are connected on the same GND plane (right hand side in Figure 37)

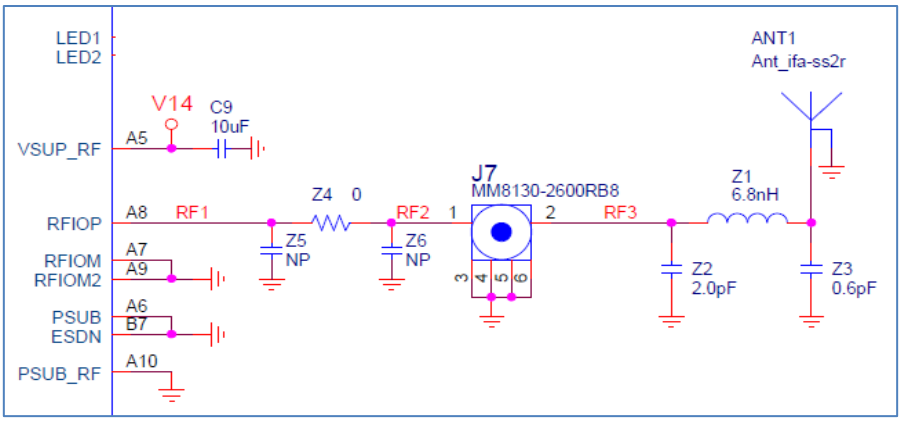


Figure 38: RFIO Circuit

5.15.1 Antennas and General Considerations

Consider the following points before adding an antenna to the design:

- Do not place metal layers below the antenna itself. The antenna footprint must be kept free of metal

- Do not place metal screws, radiators, piezo buzzers, batteries, etc. in the proximity of the antenna
- As a rule of thumb, at least 5 mm should be allowed around the antenna footprint, both horizontally on the PCB and vertically around the PCB footprint
- Do not use metal enclosures for products with antennas. Metal enclosures prevent the antenna from radiating and performing as intended
- Refer to Dialog's Application Note AN-B-027 [2] for designing printed antennas

5.16 PCB Layout

The PCB layout of the DA1469x Soc mainly depends on the chip's package. Due to the fine pitch and the number of pins in the VFBGA100 package, it requires a denser microvia approach. For the larger VFBGA86 package, a cheaper PTH-via approach can be adopted.

5.16.1 PCB Footprint

The VFBGA100 package has a pin-to-pin pitch of 0.475 mm, whereas the VFBGA86 pitch is 0.550 mm. The copper pad diameter used on DA1469x DK Pro is 0.205mm. As the ball diameter is 0.250 mm, the size of the copper pad is sufficient for proper soldering of the chip in a Non Mask-defined pad configuration. In addition, for the VFBGA86, this scheme provides enough space for routing a 0.145 mm trace between two pads.

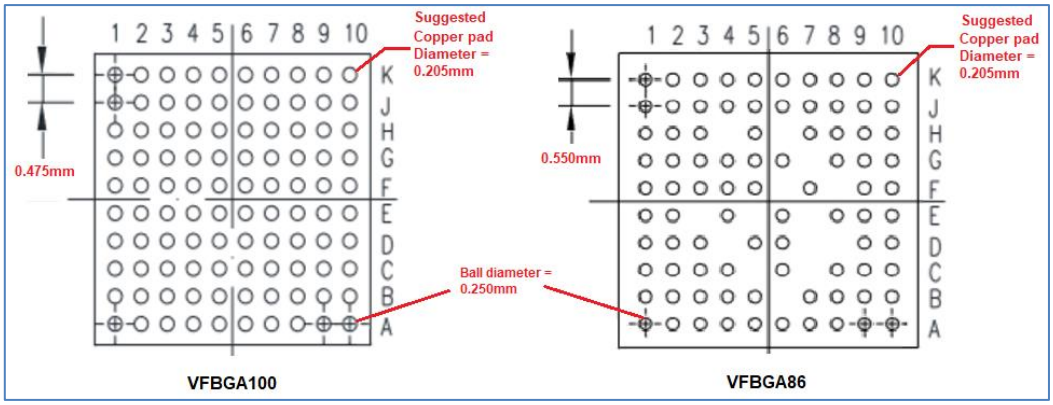


Figure 39: Bottom View of Packages VFBGA100 (Left) and VFBGA86 (Right)

5.16.2 Microvias or PTH Vias

Microvias, and especially microvias on chip pads, make board design easier because of their small size. Copper filled vias offer low DC resistance. The thickness of the dielectric layer depends on the microvias aspect ratio (hole diameter to microvias depth), which is determined by PCB manufacturers' capability. For example, for an aspect ratio of 1:0.8, if the drill diameter of a microvia is 100 µm, the dielectric layer cannot be thicker than 80 µm.

The cost of producing a PCB with microvias is higher than producing a PCB with PTH vias. For copper filled vias, cost and production time are significantly higher.

5.16.3 Generic PCB Layout Guidelines

Generic guidelines for the DA1469x PCB layout are:

- Active components operating at high frequency should have layouts as compact as possible to prevent the cross-coupling between lines and to minimize the parasitic effects which has negative impacts on the operating parameters
- Always provide a solid grounding to the radio IC. Use as many vias as possible to create a solid GND under the IC itself and connect the IC to inner and bottom GND layers

- Remove GND under the pads of high speed and fast switching power components, such as QSPI data flash, power inductor, and crystals

The layout and PCB routing considerations for QSPI data flash are:

- Place QSPI data flash as close as possible to the chip
- Add decoupling capacitor next to power pin
- Route traces with equal length if possible
- Have solid ground under traces
- Ensure the safe distance between traces to avoid crosstalk

The layout and PCB routing considerations for RF layout is:

- It is important to properly route the RF strip line to the antenna. The design of RF GND is also important. See Section 5.15

The layout and PCB routing considerations for XTAL are:

- Place the XTAL32M as close as possible to the IC to minimize additional capacitive load on the input pins and to reduce the chance of crosstalk and interference with other signals on the board
- Remove GND area under XTAL pads (Figure 40)
- If possible, try to create a ground shield around the crystals. XTAL32M ground is connected to the three XTAL32M GND balls (Figure 41)

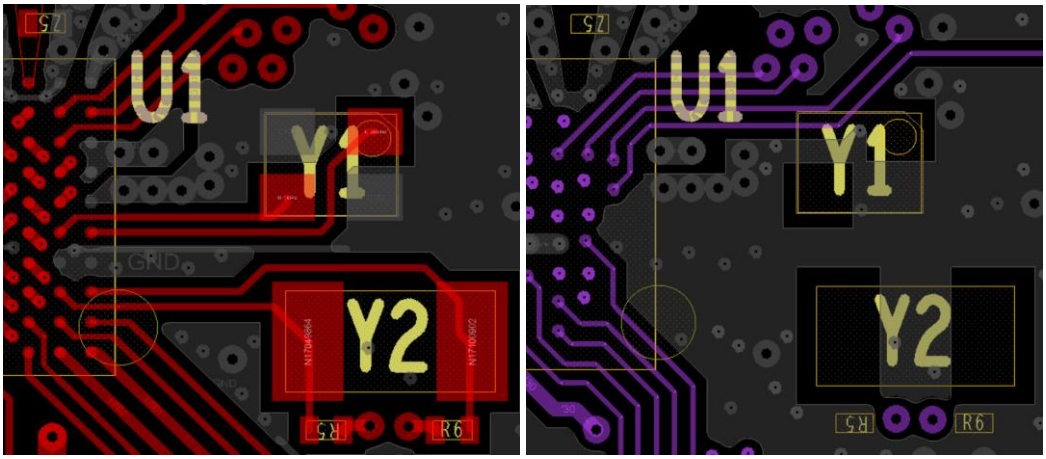


Figure 40: Remove Copper on Internal Layer (Right) under XTAL

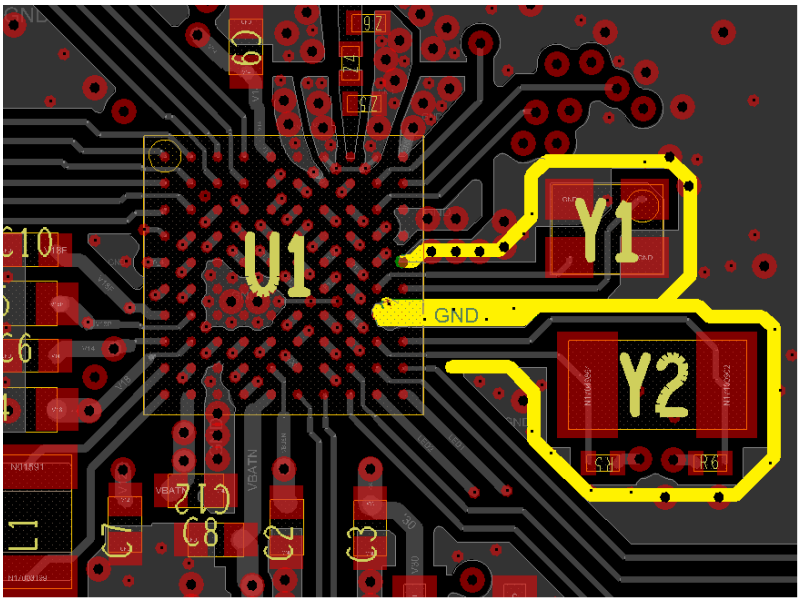


Figure 41: XTAL Grounding

ESD considerations: Consider the following points for a good ESD performance of your applications. Also see Section 5.10.1 for ESD measures on the USB connector.

- If charger contact pins are used, place an ESD protection device directly between the two charger connections, VBUS and ground. ESD testing according IEC 61000-4-2 means that ESD shooting at the charger contact pins will be done
- Isolate XTAL32M ground connections from the ground used by the ESD protection devices
- It is strongly advised to connect the battery ground terminal to the same ground point or ground plane as the VBUS ground connection
- If a GPIO or the antenna can be touched by users, provide an ESD protection device for them
- Protected signal lines should be routed directly to the transient-voltage-suppression diode. Ground connections should be made directly to the ground plane for minimizing parasitic inductance
- For connectors, transient-voltage-suppression device should be placed as close to the connector as possible to reduce transient coupling into nearby traces. The secondary effects of radiated emissions can cause upset to other areas of the board, even if there is no direct path to the connector

5.16.4 PCB Layout for VFBGA100 Package

High density interconnect (HDI) PCB structure is required for the VFBGA-100 package where microvias are used. Here we take the PCB of DA14697/9 where all signals are extracted as an example (Figure 42). This is a PCB of six layers in a 1-1-2-1-1 configuration. Microvias of 250 µm – 100 µm are used between layers Top (L1) – L2 and L2- L3 as well as between L4 to L5 and L5 to Bottom (L6). No buried vias are used. PTH vias are 460 µm – 200 µm (pad diameter – drill diameter).

- On the top-L1 layer, the signals of the external row of the pins are routed
- Layers L2 and L3 are used for routing the pins of the internal rows (signal and power)
- Layer L4 is the reference GND plane
- Layers 5 and 6 are used for signal and power traces routing

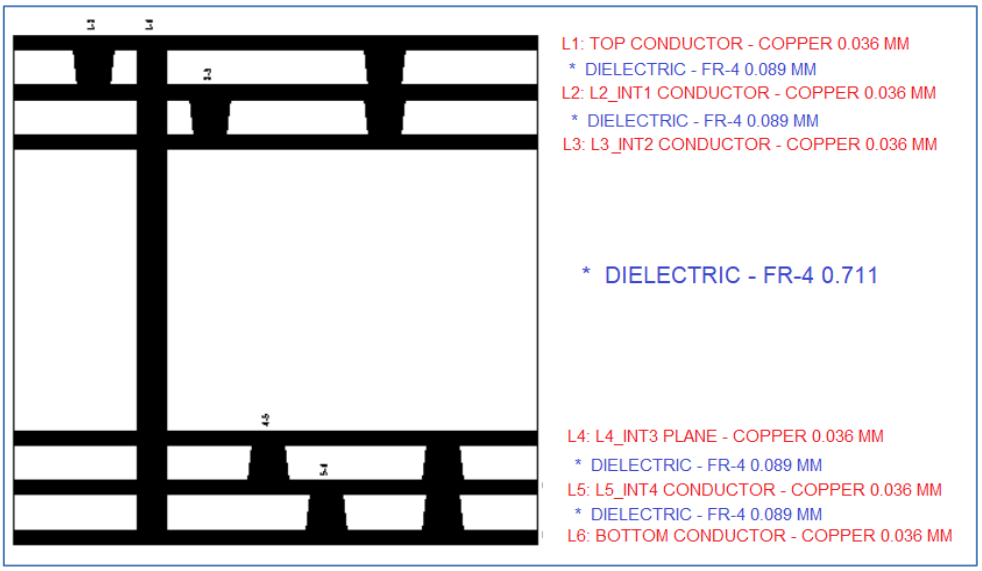


Figure 42: PCB Cross Section for VFBGA100 Package

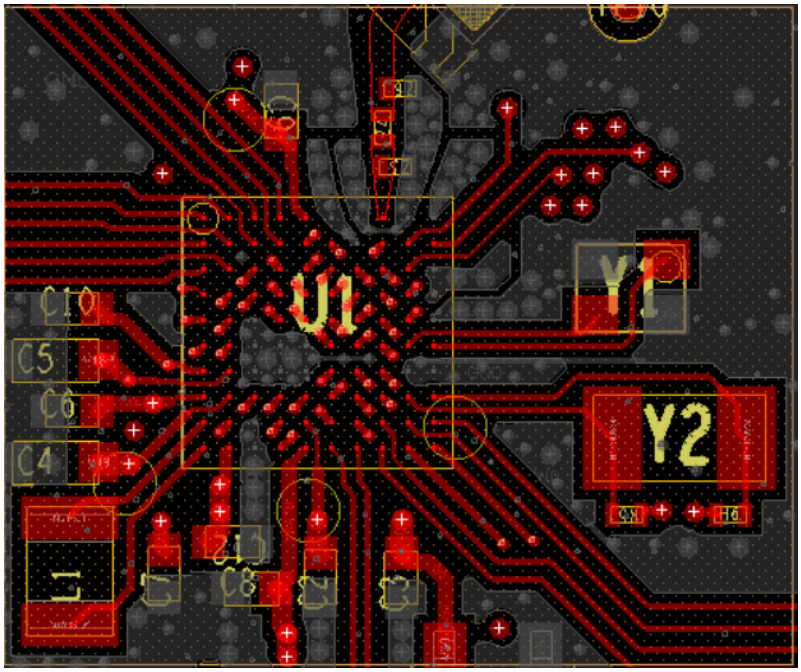


Figure 43: VFBGA100 PCB Layout, L1, Top Side

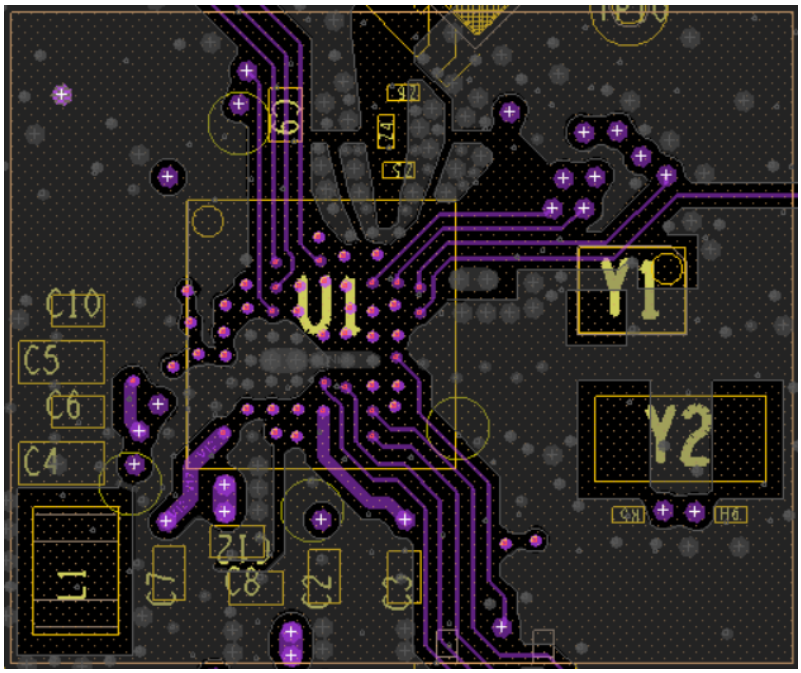


Figure 44: VFBGA100 PCB Layout, Layer L2

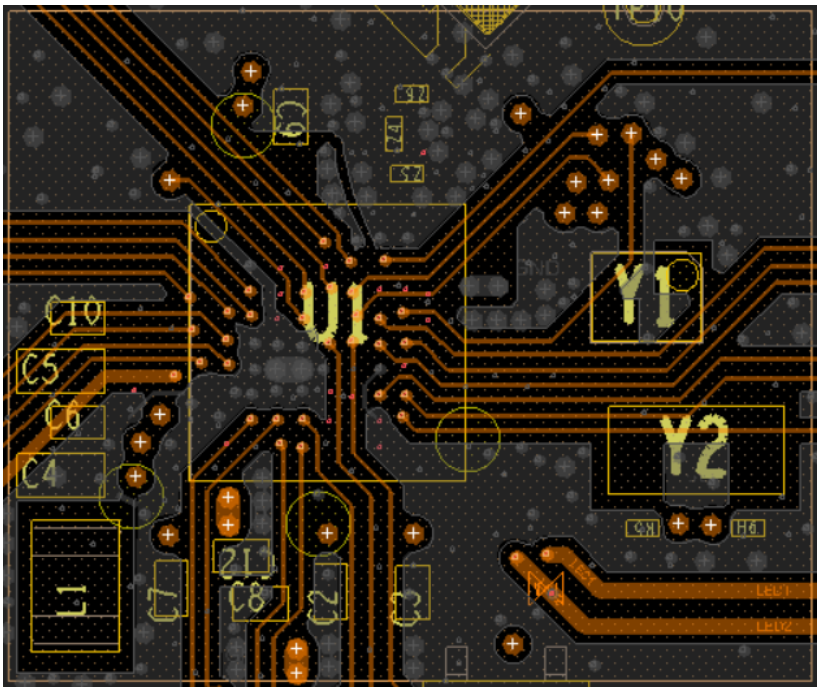


Figure 45: VFBGA100 PCB Layout, Layer L3

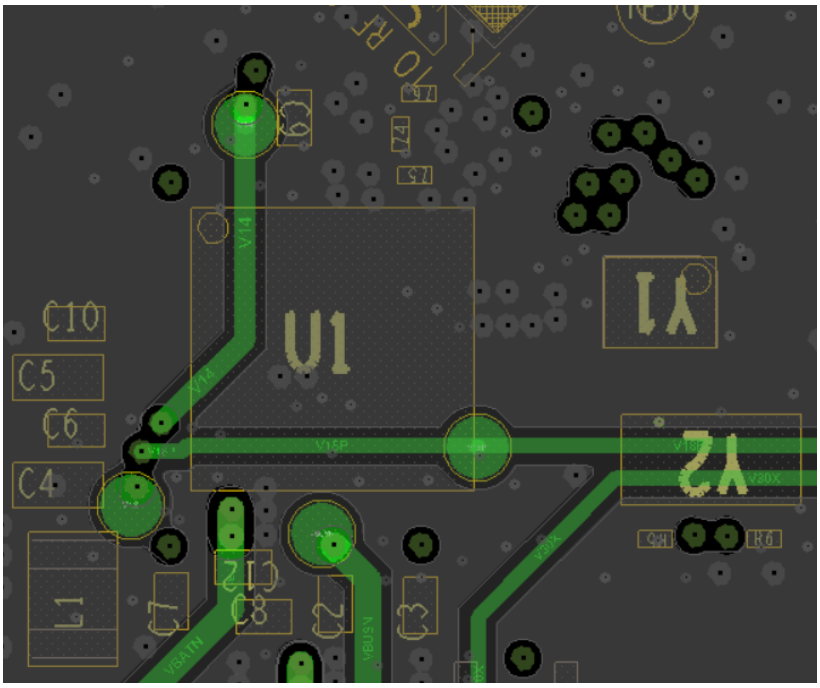


Figure 46: VFBGA100 PCB Layout, Layer L4 Reference Ground

A good PCB design practice is to have controlled impedance of the routed traces, for example, 60 to 80 Ω. The trace impedance referred to L4 gets higher due to the distance from the three other layers. So, the traces should be much wider to obtain the desired impedance. The solution to this is to arrange traces in each layer in a way that they have ground reference to the nearest other layer, for example, traces in layer L2 can refer to ground on L1 or L3.

Users need to pay special attention to the routing of the GND pins of theDA1469x SoC. PSUB/PSUB_RF/ESDN are noisy. whereas RFIOM, RFIOM2, GND_RF1, GND_RF2, and XTAL32M_GND are sensitive. The most sensitive ground pin is ball E10 for the XTAL32M which lies next to the GND_RF1/RF2 ground pins. Always try to keep these two groups separated (Figure 47).

- RFIOM/RFIOM2, GND_RF1/GND_RF2, and PSUB_RF signals are separated on top-L1 and L2 layers and they are shorted together on L4
- XTAL32M_GND is separated to GND_RF1 and GND_RF2 for top-L1, L2, and L3. They are shorted together on L4
- The indicated ground groups have direct connection to the reference ground (L4) with mechanical through vias
- 50 Ω microstrip line for the antenna is referred to layer L3

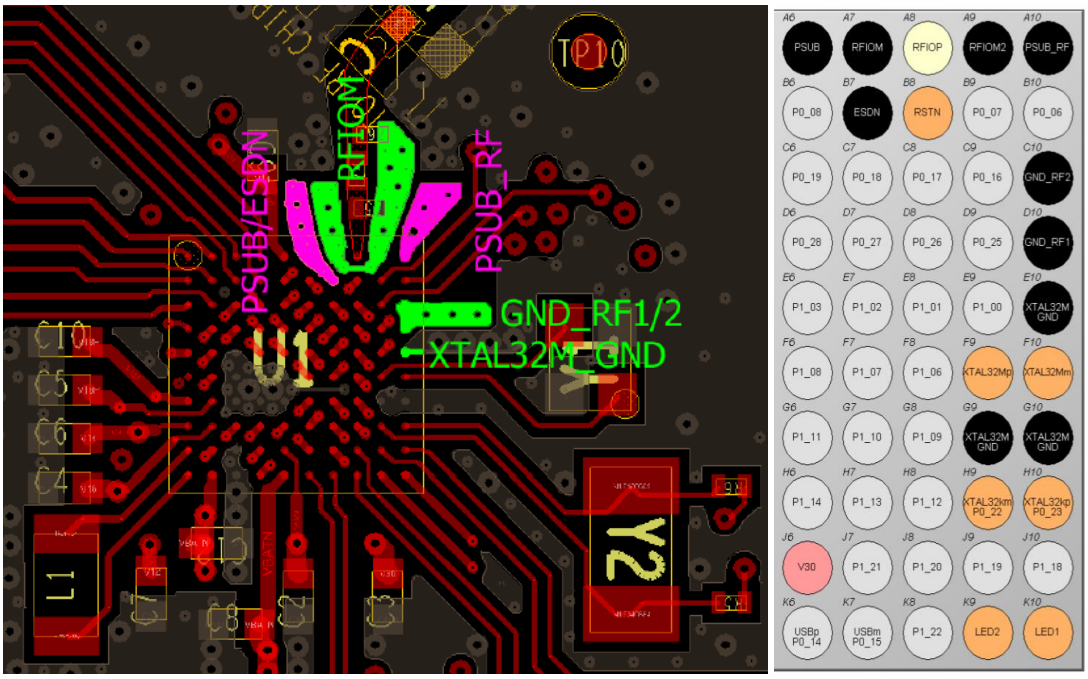


Figure 47: VFBGA100 Ground Connectivity Top (Left) and Pins Location on Chip (Right)

5.16.5 PCB Layout for VFBGA86 Package

VFBGA86 package has a pitch of 0.55 mm. Because pads with a diameter of 200 µm are used, it is feasible to route traces between pads, so the PCB layout for the VFBGA86 package is done in four layers without microvias. The PTH vias are 460 µm – 200 µm (pad diameter/drill diameter).

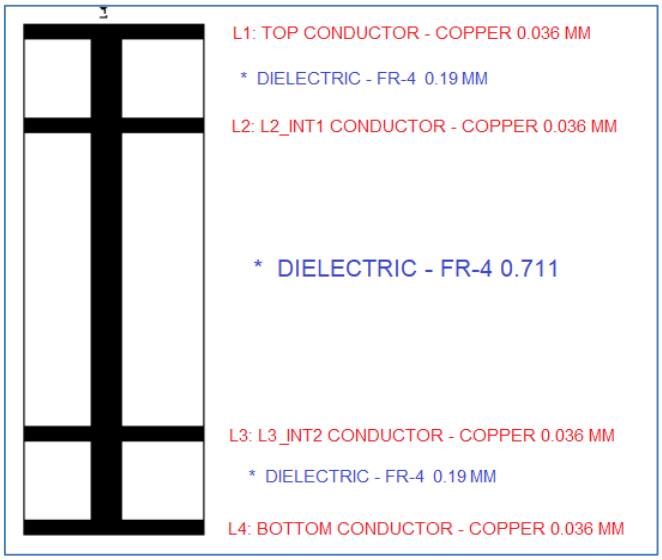


Figure 48: PCB Cross Section for VFBGA86 Package

- On the top-L1 layer, the signals of the external two rows are routed
- Layer L2 is used for routing the pins of the internal rows (signal and power)
- Layer L3 is the reference GND plane
- Layers 4 is used for signal and power traces routing

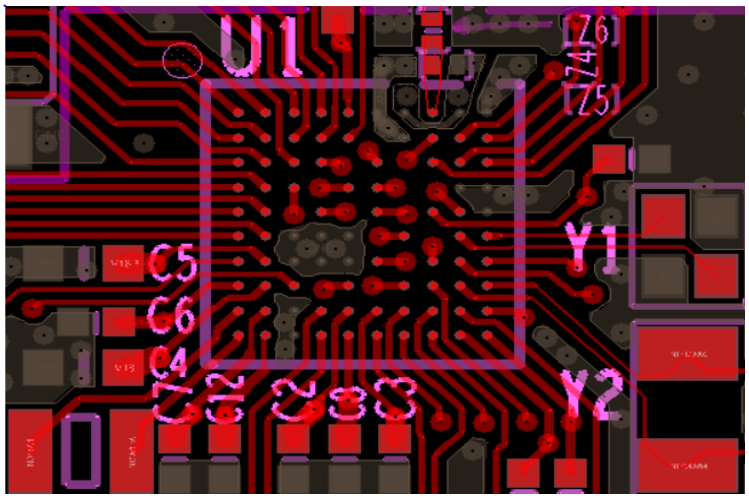


Figure 49: VFBGA86 PCB Layout, L1-Top Layer

A good PCB design practice is to have controlled impedance of the routed traces, for example, 60 to 80 Ω. The trace impedance referred to L3 gets higher due to the distance (0.936 mm) from the two other layers. So, traces should be much wider to obtain the desired impedance. The solution to this is to arrange traces in each layer in a way that they have ground reference to the nearest other layer, for example, traces in layer L2 can refer to ground on L1 or L3.

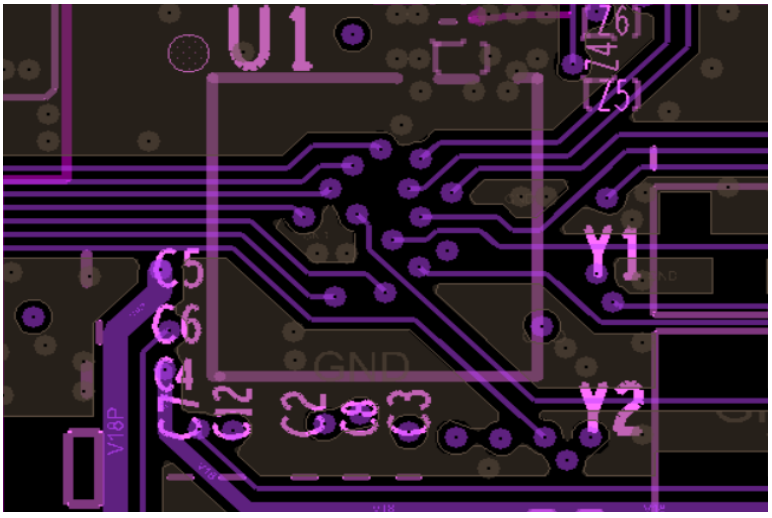


Figure 50: VFBGA86 PCB Layout, L2 Layer

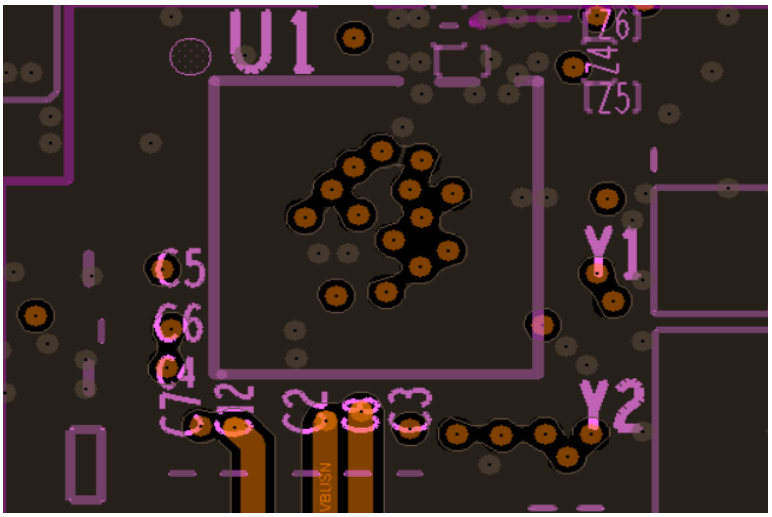


Figure 51: VFBGA86 PCB Layout, L3 Layer, Reference Ground

Users need to pay special attention to the grounding of the following pins:

- RFIOM and RFMIO2 are shorted together on top-L1 layer, separated from other ground pads and plane. They are connected to the GND plane on L2 layer (second layer)
- ESDN and PSUB are shorted together on top-L1 layer, separated from other ground pads and plane. They are connected to the GND plane on L2 layer (second layer)
- PSUB_RF is separated from other ground pads and plane on top-L1 layer. It is connected to the GND plane on L2 layer (second layer)
- 50 Ω microstrip line for the antenna is referred to layer L2

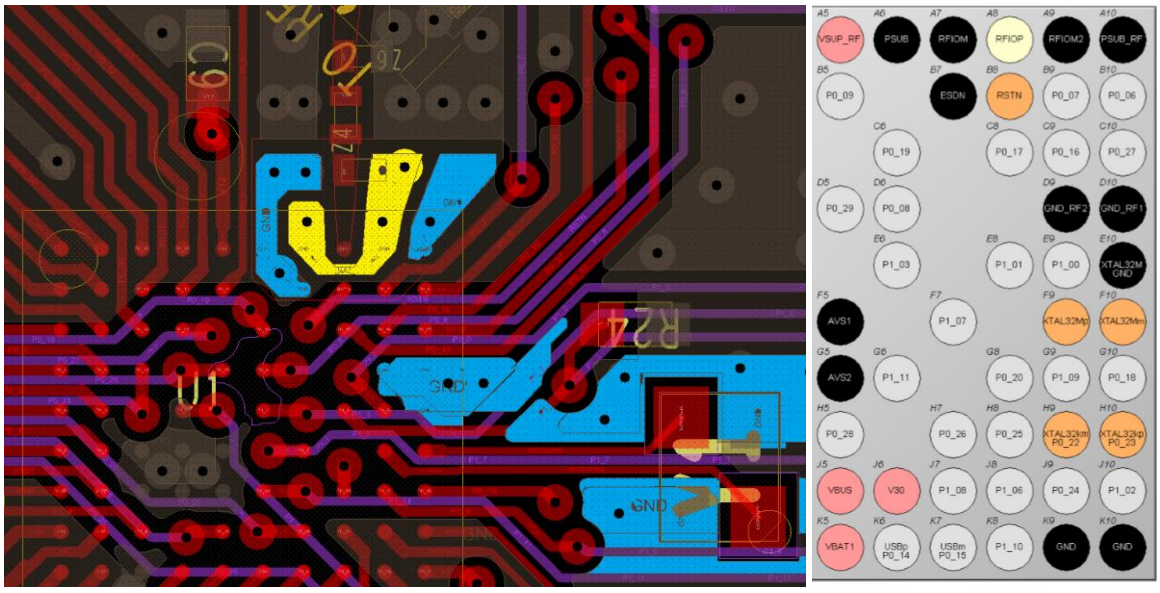


Figure 52: VFBGA86 Ground Connectivity Top (Left) and Pins Location on Chip (Right)

5.17 Package Outline Drawing for VFBGA100 and VFBGA86

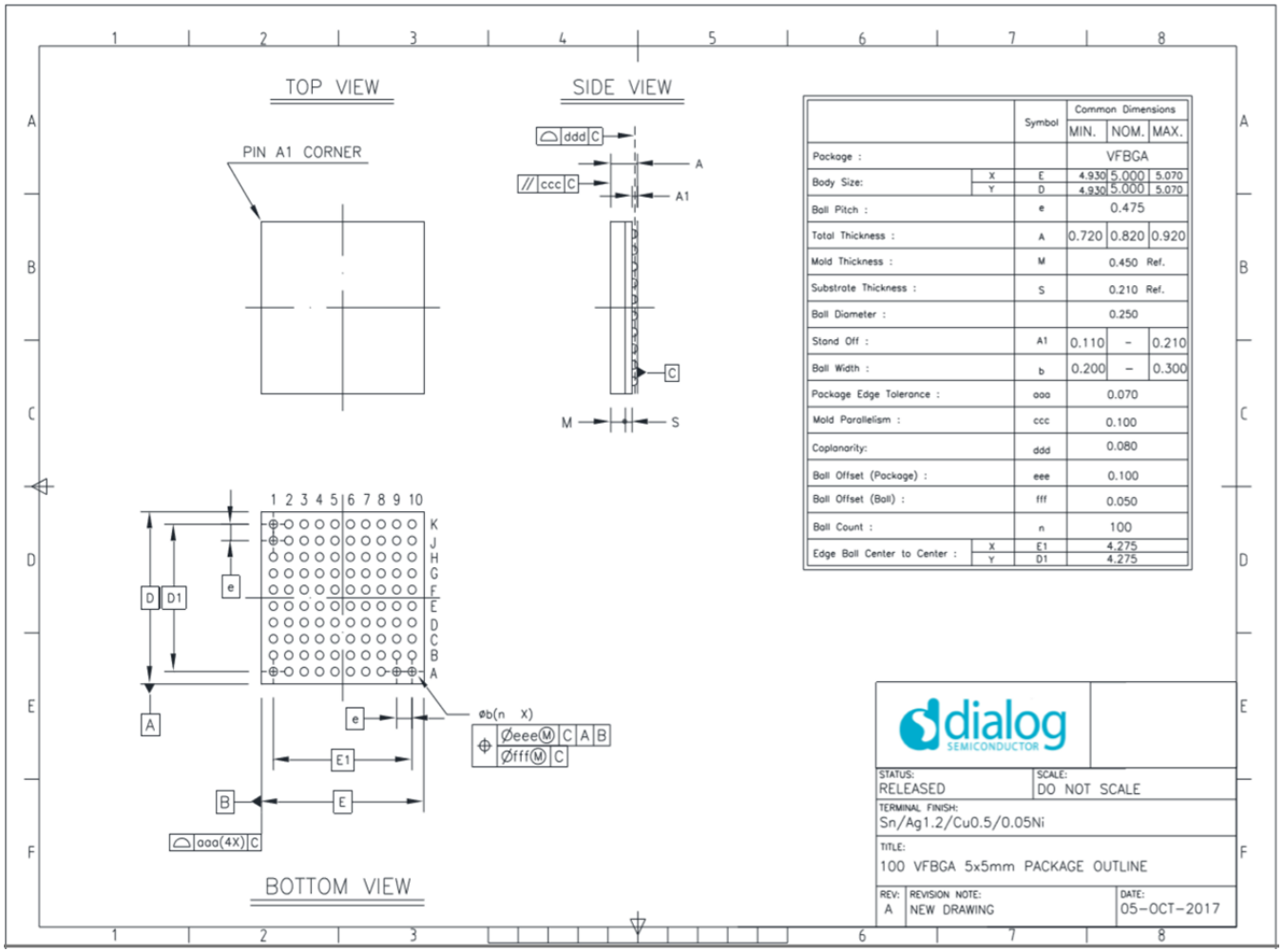
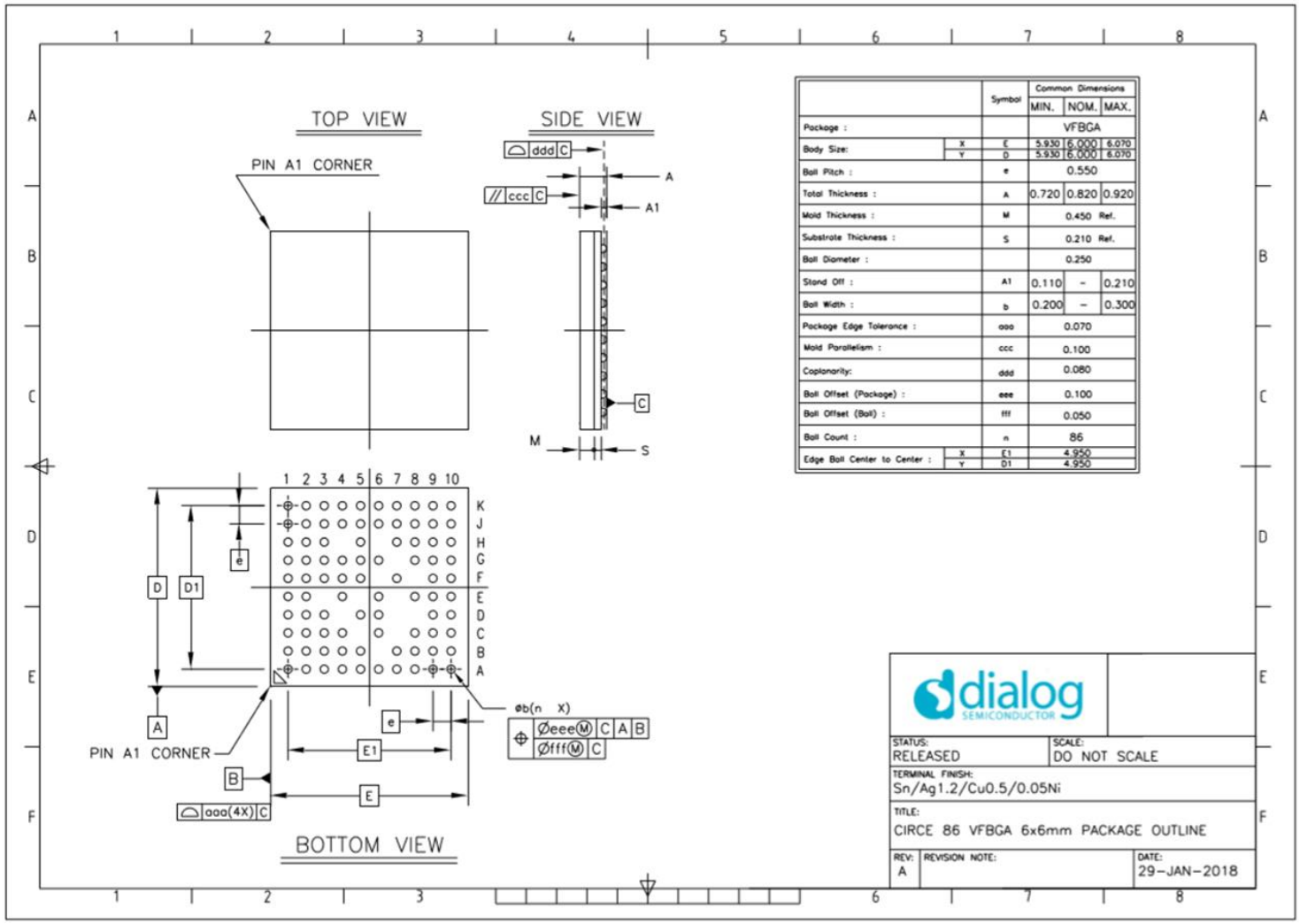


Figure 53: POD for VFBGA100



		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package :				VFBGA	
Body Size:	X	E	5.930	6.000	6.070
	Y	D	5.930	6.000	6.070
Ball Pitch :		e		0.550	
Total Thickness :		A	0.720	0.820	0.920
Mold Thickness :		M		0.450 Ref.	
Substrate Thickness :		S		0.210 Ref.	
Ball Diameter :				0.250	
Stand Off :		A1	0.110	–	0.210
Ball Width :		b	0.200	–	0.300
Package Edge Tolerance :		aaa		0.070	
Mold Parallelism :		ccc		0.100	
Coplanarity:		ddd		0.080	
Ball Offset (Package) :		eee		0.100	
Ball Offset (Ball) :		fff		0.050	
Ball Count :		n		86	
Edge Ball Center to Center :	X	E1		4.950	
	Y	D1		4.950	

Figure 54: POD for VFBGA86

Appendix A : Hardware Files Deliverables

For system familiarization, comprehension, testing, and software development, Dialog Semiconductor provides DA1469x hardware development kits:

- PRO-daughterboard, VFBGA100: 2522-db-vfbga86_[331-19-x], Figure 55
- PRO-daughterboard, VFBGA86: 2522-db-vfbga100_[331_06-x], Figure 55
- PRO-motherboard: 2522-mb-pro_[331-07-x], Figure 56
- DA14695 USB kit: 2522_devkt-b-usb_[331-22-x], Figure 57

Deliverables related to the DA1469x hardware development are available to users for speeding up the DA1469x system design and development:

- Design files:
  - Schematic of DA1469x DK PRO, in PDF and Cadence Capture CiS
  - PCB Layout files of DA1469x DK PRO in PDF and Cadence Allegro SPB 16.6
- Manufacturing files:
  - Gerber files
  - ODB++ file
  - Bill of materials (BOM)
    Links to design documents on the Dialog DA1469x Website:
  - https://www.dialog-semiconductor.com/products/da14695-development-kit-pro
  - https://www.dialog-semiconductor.com/products/da14695-development-kit-usb

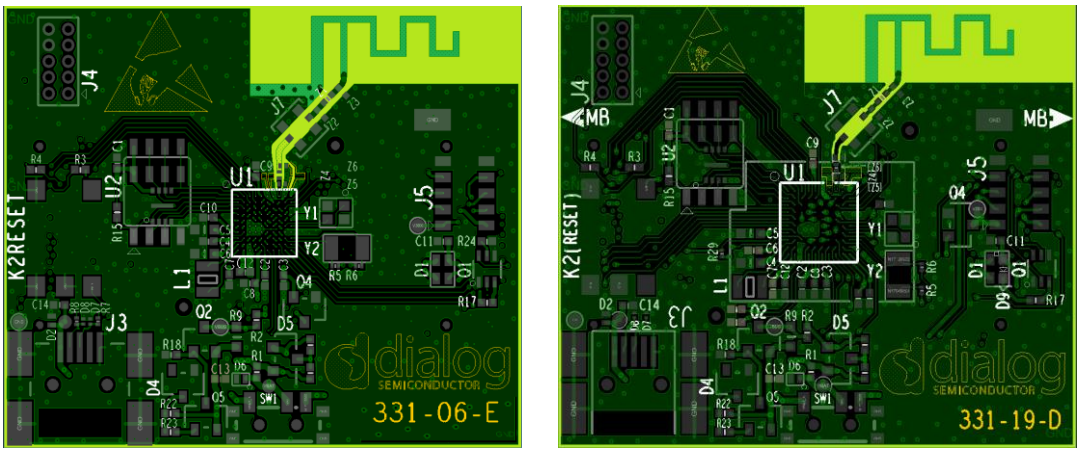


Figure 55: PRO-DB D2522-db-vfbga100_331_06-x (Left) and D2522-db-vfbga86_331-19-x (Right)

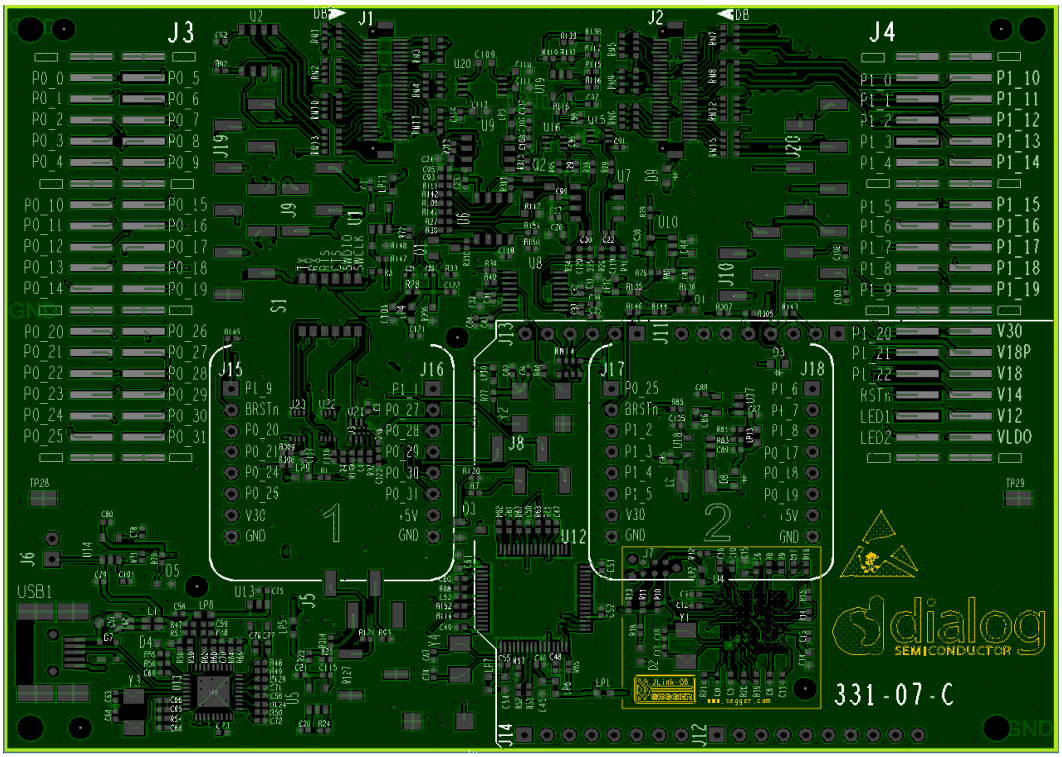


Figure 56: DA1469x DK Pro Motherboard: 2522-mb-pro_331-07-x

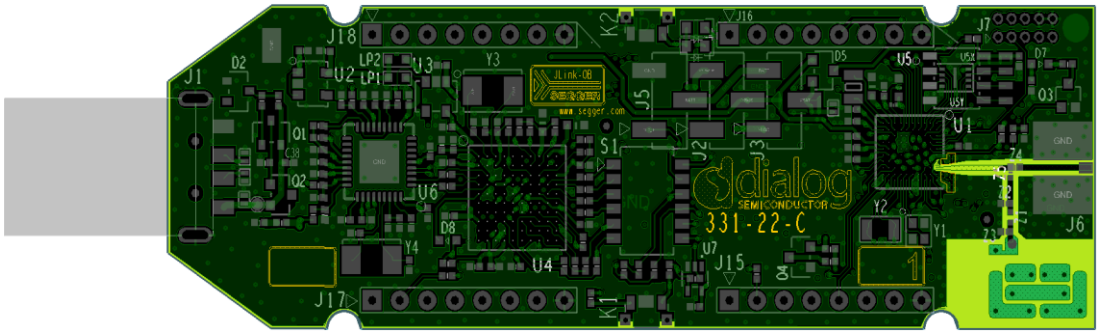


Figure 57: DA14695 USB Kit: 2522_devkt-b-usb_331-22-x

Appendix B : Reflow Soldering Profile

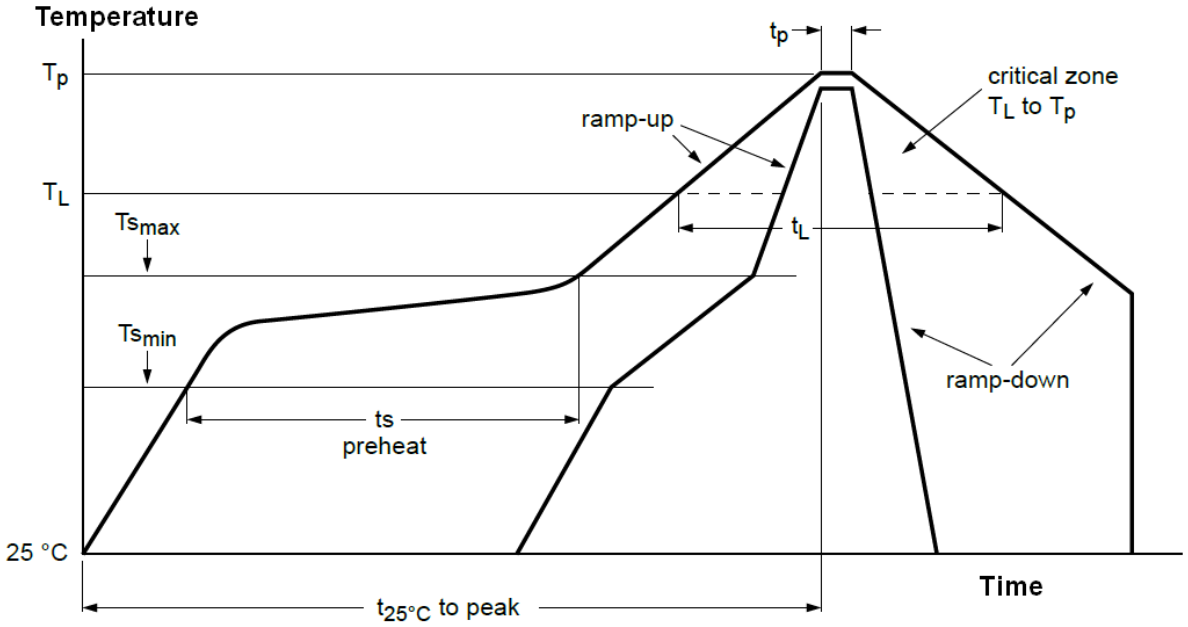


Figure 58: Soldering Profile

Table 25: Soldering Profile Limiting Values Based on IPC/JEDEC J-STD-020E [4]

Profile Feature	SnPb eutectic assembly	Pb-free assembly
Average ramp-up rate (Tsmax to Tp)	3 °C/sec maximum	3 °C/sec maximum
Preheating		
Temperature minimum (Tsmin)	100 °C	150 °C
Temperature maximum (Tsmax)	150 °C	200 °C
Time (ts: Tsmin to Tsmax)	60 to 120 seconds	60 to 120 seconds
Time (tL) maintained above TL		
Liquidous Temperature (TL)	183 °C	217 °C
Time (tL)	60 to 150 seconds	60 to 150 seconds
Peak package body temperature (Tp)	235 °C (> 215 °C)	255 °C (> 235 °C)
Time within 5 °C of actual peak temperature (tp)	10 to 30 seconds	20 to 40 seconds
Ramp-down rate	6 °C/sec maximum	6 °C/sec maximum
Time 25 °C to peak temperature	6 minutes maximum	8 minutes maximum

Revision History

Revision	Date	Description
1.8	24-Nov-2022	BOD Section 5.3.2 updated.
1.7	21-Jan-2022	Updated logo, disclaimer, copyright.
1.6	30-Jul-2021	SD-ADC Section 5.14.1: correction of the maximum allowed voltage applied to the external reference pin of the SD-ADC. Added information on external pull-up resistor connections in Section 5.4. Added Section 5.3 about BOD.
1.5	20-Jun-2020	Small additions and corrections, e.g. Figure 2.
1.4	20-Feb-2020	Added a note that the JEITA charger registers are not protected from wrong write accesses, in section 5.11. Corrected Table 11 (.textual: VFBGA87 Pins Location). New Arm® product branding applied.
1.3	20-Sep-2019	Revised section 5.1.2. Parts of section 5.3 have been restructured and revised. Added trim limitations for 32 MHz crystals with CL= 4 or 8 pF in 5.5.1. Added 4 examples of DCDC inductors: Table 7. Added 3 examples of 32 MHz crystals: Table 13. Added another 32.768 KHz crystal: Table 15. Updated the list of supported QSPI Flash chips: Table 23. Soldering profile added: Appendix B.
1.2	27-May-2019	Update Figure 6 Added paragraph 5.11.1 (Charger Headroom Effect)
1.1	06-Mar-2019	Corrected sensitivity and budget link
1.0	22-Feb-2019	Initial version.

DA1469x Application Hardware Design Guidelines

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

RoHS Compliance

Dialog Semiconductor's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.