

Calculating Maximum Processing Rates of the PDC (HSP50214, HSP50214A and HSP50214B)

Introduction

Configuring the Programmable Digital Downconverter (PDC) requires selecting clock, decimation and interpolation rates for the various filter sections. Each filter section has limitations due to the hardware implementation. Furthermore, the input and output rates of the various sections must match in order for the composite configuration to be valid. In many cases, there may be multiple configurations that will yield the desired composite conversion and filter. In a few applications, a particular hardware constraint or specification will drive the complete configuration. This application note reviews the application of system requirements to the PDC, details the hardware constraints, introduces design approaches to the PDC, and then details the hardware constraints; section by section.

The input sample rate, CLKIN, is 52MHz, for the original part and 65MHz for the A and B mask revisions. The PROCCLK rate is 35MHz on the original part and 55MHz for the A and B mask revisions. Calculations for the A and B versions will be given in brackets following the calculation for the original part. REFCLK is a local reference input that can be used to phase lock the PDC output sample rate to local clocks. External clock recovery loop filters are required to process the PDC "Timing Error" into a valid Resampler NCO control input. Since the rates of the PDC output and the local clocks can be different, refer to the Polyphase Filters and Interpolating Halfband Filters section for guidance in selecting the NCO and REFCLK frequencies.

Mapping System Constraints into PDC Configuration

Three system parameters that will drive the PDC configuration are: 1) IF frequency, 2) the Bandwidth of Interest, and 3) the baud rate of the baseband data. This section details the first pass design configuration of the PDC based on these three system parameters. Once this first pass is completed, the remaining information in this application note will be used to optimize the PDC design configuration.

System Input Specifications

The IF frequency and the Bandwidth of Interest are used to set the minimum input sampling frequency, f_s , of the PDC. Considerations are: 1) A/D Full Power Input Bandwidth, 2) the maximum clock rate of the A/D converter, and 3) the 52MHz maximum PDC input sampling rate. If the IF frequency is in the upper portion of the A/D bandwidth and that bandwidth is greater than the maximum sample rate of the A/D or PDC, then use of undersampling techniques to process a lower frequency sampling alias of the IF signal should be considered. This is illustrated in Figure 1.

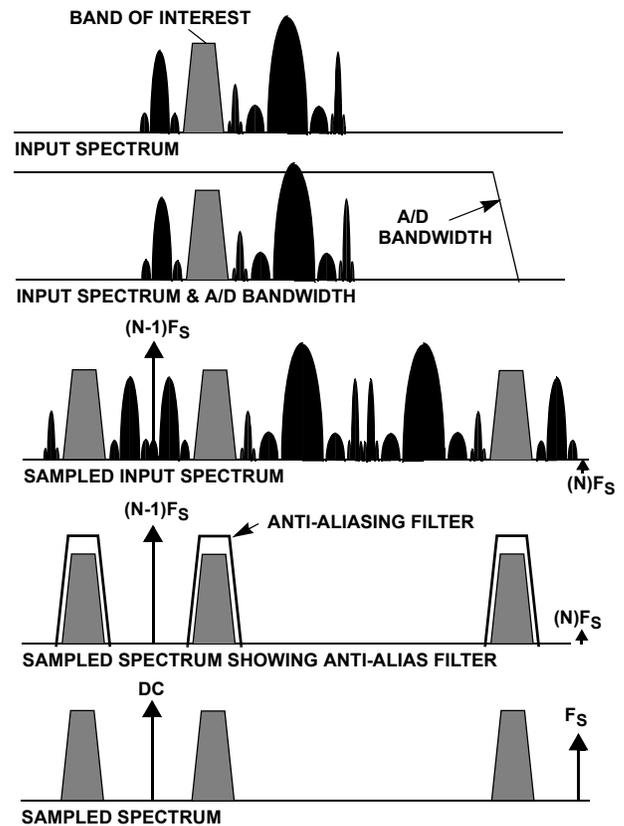


FIGURE 1. CONSIDERING IF FREQUENCY, A/D BANDWIDTH, AND ALIASING IN SELECTION UNDERSAMPLING

If the IF is in the lower portion of the A/D bandwidth and is below the maximum rate of the A/D and the PDC, then traditional oversampling techniques should be considered. This is illustrated in Figure 2. In both cases, consideration of signals outside the band of interest, but inside the A/D converter bandwidth must be considered to avoid alias interference or reduction of dynamic range. The design of the IF alias filter (bandwidth, rolloff, rejection and cost) will be an important part of this consideration. It is likely that selecting the input sampling rate to meet the Nyquist rate for the bandwidth of interest and the spectral purity requirements, will involve reviewing several frequency plans with a variety of sampling frequencies.

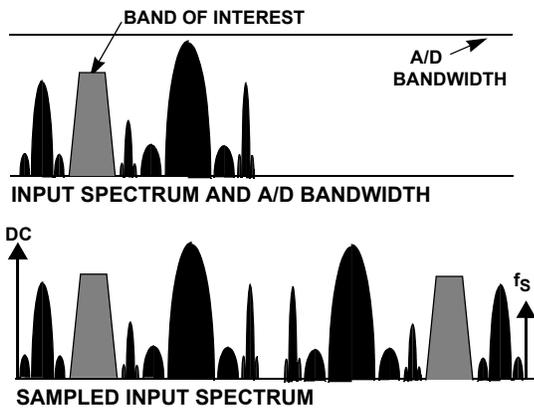


FIGURE 2. CONSIDERING IF FREQUENCY, A/D BANDWIDTH, AND ALIASING IN SELECTION

Hardware Constraint Overview

System Output Specifications

The system output specifications that affect the configuration of the PDC are the baseband baud rate and/or baseband bandwidth. The baud rate or equivalent low pass bandwidth sets the PDC output sample rate or the minimal PDC bandwidth. In some digital systems the baseband output rate is required to be a submultiple of the A/D converter sample rate. The relationship between input and output sampling rate, or total decimation is fixed and must be distributed among the various filter elements while creating a composite filter meeting the low pass bandwidth and the PDC hardware constraints. The detailed section of this document will provide the possible decimation rates for each filter section.

The 255 tap FIR filter input sampling rate should be set at greater than or equal to twice the lowpass bandwidth, since this is the narrowest filter section in the PDC. If use of even one stage from the Halfband filter is required, then the 255 tap FIR filter input sampling rate should be set at greater than or equal to four times the lowpass bandwidth, to minimize the alias effects on dynamic range. Setting the 255 tap FIR filter input rate sets the number of PROCCLKS available for filter calculations, and thus determines the number of filter taps possible.

The Halfband filter input sample rate is set at 2^N times the FIR input sample rate, where N is the number of halfband filter stages active. Note that each halfband stage will decimate by 2.

The CIC filter input is sampled at f_s , so it must provide a decimation of f_s/F_{HBIN} . The CIC filter also affects the dynamic range. At a bandwidth of 1/8 the CIC output sample rate, the CIC filter provides 84dB of dynamic range. At a bandwidth of 1/10 the CIC output sample rate, the CIC filter provides 96dB of dynamic range. At a bandwidth of 1/12 the CIC output sample rate, the CIC filter provides 100dB of dynamic range.

With the FIR, halfband filter, and CIC rates set, two checks must be performed to validate this first pass PDC

configuration: 1) the composite dynamic range - set primarily in the CIC and Halfbands, and 2) the number of clocks required for filter calculation must be met. Information provided in the detailed filter sections will provide the parameters needed to complete these checks.

Hardware Constraint Overview

This section provides an outline overview of the clocking and timing constraints of each major functional block in the PDC. More details on these constraints can be found in the respective section of this application note, or in the HSP50214 Data Sheet [1]. The intention of this outline overview is to introduce the reader to timing issues that should be kept in mind as the detailed sections of the PDC data sheet and this application note are studied.

1. Summary of Rate and Bandwidth Constraints

The PDC contains a set of very flexible filter blocks. Each filter set offers a unique design feature. The CIC offers a broad passband and initial broad stopband capability. The Halfband offers sample rate reduction and bandwidth reduction in multiples of 2. The 255 tap FIR offers high resolution filter response shaping and contouring. The Polyphase Re-Sampling FIR offers non-integer rate changes. The Interpolation HalfBand filters offer oversampling. The discriminator FIR offers bandwidth reduction. Figure 3 summarizes the rate changes (in terms of decimation) and bandwidth adjustments that occur in the various filter blocks of the PDC.

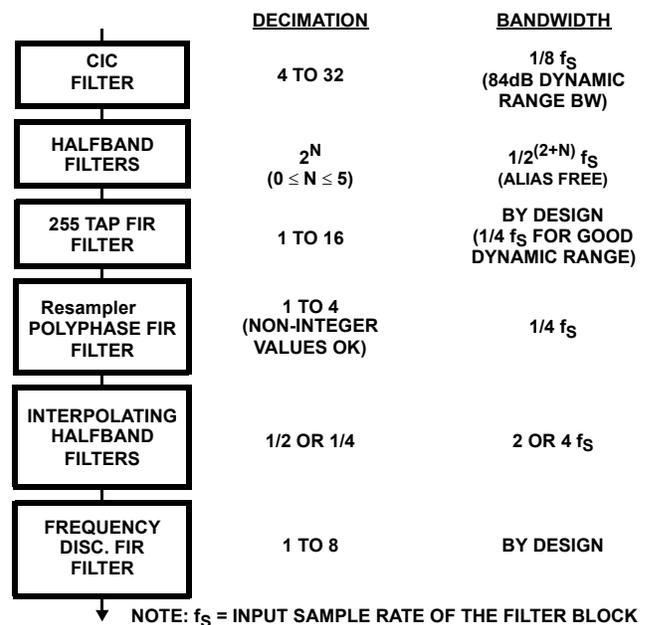


FIGURE 3. OVERVIEW OF RATES AND BANDWIDTHS

2. CIC Filter

- a) Input Sample Rate: CLKIN. $\leq 52\text{MHz}$ [$\leq 65\text{MHz}$]
- b) Compute Clock: CLKIN. $\leq 52\text{MHz}$ [$\leq 65\text{MHz}$]
- c) Decimation Range: 4 to 32.
- d) Filter Characteristics See Table 1

TABLE 1. CIC FILTER CHARACTERISTICS

FREQUENCY (f _{CIC_Out})	PASSBAND ATTENUATION (dB)	ALIAS ATTENUATION (dB)
/4	4.6	52
/5	2.9	63
/6	2.0	72
/8	1.1	85
/10	0.72	96
/12	0.50	105

If the CIC is bypassed, the sync circuitry requires that the $\overline{\text{EN1}}$ signal drop low, then go high to pass data from the CIC input to the output.

For wide output bandwidths, some emphasis of the higher frequencies in the programmable FIR may be needed to flatten the passband.

3. Halfband Filters

- a) Input Sample Rate: Equal to the output sample rate of the CIC Filter Section.
- b) Compute Clock: PROCCLK. $\leq 35\text{MHz}$ [$\leq 55\text{MHz}$]
- c) Number of Stages: 0 to 5.
- d) Decimation: 2 Number of stages, (each stage decimates by 2).
- e) Filter Characteristics:
 - i) Halfband filters have very flat passband responses.
 - ii) The passband attenuation of each filter stage is -6dB at 1/4 the input sample rate for the stage (i.e., the attenuation is -6dB at the folding frequency of the output spectrum).
 - iii) Filter characteristics - alias attenuation: See Table 2

TABLE 2. CIC FILTER ALIAS ATTENUATION

	f _{OUT} /2	f _{OUT} /4	f _{OUT} /8	f _{OUT} /16	f _{OUT} /32	f _{OUT} /64
HB5	6dB	105dB	102dB	110dB	>110dB	103dB
HB4	6	50	>110	>110	>110	>110
HB3	6	40	88	>110	>110	>110
HB2	6	32	66	104	>110	>110
HB1	6	25	48	72	98	>110

- f) When all five halfbands are enabled, the alias attenuation for the filters align as follows: f_{OUT}HB1/64 = f_{OUT}HB2/32 = f_{OUT}HB3/16 = f_{OUT}HB4/8 = f_{OUT}HB5/4.
- g) The filter computation requirements (per input sample): HB5 requires 7 clocks; HB4 requires 6 clocks; HB3 requires 5 clocks; HB2 requires 4 clocks; HB1 requires 3 clocks.
- h) When cascading filters, the computational requirements are: [(clocks for last filter) + 2 * (clocks for second to last filter) + 4 * (clocks for third to last filter) + ...]/2^(number of filters - 1). For example, using HB5, HB4, and HB3, the number of processing clock (PROCCLK) cycles needed per input sample to the Halfband Filter Section is: (7 + 2*6 + 4*5)/(2³⁻¹) = 9.75.

The HB filter input sample rate is required to be less than PROCCLK by an amount determined by the number of halfband filters selected. The range of the divisor is 3 to 9.75 (See Table 8 and 8A in the HB Filter Section). **NOTE: If the Halfband is bypassed, decimation may be required in the 255 tap FIR filter to lower the sample rate to the PROCCLK/6 requirement of the AGC.**

4. 255 Tap FIR

- a) Input Sample Rate: Equal to the output rate of the halfband filter block.
- b) Compute Clock: PROCCLK $\leq 35\text{MHz}$ [$\leq 55\text{MHz}$].
- c) Decimation: 1 to 16.
- d) The maximum number of taps is 255 for a symmetric filter, 128 for an asymmetric filter, and 64 for a complex filter.
- e) The number of taps available depends on the processing clock, the input sample rate, and the symmetry of the filter. See Table 3.

TABLE 3. DETERMINING THE NUMBER OF FILTER TAPS

FILTER TYPE	EQUATION FOR NUMBER OF FILTER TAPS
Real, Symmetric, Even # Taps	[PROCCLKS/f _{SAMP} /R] - R]*2
Real, Symmetric, Odd # Taps	[(PROCCLKS/f _{SAMP} /R) - R] - 1]*2
Real, Asymmetric	[PROCCLKS/(f _{SAMP} /R) - R]
Complex	[PROCCLKS/f _{SAMP} /R] - R]/2

Where CLKS = PROCCLK divided by the output sample rate of the FIR (quotient truncated to nearest integer) and R is the decimation factor.

- f) Each coefficient bits has 22 bits.

Filter bypass is achieved by setting the center tap to 1 and taps C₋₁ and C₁ to zero. A rule of thumb for the largest number of taps that can be achieved is:

$$(\text{PROCCLK}) / (f_{\text{FIROUT}}) - R \times 2 \text{ Number of Taps} \quad (\text{EQ. 1})$$

5. AGC

- a) Input Sample Rate: Equal to the output sample rate of the programmable FIR.
- b) Compute Clock: PROCCLK $\leq 35\text{MHz}$ [$\leq 55\text{MHz}$].
- c) Decimation: None.
- d) The processing clock must be at least 6 times the input sample rate of the AGC.

The AGC requires 6 PROCCLKS to process data - **always**. The AGC functional bypass can be effected by setting the upper and lower AGC limits to an identical number. The bypass mode still requires 6 PROCCLKS to complete the calculation.

6. Resampler Filter and Interpolating Halfband Filters

- a) Input Sample Rate: Equal to the output sample rate of the programmable FIR PROCCLK.
- b) Compute Clock: PROCCLK $\leq 35\text{MHz}$ [$\leq 55\text{MHz}$].
- c) Decimation: 1 to 4, NCO controlled, non-integer allowed.

- d) The coefficients are fixed.
- e) The output sample rate is controlled by the Resampler NCO. The Resampler NCO is 32 bits and is updated at the Resampler input sample rate. The output frequency is: $f_{IN} * N/2^{32}$, where f_{IN} is the input sample rate for the block, N is the 32-bit control word (unsigned, 0 to $2^{32}-1$).
- f) The spacing between output samples varies between $1/f_{IN}$ and $2/f_{IN}$.
- g) The resampling process produces a higher noise floor than the other filters due to the filter response and the aliasing of the filtered interpolation images.
- h) Filter characteristics: See Table 4.

TABLE 4. RESAMPLER FILTER CHARACTERISTICS

FREQUENCY (* f_{IN})	AMPLITUDE (dB)
0	0
0.125	-0.24
0.25	0
0.375	-2.6
0.5	-9.6
0.625	-24.2
0.75	-67.6
0.875	-62.4

- i) The bandwidth of the signal into the Resampler should be less than $f_{IN}/4$ to minimize aliasing.
- j) All band selection filtering should be done before the Resampler.
- k) The Resampler and Interpolation Halfband filter use the same compute engine. The number of processing clocks per input sample required for the possible filter configurations are shown in Table 5.

TABLE 5. PROCESSING CLOCK REQUIREMENTS FOR THE RESAMPLER AND INTERPOLATING HALFBAND FILTERS

CONFIGURATION	PROCESSING CLOCK CYCLES PER INPUT SAMPLE
Resampler	6
Resampler + 1 HB Filter	13
Resampler + 2 HB Filters	23
1 Halfband Filter	7
2 Halfband Filters	17
Bypass	0

- l) When the Resampler is used, the number of processing clock cycles is actually per output sample, but at decimation factors close to 1.0, the filter buffer may overflow due to a long string of computations.

7. Cartesian to Polar Coordinate Converter

The Coordinate converter requires 17 clocks to yield 16 bits of accuracy on the phase and magnitude outputs. If new input samples arrive prior to the completion of 17 clock cycles, the calculation is terminated and the interim result is latched with reduced resolution. The minimum accuracy possible is approximately 5.5 bits for magnitude and 6.5 bits for phase.

8. Discriminator FIR Filter

- a) Input Sample Rate: Equals the output sample rate of the resampler/halfband block.
- b) Compute Clock: PROCCLK ≤ 35 MHz [≤ 55 MHz].
- c) Decimation: 1 to 8.
- d) The maximum number of taps is 63 for a symmetric filter and 32 for an asymmetric filter.
- e) The equations for calculating the number of taps available, (which is dependent on the processing clock, the input sample rate, and the symmetry of the filter) are shown in Table 6.

TABLE 6. CALCULATION DISCRIMINATOR FIR TAP NUMBER

	SYMMETRIC, EVEN # OF TAPS	SYMMETRIC, ODD # OF TAPS	ASYMMETRIC
# of available taps	$2 * (CLKS - R)$	$2 * (CLKS - R) - 1$	$CLKS - R$

Where CLKS = PROCCLK divided by the output sample rate of the FIR (quotient truncated to nearest integer) and R is the decimation factor.

- f) Each coefficient bits has 22 bits.
- g) The frequency detection is done by delaying and subtracting (modulo 2π) the phase value from the cartesian to polar conversion block ($d\Phi/dt$). The delay can range from 1 to 8 samples. At a delay of one, the range of the discriminator is $\pm(f_{IN}/2)$. As the delay increases, the range decreases. For example, at a delay of 3, the detection range is $\pm(f_{IN}/6)$.
- h) There is a phase multiplier (modulo 2π) block preceding the $d\Phi/dt$ calculation that can multiply the phase by 1, 2, 4, or 8 to remove phase modulation before frequency detection. The phase multiplication restricts the discriminator range by factors of 1, 2, 4 or 8.
- i) The signal should be limited to a bandwidth less than the detection range of the discriminator or there may be frequency wrap around (aliasing).
- j) In the A and B versions of the HSP50214, the delayed and subtracted phase, the magnitude, or the I output of the Resampler/Halfband block can be selected as the source for the input of the discriminator FIR. (See the HSP50214A/B Data Sheets.

The Discriminator FIR filter output is provided at the discriminator input sample rate, so that if the filter is decimating, multiple data outputs will result until the decimation requires the next output sample to appear. DATARDY is asserted time aligned with and at the same rate as the data type selected for the AOUT output.

Design Approaches for the PDC

The PDC contains an NCO/Mixer and six filter blocks which can be configured for various applications. A natural question to ask about the PDC is “What is the maximum operation rate?” Because there are three internal clocks: CLKIN for the front end blocks; PROCCLK for back end blocks; and the Re-Sampling NCO clock for the Re-sampling polyphase FIR, Interpolating Halfband filters, and output blocks, the answer is not so simple. Likewise, determining the maximum output bandwidth can be somewhat complex. A top level approach to PDC configuration is necessary to understand and to maximize the many features of each filter block in this very flexible downconverter.

1. Begin with the FIR

The 255 tap FIR is a very important filter element in the PDC because of all the PDC filter elements it provides the most flexibility in establishing spectral shaping and complying with the out of band rejection, passband bandwidth and transition band specifications. The FIR establishes the narrowest bandwidth in the downconverter, and thus its output rate is related to the Nyquist rate of the bandwidth of interest in any application. Three design parameters, 1) out of band rejection, 2) transition bandwidth, and 3) number of taps, offer three degrees of design freedom in approaching a digital downconverter. These three degrees of freedom allow optimizing dynamic range, sample rates, number of filter taps and out of band rejection throughout the filter blocks in the converter. All three approaches begin with the FIR filter design. Many of the requirements for the FIR filter are set by the transmit baseband filtering.

The first design approach fixes the number of taps and varies the out of band rejection and transition band until a compliant design is implemented. The fixed number of filter taps may be set because of some clocking restraint of one of the filter blocks in the PDC or somewhere in the overall system.

The second design approach sets an out of band specification and varies the number of filter taps or the transition band to create a compliant design.

The third design approach sets a fixed transition band specification and varies the number of filter taps and the out of band rejection, to create a compliant design. An overview of these three approaches is illustrated in Figure 4.

The 255 tap FIR should be designed to have an output bandwidth no greater than 1/4 of the FIR input sample rate. This prevents the halfband filter from introducing interfering alias signals in the band of interest. Excellent passband dynamic range can be achieved when the bandwidth of interest is less than 1/4 the HB5 Halfband Filter output sample rate,

$$f_{HB5} = \frac{CIC\ OutputRate}{2^N}, \quad 0 < N < 5 \quad (EQ. 2)$$

because it ensures significant attenuation of the composite filter alias profile in the passband. Figure 5 illustrates such a filter design.

Use of the Interpolating Halfband Filters further down the processing chain can allow the FIR to run at reduced rate to maximize the number of taps available in the 255 tap FIR filter.

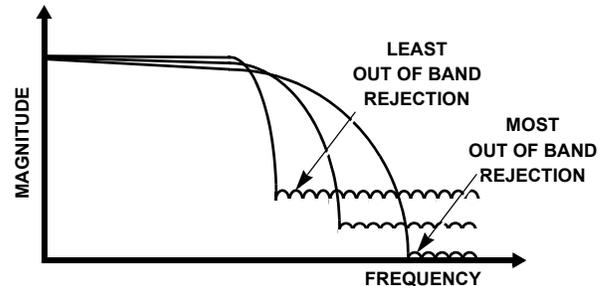


FIGURE 4A. FIXED NUMBER OF FILTER TAPS, VARIABLE OUT OF BAND REJECTION, VARIABLE TRANSITION BAND

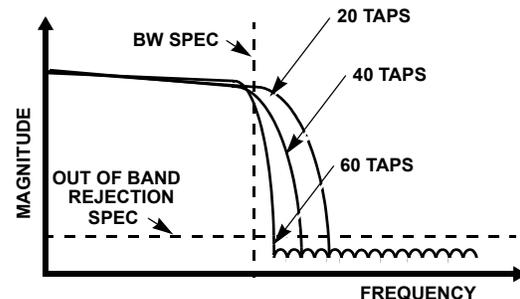


FIGURE 4B. FIXED OUT OF BAND REJECTION, VARIABLE NUMBER OF FILTER TAPS, VARIABLE TRANSITION BAND

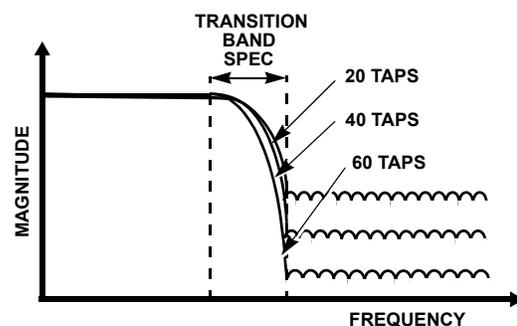


FIGURE 4C. FIXED TRANSITION BAND, VARIABLE OUT OF BAND REJECTION, VARIABLE NUMBER OF FILTER TAPS

FIGURE 4. FREQUENCY DOMAIN VIEW OF DESIGN TRADES

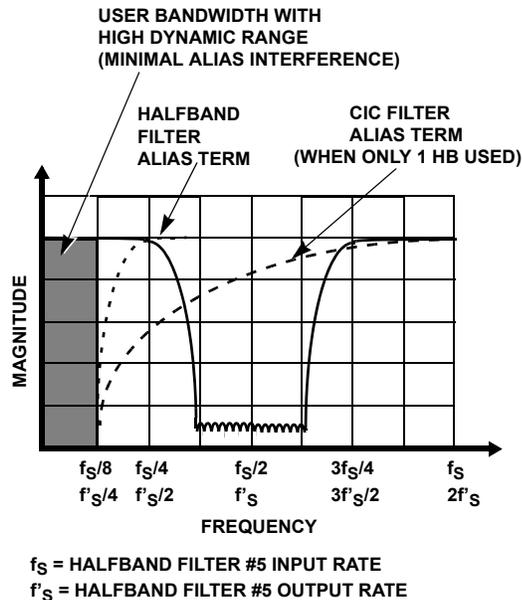


FIGURE 5. RULE OF THUMB DESIGN OF FIR PASSBAND

2. Resampler and Interpolation Considerations

The second filter block to be considered is the Polyphase Resampler FIR/ Interpolation Filters. While the 255 Tap FIR establishes the bandwidth of interest, the Polyphase Resampler/Interpolating Halfband filter is used to establish the output rate of the PDC. The output sample rate of the polyphase re-sampling filter is less than its input sample rate. The rate change is set by the ratio of the Resampler NCO frequency to the Resampler input sample rate. The range of the rate change is from 1/4 to ~1, of f_s , the Resampler filter input sample rate. This value is not required to be an integer! The 3dB passband of the polyphase Resampler filter is located at 0.375 the Resampler filter input sampling frequency. At 0.25 the Resampler input sampling frequency greater than 60dB alias attenuation is achieved. Use this filter to establish the non-integer rate changes from the input sampler to the output (user) sample rate. The Resampler NCO update rate is the input sample rate to the Resampler filter.

The Interpolation Halfbands offer the designer the ability to oversample the resampled polyphase filtered data by twice or four times the polyphase filter output rate. Thus, the rate change of this filter block can vary from 0.25 to 4. These halfband filters allow the 255 tap FIR filter to be run at a lower rate to obtain more filter taps and then interpolated to regain the time resolution. The output rate of this filter block is the sample rate of the coordinate converter, the discriminator, the discriminator FIR and the output block.

3. Halfband Filter Considerations

The third filter block to be considered is HalfBand filter block. The halfband filters are used to reduce the sampling rate and bandwidth of the input signal. This filter block allows the user to set an even multiple of 2 rate reduction and bandwidth reduction. Rate changes from 1 to 1/32 are possible with

bandwidth reductions of up to 1/32 using this filter block. The halfband filters have a flatter passband and a wider "alias free" output bandwidth than the CIC filter.

Use of this block requires an understanding of the alias profile to ensure that the desired dynamic range is achieved prior to entering the 255 tap FIR filter. Recall that the FIR filter bandwidth was set to 1/8 of its input frequency to avoid the alias images of the last halfband filter, which fall at 1/4 of the FIR input sample rate. The effect of the alias on full dynamic range is illustrated in Figure 6, which compares the full dynamic range bandwidth of the first and last stage of the Halfband filter block. By establishing a dynamic range specification, the bandwidth can be selected from any combination of the halfband filters, although the filters are typically enabled from stage 5 down to stage 1, as increasing number of stages are required.

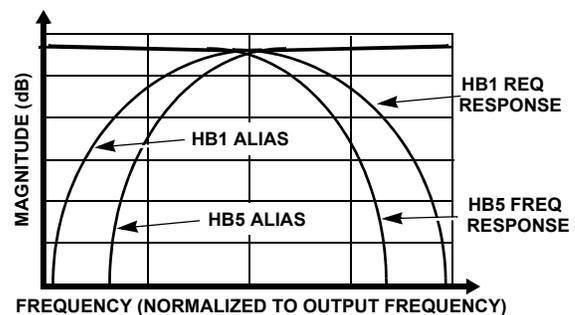


FIGURE 6A.

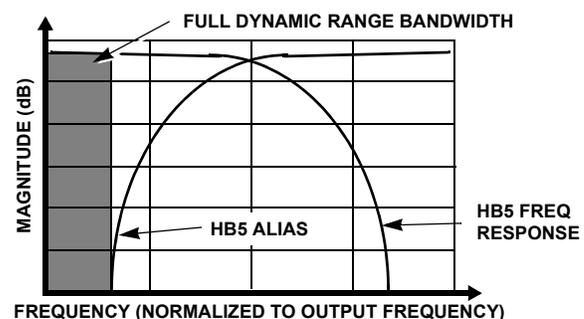


FIGURE 6B.

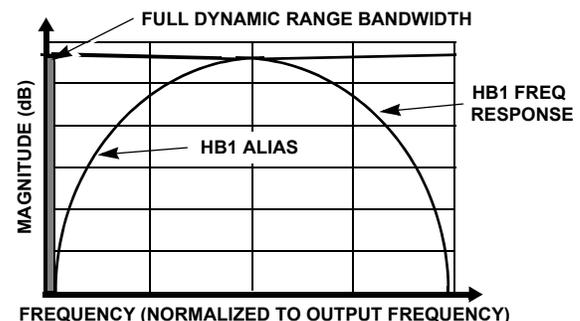


FIGURE 6C.

FIGURE 6. HALFBAND FULL DYNAMIC RANGE BANDWIDTHS

4. CIC Filter Considerations [2]

The final filter stage to be considered is the CIC filter. The CIC filter is the only filter stage that is running at the CLKIN rate (when CLKIN > PROCCLK). This filter provides the rate reduction necessary to meet the back end processing rate, PROCCLK. This allows for maximum sampling speed into the part. The CIC filter does rate reduction and out of band signal filtering. The CIC filter response has a main lobe extending to f_s/R , where R is the decimation rate of the filter and ranges from 4 to 32. These two constraints can be opposing.

5. Filter Implementation Trades

With the initial pass of the PDC internal filter configuration process complete, the next step is to optimize the filters. Begin by verifying that all of the filter sample rates match at the interfaces. Setting CLKIN high yields wider user bandwidth and reduces the requirements on the analog anti-aliasing filter. Setting PROCCLK high yields filters with more taps for a given filter input sample rate. These two constraints can be opposing.

For example, if f_{SAMP} , the FIR input sample rate, is set to a few frequencies in GSM (multiples of the baud rate). The FIR output sample rate must be a submultiple to find acceptable FIR input sample rates and make sure it can be implemented. Then check the alias of the halfband ($BW < 1/4 f_{SAMPLE}$ FIR).

Remember that the CLKIN rate limit is 52MHz [65MHz for A/B], while the PROCCLK is 35MHz [55MHz for A/B]. This means that the CLKIN input sample rate must be decimated by at least 2 to make the interface compatible. PROCCLK must always be greater than or equal to the CIC filter output rate discussed in the Polyphase Re-Sampling filter section.

After configuring the filters, the next step is to confirm that the dynamic range is acceptable. Finally, check the FIR filter taps available and ensure that the out of band attenuation and transition band filter performance are acceptable. The final check is verify that the output rate is sufficient for the application.

Detailed Filter Block Descriptions

Fifth Order CIC Filter

This filter has a minimum decimation rate of $R = 4$ and a maximum decimation rate of $R = 32$ (Note 1). The minimum rate of 4 is set by the hardware multiplex and throughput delays. This section is clocked at CLKIN rate, defining the maximum input rate as 52MSPS for the HSP50214 and 65MHz for the HSP50214A and B. Tables 7 and 7A detail the maximum output rates for all CIC filter decimation factors.

The CIC delay is calculated as follows:

$$\text{CIC Delay} = 5\text{CLKIN} + \frac{6\text{CLKIN}}{R}$$

$$\text{CIC Delay} = \left[5 + \frac{6}{R} \right] (\text{CLKIN Period})$$

The 5CLKIN cycles is for the integrator and the 6CLKIN/R cycles is for the COMB filter.

**TABLE 7. CIC FILTER OUTPUT RATE vs DECIMATION
RATE FOR HSP50214**

CIC MODE	(NOTE 1) DECIMATION RATE (R)	(NOTE 2) MAXIMUM FILTER OUTPUT RATE (MSPS)	COMMENTS
Bypass	-	52	No Decimation
CIC	4	52/4 = 13.0	Minimum Decimation is 4
CIC	5	52/5 = 10.4	
CIC	6	52/6 = 8.67	
CIC	7	52/7 = 7.43	
CIC	8	52/8 = 6.50	
CIC	9	52/9 = 5.78	
CIC	10	52/10 = 5.20	
CIC	11	52/11 = 4.73	
CIC	12	52/12 = 4.33	
CIC	13	52/13 = 4.00	
CIC	14	52/14 = 3.71	
CIC	15	52/15 = 3.47	
CIC	16	52/16 = 3.25	
CIC	17	52/17 = 3.06	
CIC	18	52/18 = 2.89	
CIC	19	52/19 = 2.74	
CIC	20	52/20 = 2.60	
CIC	21	52/21 = 2.48	
CIC	22	52/22 = 2.36	
CIC	23	52/23 = 2.26	
CIC	24	52/24 = 2.17	
CIC	25	52/25 = 2.08	
CIC	26	52/26 = 2.00	
CIC	27	52/27 = 1.93	
CIC	28	52/28 = 1.86	
CIC	29	52/29 = 1.79	
CIC	30	52/30 = 1.73	
CIC	31	52/31 = 1.68	
CIC	32	52/32 = 1.63	Maximum Decimation is 32

NOTES:

1. It is possible to achieve a decimation of 64 using a 10-bit converter shifted to the bottom of the input bits, a non-standard configuration.
2. The maximum rate may be limited in subsequent blocks.

**TABLE 7A. CIC FILTER OUTPUT RATE vs DECIMATION
RATE FOR HSP50214A AND B**

CIC MODE	(NOTE 3) DECIMATION RATE (R)	(NOTE 4) MAXIMUM FILTER OUTPUT RATE (MSPS)	COMMENTS
Bypass	-	65	No Decimation
CIC	4	65/4 = 16.25	Minimum Decimation is 4
CIC	5	65/5 = 13.00	
CIC	6	65/6 = 10.83	
CIC	7	65/7 = 9.29	
CIC	8	65/8 = 8.13	
CIC	9	65/9 = 7.22	
CIC	10	65/10 = 6.50	
CIC	11	65/11 = 5.91	
CIC	12	65/12 = 5.42	
CIC	13	65/13 = 5.00	
CIC	14	65/14 = 4.64	
CIC	15	65/15 = 4.33	
CIC	16	65/16 = 4.06	
CIC	17	65/17 = 3.82	
CIC	18	65/18 = 3.61	
CIC	19	65/19 = 3.42	
CIC	20	65/20 = 3.25	
CIC	21	65/21 = 3.10	
CIC	22	65/22 = 2.95	
CIC	23	65/23 = 2.83	
CIC	24	65/24 = 2.71	
CIC	25	65/25 = 2.60	
CIC	26	65/26 = 2.50	
CIC	27	65/27 = 2.41	
CIC	28	65/28 = 2.32	
CIC	29	65/29 = 2.24	
CIC	30	65/30 = 2.17	
CIC	31	65/31 = 2.10	
CIC	32	65/32 = 2.03	Maximum Decimation is 32

NOTES:

3. It is possible to achieve a decimation of 64 using a 10-bit converter shifted to the bottom of the input bits, a non-standard configuration.
4. The maximum rate may be limited in subsequent blocks.

Decimating Halfband Filters

The decimating halfband filters are clocked by the PROCCLK, which makes the maximum input rate for this filter section equal to 35MHz. It is important that this section must be able to support the output rate of the CIC section for proper operation. Five selectable decimating halfband filters in this block have progressively narrower alias free transition bandwidths, ranging from 0.5 to 0.125 times the input sample rate. The 6dB bandwidth of all five filters is 0.250 times the input sample rate. Each halfband section will decimate by two, (i.e., the output rate will be half the input rate). Note that the filter sections may be enabled in any combination. Filters should be selected based on the required transition band steepness and acceptable clock rate. The equation used in Tables 8 and 8A, to calculate the ratio of the PROCCLK to Sample Rate is:

$$f_{PROCCLK}/f_S \geq [(7)(HB5)(2^{HB5}) + (6)(HB4)(2^{(HB4 + HB5)}) + (5)(HB3)(2^{(HB3 + HB4 + HB5)}) + (4)(HB2)(2^{(HB2 + HB3 + HB4 + HB5)}) + (3)(HB1)(2^{(HB1 + HB2 + HB3 + HB4 + HB5)})]/2^T \quad (EQ. 3)$$

where

HB1 = 1 if HB1 is selected and 0 if it is bypassed;

HB2 = 1 if HB2 is selected and 0 if it is bypassed

HB3 = 1 if HB3 is selected and 0 if it is bypassed

HB4 = 1 if HB4 is selected and 0 if it is bypassed

HB5 = 1 if HB5 is selected and 0 if it is bypassed

T = number of Halfband Filters. The range for T is (0-5).

TABLE 8. DECIMATING HALFBAND MAXIMUM OUTPUT RATES vs CONFIGURATION

HALFBAND FILTER SECTION NUMBER					OVERCLOCK RATE FACTOR	MAXIMUM INPUT SAMPLE RATE (MHz)	MODE	MAXIMUM OUTPUT RATE (MHz)
5	4	3	2	1	(F _{PR} /f _S)	F _{PR} = 35MHz	Activated Halfband Filter	F _{PR} = 35MHz
0	0	0	0	0	1.00	35.00	Bypass - None	35.00
1	0	0	0	0	7.00	5.000	HB5	2.500
0	1	0	0	0	6.00	5.853	HB4	2.917
1	1	0	0	0	9.50	3.684	HB5 and HB4	0.921
0	0	1	0	0	5.00	7.000	HB3	3.500
1	0	1	0	0	8.50	4.4118	HB5 and HB3	1.029
0	1	1	0	0	8.00	4.375	HB4 and HB3	1.084
1	1	1	0	0	9.75	3.590	HB5, HB4 and HB3	0.449
0	0	0	1	0	4.00	8.750	HB2	4.375
1	0	0	1	0	7.50	4.667	HB5 and HB2	1.167
0	1	0	1	0	7.00	5.000	HB4 and HB2	1.250
1	1	0	1	0	8.75	4.000	HB5, HB4 and HB2	0.500
0	0	1	1	0	6.50	5.385	HB3 and HB2	1.346
1	0	1	1	0	8.25	4.242	HB5, HB3 and HB2	0.530
0	1	1	1	0	8.00	4.375	HB2, HB3 and HB4	0.547
1	1	1	1	0	8.88	3.944	HB5, HB4, HB3 and HB2	0.247
0	0	0	0	1	3.00	11.667	HB1	5.833
1	0	0	0	1	6.50	5.385	HB5 and HB1	1.346
0	1	0	0	1	6.00	5.833	HB4 and HB1	1.458
1	1	0	0	1	7.75	4.516	HB5, HB4 and HB1	0.565
0	0	1	0	1	5.50	6.364	HB3 and HB1	1.591
1	0	1	0	1	7.25	4.828	HB5, HB3 and HB1	0.603
0	1	1	0	1	7.00	5.000	HB4, HB3 and HB1	0.625
1	1	1	0	1	7.88	4.444	HB5, HB4, HB3 and HB1	0.278
0	0	0	1	1	5.00	7.000	HB2 and HB1	1.750
1	0	0	1	1	6.75	5.185	HB5, HB2 and HB1	0.648
0	1	0	1	1	6.50	5.385	HB4, HB2 and HB1	0.673
1	1	0	1	1	7.38	4.746	HB5, HB4, HB2 and HB1	0.297
0	0	1	1	1	6.25	5.600	HB3, HB2 and HB1	0.700
1	0	1	1	1	7.13	4.912	HB4, HB3, HB2 and HB1	0.307
0	1	1	1	1	7.00	5.000	HB4, HB3, HB2 and HB1	0.313
1	1	1	1	1	7.44	4.706	HB5, HB4, HB3, HB2 and HB1	0.147

TABLE 8A. DECIMATING HALFBAND MAXIMUM OUTPUT RATES vs CONFIGURATION

HALFBAND FILTER SECTION NUMBER					OVERCLOCK RATE FACTOR	MAXIMUM INPUT SAMPLE RATE (MHz)	MODE	MAXIMUM OUTPUT RATE (MHz)
5	4	3	2	1	(F _{PR} /f _S)	F _{PR} = 55MHz	Activated Halfband Filter	F _{PR} = 55MHz
0	0	0	0	0	1.00	55.00	Bypass - None	55.00
1	0	0	0	0	7.00	7.857	HB5	3.929
0	1	0	0	0	6.00	9.167	HB4	4.583
1	1	0	0	0	9.50	5.789	HB5 and HB4	1.447
0	0	1	0	0	5.00	11.000	HB3	5.500
1	0	1	0	0	8.50	6.471	HB5 and HB3	1.618
0	1	1	0	0	8.00	6.875	HB4 and HB3	1.719
1	1	1	0	0	9.75	5.641	HB5, HB4 and HB3	0.705
0	0	0	1	0	4.00	13.750	HB2	6.875
1	0	0	1	0	7.50	7.333	HB5 and HB2	1.833
0	1	0	1	0	7.00	7.857	HB4 and HB2	1.964
1	1	0	1	0	8.88	6.197	HB5, HB4 and HB2	0.387
0	0	1	1	0	6.50	8.462	HB3 and HB2	2.115
1	0	1	1	0	8.25	6.667	HB5, HB3 and HB2	0.833
0	1	1	1	0	8.00	6.875	HB2, HB3 and HB4	0.859
1	1	1	1	0	8.88	6.197	HB5, HB4, HB3 and HB2	0.387
0	0	0	0	1	3.00	18.333	HB1	9.167
1	0	0	0	1	6.50	8.462	HB5 and HB1	2.115
0	1	0	0	1	6.00	9.167	HB4 and HB1	2.292
1	1	0	0	1	7.75	7.097	HB5, HB4 and HB1	0.887
0	0	1	0	1	5.50	10.000	HB3 and HB1	2.500
1	0	1	0	1	7.25	7.586	HB5, HB3 and HB1	0.948
0	1	1	0	1	7.00	7.857	HB4, HB3 and HB1	0.982
1	1	1	0	1	7.88	6.984	HB5, HB4, HB3 and HB1	0.437
0	0	0	1	1	5.00	11.000	HB2 and HB1	2.750
1	0	0	1	1	6.75	8.148	HB5, HB2 and HB1	1.019
0	1	0	1	1	6.50	8.462	HB4, HB2 and HB1	1.058
1	1	0	1	1	7.38	7.458	HB5, HB4, HB2 and HB1	0.466
0	0	1	1	1	6.25	8.800	HB3, HB2 and HB1	1.100
1	0	1	1	1	7.13	7.719	HB4, HB3, HB2 and HB1	0.482
0	1	1	1	1	7.00	7.857	HB4, HB3, HB2 and HB1	0.491
1	1	1	1	1	7.44	7.395	HB5, HB4, HB3, HB2 and HB1	0.231

255 TAP FIR Filter

The 255 TAP FIR filter has a minimum decimation factor of $R = 1$. The maximum decimation factor in this filter is $R = 16$. The filter can be “effectively” bypassed by setting $C_0 = 1$ and $C_N = 0$. This requires three clock cycles. The filter is clocked by PROCCLK, so the maximum input rate is 35MHz for the HSP50214 and 55MHz for the HSP50214A and B. One clock is used to write data into the ROM.

1. Determining the Number of FIR Filter Taps

For the generic filter configuration, use Equation 4 to calculate the number of taps available at a given input sample rate. We can use Equation 5 to calculate the maximum input rate, and Equation 6 to calculate the maximum output rate.

$$\text{Taps} = \text{floor}[\text{PROCCLK}/(f_{\text{SAMP}}/R) - R] \bullet (1 + \text{SYM}) - (\text{SYM} \bullet \text{ODD}) \text{ for real filters} \quad (\text{EQ. 4A})$$

$$\text{Taps} = \text{floor}[(\text{PROCCLK}/f_{\text{SAMP}}/R) - R]/2 \text{ for complex filters} \quad (\text{EQ. 4B})$$

where floor is defined as the integer portion of a number; PROCCLK is the compute clock; f_{SAMP} = the FIR input sample rate; R = Decimation Rate; $\text{SYM} = 1$ for symmetrical filter, 0 for asymmetrical filter; $\text{ODD} = 1$ for an odd number of filter taps, 0 = an even number of taps.

PDC FIR Filter Number of Taps Calculation

Table 9 details the formula for four common filter types. Tables 10 and 11 detail the rates at which a “maximum number of taps” filter can run, for minimum and maximum FIR decimation factors.

TABLE 9.

FILTER TYPE	EQUATION FOR NUMBER OF FILTER TAPS
Real, Symmetric, Even # Taps	$[\text{PROCCLKS}/f_{\text{SAMP}}/R) - R]^*2$
Real, Symmetric, Odd # Taps	$\{[\text{PROCCLKS}/f_{\text{SAMP}}/R) - R] - 1\}^*2$
Real, Asymmetric	$[\text{PROCCLKS}/(f_{\text{SAMP}}/R) - R]$
Complex	$[\text{PROCCLKS}/f_{\text{SAMP}}/R) - R]/2$

Where:

PROCCLK is the PDC backend compute clock,

f_{SAMP} is the FIR input sample clock,

R is the FIR decimation factor.

$\text{PROCCLKS}/(f_{\text{SAMP}}/R)$ is the number of clocks required to generate a FIR output.

TABLE 10. EXAMPLE FOR PROCCLK = 55MHz, $f_{\text{SAMP}} = 5\text{MHz}$; $R = 16$

FILTER TYPE	EQUATION FOR NUMBER OF FILTER TAPS
Real, Symmetric, Even # of Taps	$[\text{PROCCLK}/(f_{\text{SAMP}}/R) - R]^*2$ $[55 \times 10^6 / (6.154 \times 10^6 / 16) - 16]^*2 = 254$
Real, Symmetric, Odd # of Taps	$\{[\text{PROCCLK}/(f_{\text{SAMP}}/R) - R] - 1\}^*2$ $\{[55 \times 10^6 / (6.154 \times 10^6 / 16) - 16] - 1\}^*2 = 252$
Real, Asymmetric	$[\text{PROCCLK}/(f_{\text{SAMP}}/R) - R]$ $[55 \times 10^6 / (6.154 \times 10^6 / 16) - 16] = 127$
Complex	$[\text{PROCCLK}/(f_{\text{SAMP}}/R) - R]/2$ $[55 \times 10^6 / (6.154 \times 10^6 / 16) - 16]/2 = 63$

TABLE 11. EXAMPLE FOR PROCCLK = 55MHz; $f_{\text{SAMP}} = 0.430\text{MHz}$; $R = 1$

FILTER TYPE	EQUATION FOR NUMBER OF FILTER TAPS
Real, Symmetric, Even # Taps	$[\text{PROCCLKS}/f_{\text{SAMP}}/R) - R]^*2$ $[55 \times 10^6 / (0.430 \times 10^6 / 1) - 1]^*2 = 254$
Real, Symmetric, Odd # Taps	$\{[\text{PROCCLKS}/f_{\text{SAMP}}/R) - R] - 1\}^*2$ $\{[55 \times 10^6 / (0.430 \times 10^6 / 1) - 1] - 1\}^*2 = 252$
Real, Symmetric	$[\text{PROCCLKS}/f_{\text{SAMP}}/R) - R]$ $[55 \times 10^6 / (0.430 \times 10^6 / 1) - 1] = 127$
Complex	$[\text{PROCCLKS}/(f_{\text{SAMP}}/R) - R]/2$ $[55 \times 10^6 / (0.430 \times 10^6 / 1) - 1]/2 = 63$

Example FIR Filter “Number of Taps” Calculation

As an example, for a 35MHz compute clock, a 5MHz input sample rate, decimation by 2, even symmetry, and an odd number of taps, the number of taps is:

$$\text{Taps} = \text{floor}[35\text{MHz}/(5\text{MHz}/2) - 2] \bullet (1 + 1) - (1 \bullet 1) = \text{floor}[14 - 2] \bullet 2 - 1 = 12 \bullet 2 - 1 = 23 \text{ for a real filter and}$$

$$\text{Taps} = \text{floor}[(35\text{MHz}/(5\text{MHz}/2) - 2)/2] = \text{floor}[(14 - 2)/2] = 6 \text{ for a complex filter}$$

2. Calculating the Maximum Input Sample Rate

We can rearrange Equations 4 and 4A to yield the maximum input sample rate.

$$f_{\text{SAMP}} = \text{PROCCLK} \bullet (R) / [R + [(Taps) + (\text{SYM} \bullet \text{ODD})] / (1 + \text{SYM})] \text{ for real filters} \quad (\text{EQ. 5A})$$

$$f_{\text{SAMP}} = \text{PROCCLK} \bullet R / [R + [(Taps) \bullet 2]] \text{ for complex filters} \quad (\text{EQ. 5B})$$

where PROCCLK is the compute clock; f_{SAMP} = the FIR input sample rate; R = Decimation Rate; $\text{SYM} = 1$ for symmetrical filter, 0 for asymmetrical filter; $\text{ODD} = 1$ for an odd number of filter taps, 0 = an even number of taps.

Example Maximum Input Rate Calculation

Let's use the example provided above to see if we can predict the 5MHz input rate.

$$f_{\text{SAMP}} = 35\text{MHz} \cdot (2) / [2 + ((23) + (1)) / (2)] = 5.00\text{MHz}, \text{ which is correct.}$$

3. Calculating the Maximum Output Rate

The equation for the maximum output sample rate becomes:

$$f_{\text{FIROUT}} = (f_{\text{SAMP}}) / R \quad (\text{EQ. 6})$$

for both real and complex filters.

An Example Maximum Output Rate Calculation

As an example, for a compute clock of 35MHz and a real, symmetrical filter, no decimation, all 255 taps can be used for output sample rates of 272.37kHz. If that same filter decimates by 16, then the output sample rate becomes $272.37/16 = 17.023\text{kHz}$.

Table 12 and 12A provides a sampling of the filter output rate calculations. The maximum output rate as a function of a real symmetric 127 tap filter configuration with varying decimation rates is given. Use of Equations 4, 5 and 6 provide the details necessary to calculate an application specific filter configuration. Remember that prior to obtaining a part level operational configuration, the input rate of the 255 tap FIR Filter section must match the output rate of the Halfband filter section.

Figures 7 and 8 provide a plot of Input Rate and Output Rate as a function of Decimation Rate for a set of odd number of tap, symmetric filters (15, 31, 63, 127, 191 and 255). They will help in estimating input and output rates if the filter is known.

Another approach is to determine the number of filter taps that can be implemented at a specific input rate. Figures 9 through 12A are plots of the number of filter taps based on the input rate. Each figure represents a different decimation rate ($R = 1, 2, 4, 8, \text{ and } 16$). These plots will help determine the extent of shaping that can be done with the FIR filter for the specific input rate.

TABLE 12. MAXIMUM OUTPUT RATE vs FIR FILTER CONFIGURATION

MODE	DECIMATION (R)	REAL OR COMPLEX	SYMMETRIC OR ASYMMETRIC	NUMBER OF TAPS	MAXIMUM INPUT SAMPLE RATE (MHz)	MAXIMUM OUTPUT RATE (MHz)
Bypass	1	Real	-	1	5.83 (Notes 5, 6)	5.83 (Notes 5, 6)
Filter	2	Real	Symmetric	127	1.060606	0.530303
Filter	3	Real	Symmetric	127	1.567164	0.522388
Filter	4	Real	Symmetric	127	2.058824	0.514706
Filter	5	Real	Symmetric	127	2.536232	0.507246
Filter	6	Real	Symmetric	127	3.000000	0.500000
Filter	7	Real	Symmetric	127	3.450704	0.492958
Filter	8	Real	Symmetric	127	3.888889	0.486111
Filter	9	Real	Symmetric	127	4.315068	0.479452
Filter	10	Real	Symmetric	127	4.729730	0.472973
Filter	11	Real	Symmetric	127	5.133333	0.466667
Filter	12	Real	Symmetric	127	5.526316	0.460526
Filter	13	Real	Symmetric	127	5.909091	0.454545
Filter	14	Real	Symmetric	127	6.282051	0.448718
Filter	15	Real	Symmetric	127	6.645570	0.443038
Filter	16	Real	Symmetric	127	7.000000	0.4375 (Note 6)

NOTES:

- Assumes a 35MHz PROCCLK.
- Since 6 CLKs are required by AGC logic, max CLK = $35\text{MHz}/6 = 5.83\text{MHz}$, which is lower than the rate calculated for a FIR bypass ($35\text{MHz}/3 = 11.67$).

TABLE 12A. MAXIMUM OUTPUT RATE vs FIR FILTER CONFIGURATION

MODE	DECIMATION (R)	REAL OR COMPLEX	SYMMETRIC OR ASYMMETRIC	NUMBER OF TAPS	MAXIMUM INPUT SAMPLE RATE (MHz)	MAXIMUM OUTPUT RATE (MHz)
Bypass	1	Real	-	1	9.17 (Notes 7, 8)	9.17 (Notes 7, 8)
Filter	2	Real	Symmetric	127	1.667	0.833
Filter	3	Real	Symmetric	127	2.463	0.821
Filter	4	Real	Symmetric	127	3.235	0.809
Filter	5	Real	Symmetric	127	3.986	0.797
Filter	6	Real	Symmetric	127	4.714	0.786
Filter	7	Real	Symmetric	127	5.423	0.775
Filter	8	Real	Symmetric	127	6.111	0.764
Filter	9	Real	Symmetric	127	6.781	0.753
Filter	10	Real	Symmetric	127	7.432	0.743
Filter	11	Real	Symmetric	127	8.067	0.733
Filter	12	Real	Symmetric	127	8.684	0.724
Filter	13	Real	Symmetric	127	9.286	0.714
Filter	14	Real	Symmetric	127	9.872	0.705
Filter	15	Real	Symmetric	127	10.433	0.696
Filter	16	Real	Symmetric	127	11.000	0.688 (Note 8)

NOTES:

- Assumes a 55MHz PROCCLK.
- Since 6 CLKS are required by AGC logic, max CLK = 55MHz/6 = 9.17MHz, which is lower than the rate calculated for a FIR bypass (55/3 = 18.33MHz).

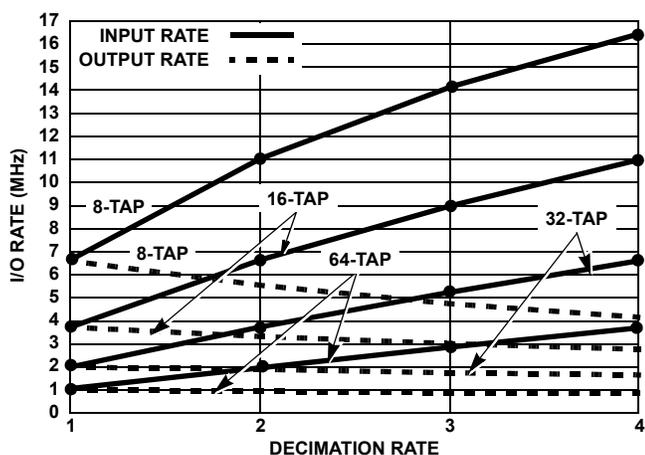


FIGURE 7. DETERMINING MAXIMUM INPUT AND OUTPUT RATES BASED ON FILTER DECIMATION FOR A 8, 16, 32 AND 64 TAP FILTER ($f_s = 33\text{MHz}$, SYM = 1, EVEN/ODD = 0)

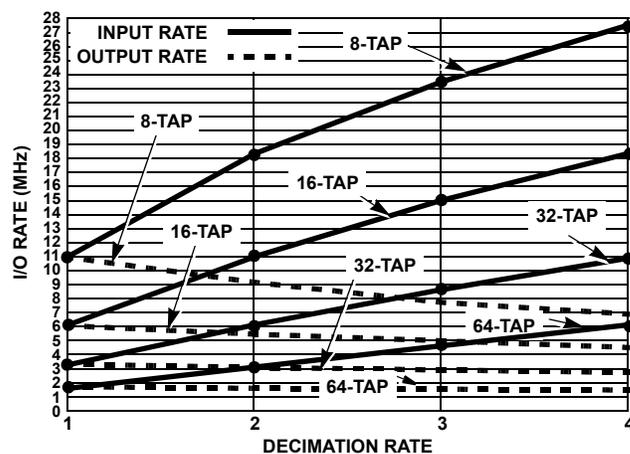


FIGURE 7A. DETERMINING MAXIMUM INPUT AND OUTPUT RATES BASED ON FILTER DECIMATION FOR A 8, 16, 32 AND 64 TAP FILTER ($f_s = 55\text{MHz}$, SYM = 1, EVEN/ODD = 0)

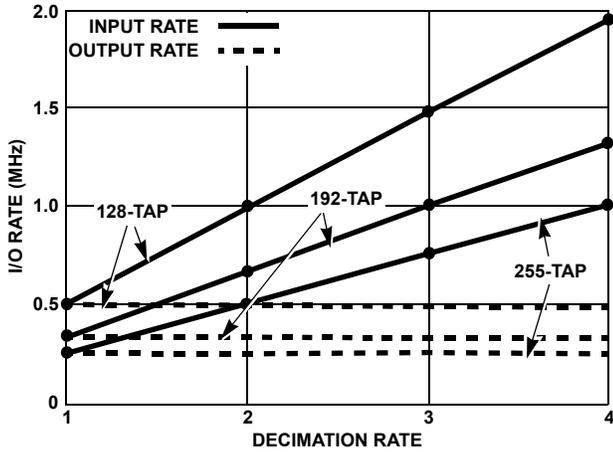


FIGURE 8. DETERMINING MAXIMUM INPUT AND OUTPUT RATES, BASED ON FILTER DECIMATION FOR A 127, 192 AND 255 TAP FILTER ($f_s = 33\text{MHz}$, $\text{SYM} = 1$, $\text{EVEN/ODD} = 0$)

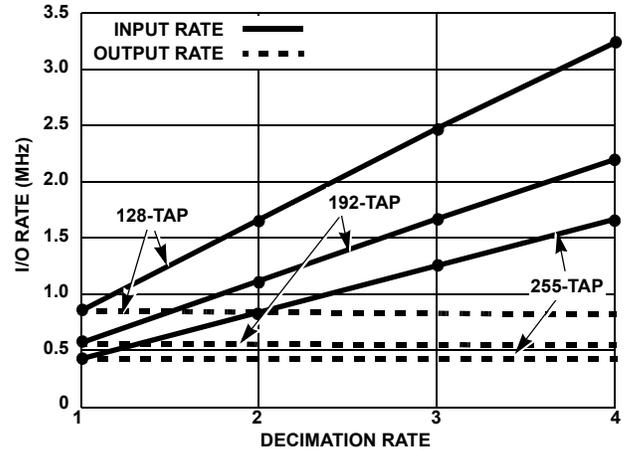


FIGURE 8A. DETERMINING MAXIMUM INPUT AND OUTPUT RATES, BASED ON FILTER DECIMATION FOR A 127, 192 AND 255 TAP FILTER ($f_s = 55\text{MHz}$, $\text{SYM} = 1$, $\text{EVEN/ODD} = 0$)

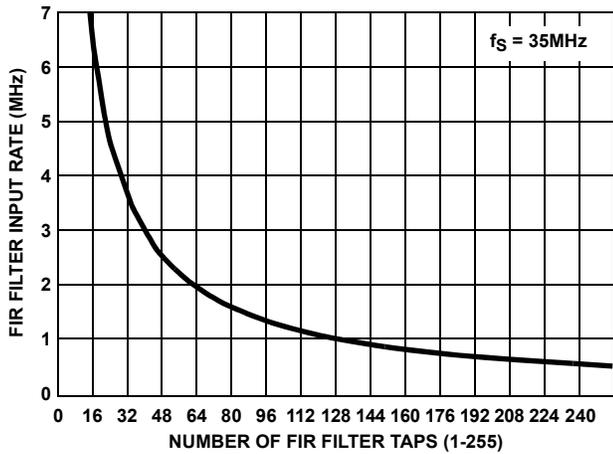


FIGURE 9. THE NUMBER OF FILTER TAPS vs INPUT RATE FOR A DECIMATION OF 2, $\text{SYM} = 1$, $\text{EVEN/ODD} = 0$

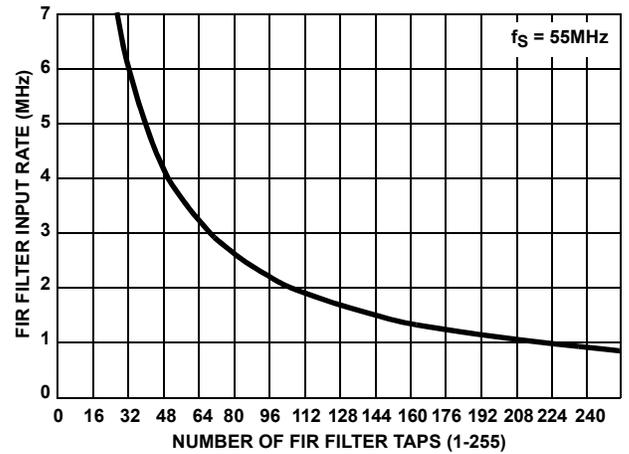


FIGURE 9A. THE NUMBER OF FILTER TAPS vs INPUT RATE FOR A DECIMATION OF 2, $\text{SYM} = 1$, $\text{EVEN/ODD} = 0$

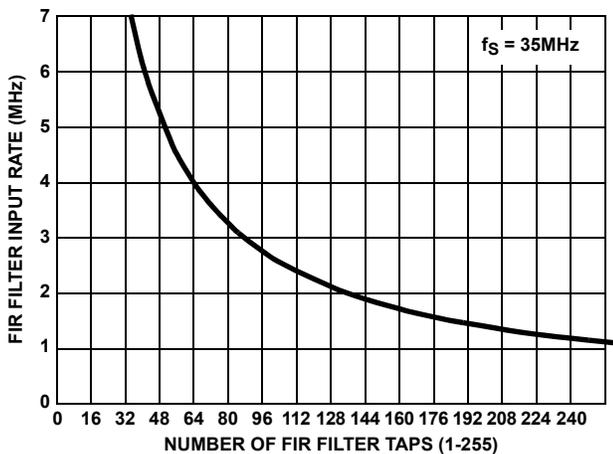


FIGURE 10. THE NUMBER OF FILTER TAPS vs INPUT RATE FOR A DECIMATION OF 4, $\text{SYM} = 1$, $\text{EVEN/ODD} = 0$

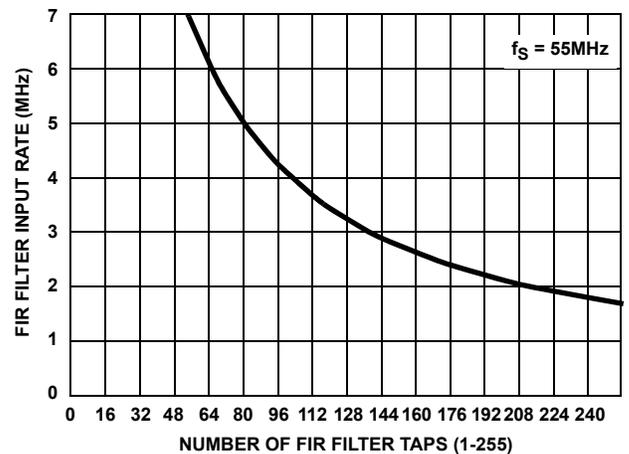


FIGURE 10A. THE NUMBER OF FILTER TAPS vs INPUT RATE FOR A DECIMATION OF 4, $\text{SYM} = 1$, $\text{EVEN/ODD} = 0$

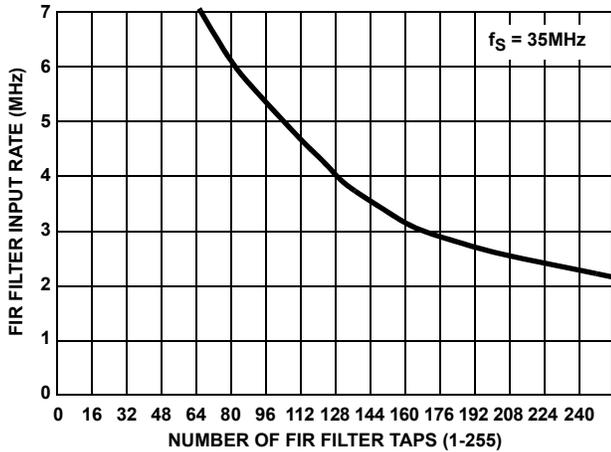


FIGURE 11. THE NUMBER OF FILTER TAPS vs INPUT RATE FOR A DECIMATION OF 8, SYM = 1, EVEN/ODD = 0

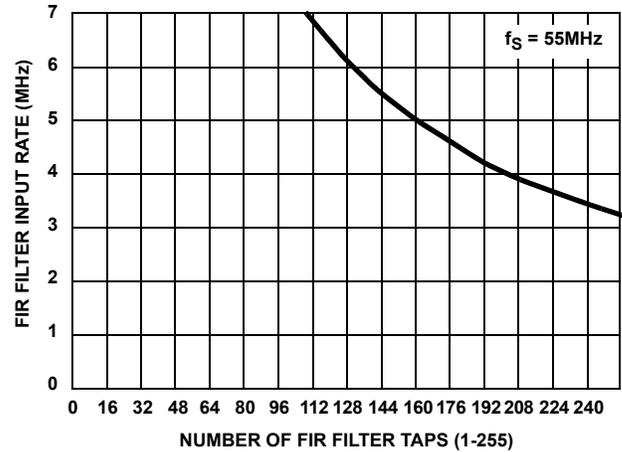


FIGURE 11A. THE NUMBER OF FILTER TAPS vs INPUT RATE FOR A DECIMATION OF 8, SYM = 1, EVEN/ODD = 0

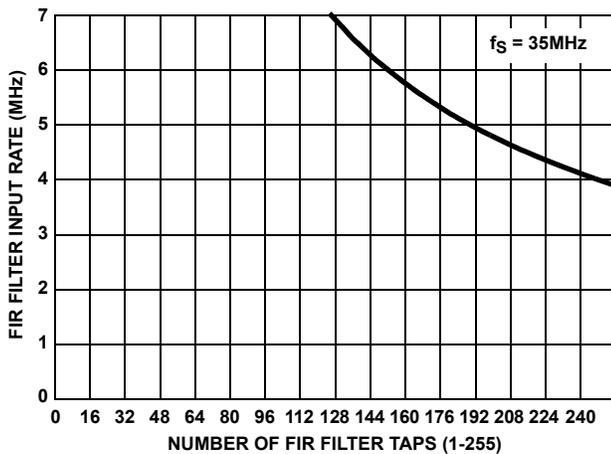


FIGURE 12. THE NUMBER OF FILTER TAPS vs INPUT RATE FOR A DECIMATION OF 16

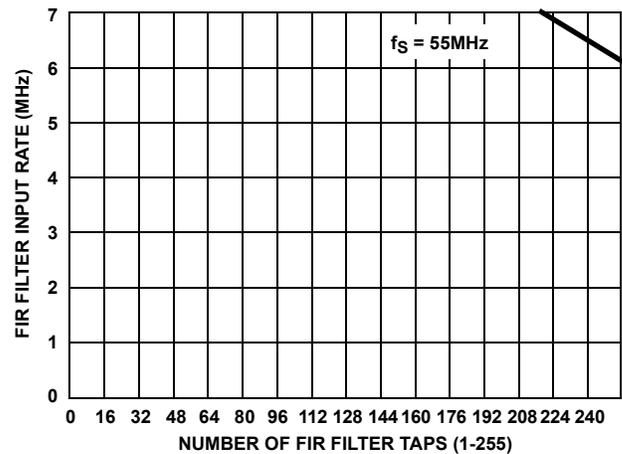


FIGURE 12A. THE NUMBER OF FILTER TAPS vs INPUT RATE FOR A DECIMATION OF 16

AGC Multipliers

The data multiplication by the AGC involves multiplexing and delay circuitry resulting an output to input clock ratio of 6. Since the circuitry is clocked by PROCCLK, the maximum input rate is 35MHz, yielding a maximum output rate of 35/6 = 5.833MHz. Tables 13 and 13A detail this rate transfer.

TABLE 13. MAXIMUM INPUT AND OUTPUT RATES OF THE AGC MULTIPLIERS

MAX INPUT RATE (MHz)	MAX OUTPUT RATE (MHz)
35.00	5.833

TABLE 13A. MAXIMUM INPUT AND OUTPUT RATES OF THE AGC MULTIPLIERS

MAX INPUT RATE (MHz)	MAX OUTPUT RATE (MHz)
55.00	9.167

Polyphase Filters and Interpolating Halfband Filters

The polyphase (Resampler) filter and interpolating halfband filters will be considered a block. The polyphase filter is clocked by PROCCLK and enabled by the Resampler NCO, which is set via processor control. Equation 7 details the calculation of the Resampler NCO Carry Output frequency.

The output sample rate is determined by the Resample NCO.

$$f_{CO} = f_S \times (TCF + TOF) / 2^{32} \quad (\text{EQ. 7})$$

where f_{CO} =; f_S = Resampler NCO Clock Frequency (FIR output rate); TCF = Timing Center Frequency; and TOF = Timing Offset Frequency. TCF is processor programmed and TOF is input via the serial interface. Both TCF and TOF are 32-bit word values ($0 < x < 4,294,967,295$). The maximum output rate is 0.999... X input rate.

The halfband filters are clocked by PROCCLK.

Emptying the filters requires a certain number of PROCCLKs, depending on which filters are enabled. The number of cycles, as well as the maximum I/O rates, are shown in Table 14.

**TABLE 14. POLYPHASE FILTER AND INTERPOLATING
HALFBAND FILTER MAX OUTPUT RATES**

MODE	CLOCK CYCLES	INPUT RATE (MHz)	INTERPOLATION RATE	MAX OUTPUT RATE (MHz)
Bypass	0	35.000	-	35.000
Polyphase Filter	6	$35/6 = 5.833$	-	NCO (5.833)
Polyphase and 1 Halfband Filter	13	$35/13 = 2.692$	2	NCO (5.385)
Polyphase and 2 Halfband Filters	23	$35/23 = 1.522$	4	NCO (6.087)
1 Halfband Filter	7	$35/7 = 5.00$	2	10.000
2 Halfband Filters	17	$35/17 = 2.059$	4	8.235

**TABLE 14A. POLYPHASE FILTER AND INTERPOLATING
HALFBAND FILTER MAX OUTPUT RATES**

MODE	CLOCK CYCLES	INPUT RATE (MHz)	INTERPOLATION RATE	MAX OUTPUT RATE (MHz)
Bypass	0	55.000	-	55.000
Polyphase Filter	6	$55/6 = 9.17$	-	9.17
Polyphase and 1 Halfband Filter	13	$55/13 = 4.23$	2	8.46
Polyphase and 2 Halfband Filters	23	$55/23 = 2.39$	4	9.56
1 Halfband Filter	7	$55/7 = 7.86$	2	15.71
2 Halfband Filters	17	$55/17 = 3.24$	4	12.94

NOTE: This frequency is set by the Resampler NCO.

Cartesian to Polar Converter

The maximum output rate of the Cartesian to Polar Converter is a function of the precision desired in the answer. This circuitry is clocked by PROCCLK, so the maximum input rate is 35MHz for the HSP50214 and 55MHz for the HSP50214A and B. To obtain full accuracy of 16 bits, 17 clocks are required. The maximum output rate is $35/17 = 2.059\text{MHz}$; $55/17 = 3.235\text{MHz}$.

Tables 15 and 15A detail the output resolution based on the maximum output clock, assuming the input is sampled at 35MHz and 55MHz, respectively. Six bits may be sufficient for many applications. In general the resolution on the phase output will need to be greater than on the magnitude output.

**TABLE 15. BIT RESOLUTION AS A FUNCTION OF
INPUT/OUTPUT RATE INTO THE CONVERTER**

INPUT RATE (MHz)	OUTPUT RATE (MHz)	MAGNITUDE OUTPUT ERROR (%)	PHASE OUTPUT ACCURACY (DEGREES)
35	35.000	-	-
35	17.500	14.12	45
35	11.667	3.98	26.565
35	8.750	1.03	14.036
35	7.000	0.26	7.125
35	5.833	0.07	3.576
35	5.00	0.02	1.790
35	4.375	0.004	0.895
35	3.889	Less than 0.004	0.447
35	3.500	Less than 0.004	0.224
35	3.182	Less than 0.004	0.112
35	2.916	Less than 0.004	0.056
35	2.688	Less than 0.004	0.028
35	2.500	Less than 0.004	0.014
35	2.333	Less than 0.004	0.007
35	2.188	Less than 0.004	0.003

NOTE: This table assumes full scale input.

**TABLE 15A. BIT RESOLUTION AS A FUNCTION OF
INPUT/OUTPUT RATE INTO THE CONVERTER**

INPUT RATE (MHz)	OUTPUT RATE (MHz)	MAGNITUDE OUTPUT ERROR (%)	PHASE OUTPUT ACCURACY (DEGREES)
55	55.000	-	-
55	27.500	14.12	45
55	18.333	3.98	26.565
55	13.750	1.03	14.036
55	11.000	0.26	7.125
55	9.167	0.07	3.576
55	7.857	0.02	1.790
55	6.857	0.004	0.895
55	6.111	Less than 0.004	0.447
55	5.500	Less than 0.004	0.224
55	5.000	Less than 0.004	0.112
55	4.583	Less than 0.004	0.056
55	4.231	Less than 0.004	0.028
55	3.929	Less than 0.004	0.014
55	3.667	Less than 0.004	0.007
55	3.438	Less than 0.004	0.003

NOTE: This table assumes full scale input.

References

For Intersil documents available on the internet, see web site <http://www.intersil.com>.

- [1] *HSP50214 Data Sheet*, Intersil Corporation, FN4266.
- [2] Hogenauer, Eugene, "An Economical Class of Digital Filters for Decimation and Interpolation", IEEE Transactions on Acoustics, Speech and Signal Processing, Vol. ASSP-29 No. 2, April 1981.
- [3] FO-006.1 HSP50214 Block Diagram, Intersil Corporation

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