

What Is This Application Note Trying To Accomplish?

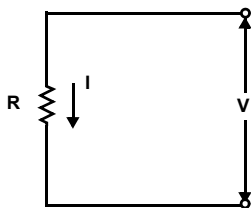
There is a long gap between engineering college and mid career in a non-engineering position, but technology marches on so a simple method of keeping abreast with the latest developments is required. This application note starts with an overview of the basic laws of physics, progresses through circuits 1 and 2, and explains op amp operation through the use of feedback principles. Math is the foundation of circuit design, but it is kept to the simplest level possible in this application note. For more advanced op amp topics please refer to the technical papers listed in references 1 and 2.

Basic Physics Laws, Circuit Theorems and Analysis

Good news and bad news. The bad news is that it takes a certain amount of dog work, like relearning physics and circuit theorems, before proficiency becomes second nature. The good news is that if you just hang in for a few pages you will experience the joy of analyzing circuits like an expert. You will gain ten years experience in a few hours. You will be able to write op amp equations like a design engineer. You might think this is a worthless effort, but imagine the look on the analog engineer's face, the one who thinks non-analog engineers are as dumb as a box of rocks, when you write your own op amp circuit equations.

Ohm's and Kirchoff's Laws

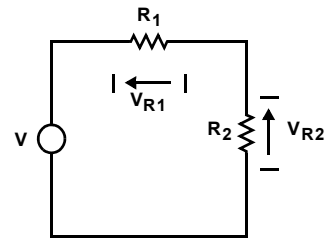
Ohm's law states that there is a relationship between the current in a circuit and the voltage potential across a circuit. This relationship is a function of a constant called the resistance.



$V = IR$ (EQ.1)

FIGURE 1. ILLUSTRATION OF OHM'S LAW

Kirchoff's voltage law states that the algebraic sum of the voltages around any closed loop equals zero. The sum includes independent voltage sources, dependent voltage sources and voltage drops across resistors (called IR drops).

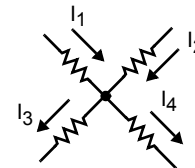


$V - V_{R1} - V_{R2} = 0$ or $V = V_{R1} + V_{R2}$ (EQ. 2)

Σ voltage sources = Σ voltage drops (EQ. 3)

FIGURE 2. ILLUSTRATION OF KIRCHOFF'S VOLTAGE LAW

Kirchoff's current law states that the algebraic sum of all the currents leaving a node equals zero. The sum includes independent current sources, dependent current sources, and component currents.



$I_1 + I_2 = I_3 + I_4$ (EQ. 4)

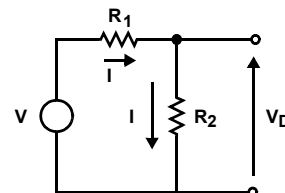
$I_1 + I_2 - I_3 - I_4 = 0$ (EQ. 5)

Σ currents into a junction = 0 (EQ. 6)

FIGURE 3. ILLUSTRATION OF KIRCHOFF'S CURRENT LAW

Voltage and Current Dividers

Voltage dividers are seen often in circuit design because they are useful for generating a reference voltage, for biasing active devices, and acting as feedback elements. Current dividers are seen less often, but they are still important so we will develop the equations for them. The voltage divider equations, which assume that the load does not draw any current, are developed in Figure 4.



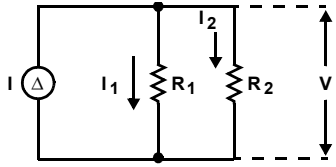
$V = IR_1 + IR_2 = I(R_1 + R_2)$ (EQ. 7)

$I = \frac{V}{(R_1 + R_2)}$ (EQ. 8)

$V_D = IR_2 = \frac{V}{(R_1 + R_2)}(R_2) = V \frac{R_2}{R_1 + R_2}$ (EQ. 9)

FIGURE 4. DERIVATION OF THE VOLTAGE DIVIDER RULE

The current divider equations, assuming that the only load is R_2 , is given in Figure 5.



$$I = I_1 + I_2 \quad (\text{EQ. 10})$$

$$V = I_1 R_1 = I_2 R_2 \quad (\text{EQ. 11})$$

$$I_1 = I_2 \frac{R_2}{R_1} \quad (\text{EQ. 12})$$

$$I = I_1 + I_2 = I_2 \frac{R_2}{R_1} + I_2 = I_2 \left(1 + \frac{R_2}{R_1} \right) = I_2 \left(\frac{R_1 + R_2}{R_1} \right) \quad (\text{EQ. 13})$$

$$\text{Then: } I_2 = I \frac{R_1}{R_1 + R_2} \quad (\text{EQ. 14})$$

FIGURE 5. DERIVATION OF THE CURRENT DIVIDER RULE

Thevenin's and Norton's Theorems

There are situations where it is simpler to concentrate on one component rather than write equations for the complete circuit. When the input source is a voltage source, Thevenin's theorem is used to isolate the component of interest, but if the input source is a current source, Norton's theorem is used to isolate the component of interest.

To apply Thevenin's theorem one must look back into the terminals of the component being replaced. Now calculate the open circuit voltage seen at these terminals, and during this calculation consider that there is no load current so the voltage divider rule can be used. Next short independent voltage sources and open independent current sources; now calculate the impedance seen looking into the terminals. The final step is to replace the original circuit with the Thevenin equivalent voltage, V_{th} , and Thevenin equivalent impedance, Z_{th} .

Thevenin's theorem is illustrated in Figure 6.

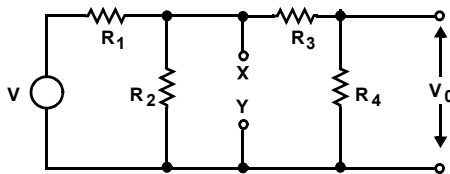


FIGURE 6. THE ORIGINAL CIRCUIT

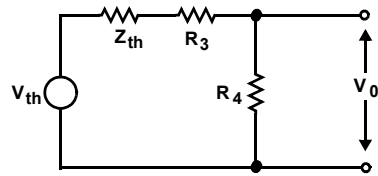
The open circuit voltage is calculated by looking into the terminals X - Y, and then calculating the open circuit voltage with the voltage divider rule.

$$V_{th} = V \frac{R_2}{R_1 + R_2} \quad (\text{EQ. 15})$$

The impedance looking back into the terminals X - Y with the independent source, V, shorted is given below.

$$Z_{th} = Z_{x-y} = \frac{R_1 R_2}{R_1 + R_2} \equiv R_1 \parallel R_2 \quad (\text{EQ. 16})$$

The circuit to the left of X - Y is now replaced by the Thevenin equivalents.

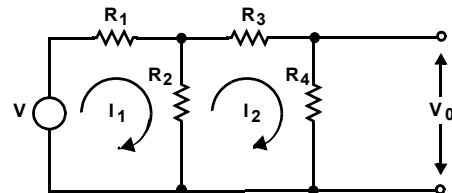


$$V_0 = V_{th} \frac{R_4}{Z_{th} + R_3 + R_4} \quad (\text{EQ. 17})$$

$$= V \frac{R_2}{R_1 + R_2} \frac{R_4}{\frac{R_1 R_2}{R_1 + R_2} + R_3 + R_4}$$

FIGURE 7. THE THEVENIN EQUIVALENT CIRCUIT

The loop equations are worked out below. Notice that not only is the derivation of the equations more laborious, but the labor will get out of hand with the addition of another loop. This is why Thevenin's theorem is preferred over loop equations.



$$V = I_1 (R_1 + R_2) - I_2 R_2 \quad (\text{EQ. 18})$$

$$I_2 (R_2 + R_3 + R_4) = I_1 R_2 \quad (\text{EQ. 19})$$

$$I_1 = \frac{R_2 + R_3 + R_4}{R_2} I_2 \quad (\text{EQ. 20})$$

$$I_2 \frac{(R_2 + R_3 + R_4)}{R_2} (R_1 + R_2) - I_2 R_2 \quad (\text{EQ. 21})$$

$$I_2 = \frac{V}{\frac{R_2 + R_3 + R_4}{R_2} (R_1 + R_2) - R_2} \quad (\text{EQ. 22})$$

$$V_0 = I_2 R_4 \quad (\text{EQ. 23})$$

$$V_0 = V \frac{R_4}{\frac{(R_2 + R_3 + R_4)(R_1 + R_2)}{R_2} - R_2} \quad (\text{EQ. 24})$$

FIGURE 8. LOOP EQUATION ANALYSIS OF THE SAME CIRCUIT

The Norton equivalent circuit is seldom used in circuit design, so its derivation [3] and illustration will be left to the serious student.

Superposition

The principle of superposition states that the equation for each independent source can be calculated separately, and then the equations (or results) can be added to give the total result. When implementing superposition the equation for

each source is calculated with the other independent voltage sources short circuited and the independent current sources open circuited. The equations for all the sources are added together to obtain the final answer.

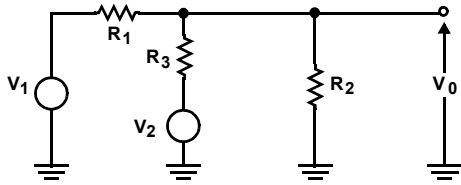


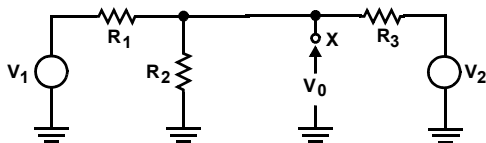
FIGURE 9. SUPERPOSITION EXAMPLE

$$V_{01}|_{V_2=0} = \frac{R_2 \parallel R_3}{R_1 + R_2 \parallel R_3} V_1 \quad V_{02}|_{V_1=0} = \frac{R_1 \parallel R_2}{R_3 + R_1 \parallel R_2} V_2 \quad (\text{EQ. 25})$$

$$V_0 = V_{01} + V_{02} = V_1 \frac{R_2 \parallel R_3}{R_1 + R_2 \parallel R_3} + V_2 \frac{R_1 \parallel R_2}{R_3 + R_1 \parallel R_2} \quad (\text{EQ. 26})$$

Analysis Tools - Why Do We Need More Than One?

Each one of the analysis tools shown has a place where it is optimal. Later during the op amp analysis the tools will be employed to relieve the burden of detailed calculation. Figures 10 and 11 illustrate an example of the extra calculations caused by using the less optimal tool to perform the analysis.



$$V_{th} = \frac{R_2}{R_1 + R_2} V_1 \quad R_{th} = R_1 \parallel R_2 \quad (\text{EQ. 27})$$

FIGURE 10. SUPERPOSITION EXAMPLE REDRAW

$$I = \frac{V_2 - V_{th}}{R_{th} + R_3} \quad V_0 = V_2 - IR_3 \quad (\text{EQ. 28})$$

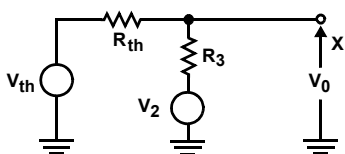


FIGURE 11. THEVENIN EQUIVALENT CIRCUIT MODEL

$$V_0 = V_2 - \frac{V_2 - V_{th}}{R_{th} + R_3} R_3 = V_2 - \frac{R_2 V_1}{R_1 \parallel R_2 + R_3} \quad (\text{EQ. 29})$$

Notice that the Thevenin method used twice as many equations to describe the circuit as were required to arrive at the same result with superposition. Also, the form of the final equation arrived at by superposition is much easier to analyze.

Feedback Principles

This discussion of feedback principles is simple because they are easy to understand. The application of the principles can be very complicated for the design engineer, but we can grasp the principles without understanding all of the nuances. If this material creates a thirst it may be slaked by reading references 2 and 3.

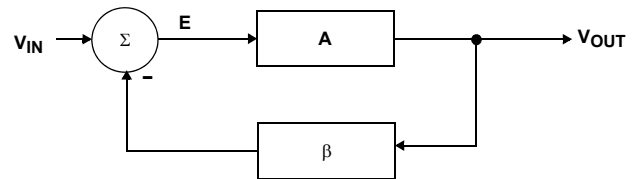


FIGURE 12. FEEDBACK BLOCK DIAGRAM

$$V_{OUT} = EA \quad (\text{EQ. 30})$$

$$E = V_{IN} - \beta V_{OUT} \quad (\text{EQ. 31})$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{A}{1 + A\beta} \quad (\text{EQ. 32})$$

Equations 30 and 31 are written on the block diagram, and Equation 32 is obtained by combining them to eliminate the error, \$E\$. If \$\beta = 1\$ in Equation 32 \$V_{OUT} = V_{IN}\$, or the feedback circuit has turned into a unity gain buffer. If \$\beta = 0\$ in Equation 32 \$V_{OUT} = AV_{IN}\$, or there is no feedback. Notice that the direct gain, \$A\$, does not control the feedback circuit closed loop gain; rather, the feedback factor, \$\beta\$, controls the closed loop gain in a feedback circuit. This is the essence of a feedback circuit; now the closed loop gain is a function of the feedback factor which is comprised of passive components. The closed loop gain error, stability and drift are now dependent on stable, accurate, and inexpensive passive components. The closed loop gain assumption is valid as long as \$A\beta \gg 1\$, also \$E \Rightarrow 0\$ if this assumption is valid.

If \$A\beta = -1\$ then Equation 32 becomes \$V_{OUT}/V_{IN} = 1/0\$, or it is indeterminate. If the energy in the circuit was unlimited the circuit would consume the world, but luckily it is limited, so the circuit oscillates from positive to negative saturation. This is an oscillator, thus the definition of an oscillator is that the gain be \$\ge 1\$ while the phase shift equals \$-180\$ degrees. Now we conclude that the feedback factor controls the closed loop gain, and the direct gain/feedback factor combination determines if the circuit will be stable or will be an oscillator.

The Op Amp Symbol

It is important to understand the op amp symbol shown in Figure 13. The -input, V-, is the inverting input, and the +input, V+, is the non-inverting input. The point of the triangle is the op amp output, and the op amp multiplies the differential voltage, (V+ - V-), by a large gain, a.

The Inverting Op Amp

Three assumptions are made in the calculation of the inverting op amp circuit equations. First, the current into the op amp inputs, I_B in Figure 13, is assumed to be zero; this is a valid assumption because the bias currents are usually much lower than signal currents. The second assumption is that the op amp gain, a, is extremely high, and this is a valid assumption in most situations where the op amp's bandwidth is much greater than the signal bandwidth. The third assumption, which is that the error voltage, V_E, equals zero, is a result of assuming an extremely high op amp gain. When a is very large V_{OUT} can assume any value required to drive the inverting input voltage to the non-inverting input voltage, so V_E will always be forced to zero.

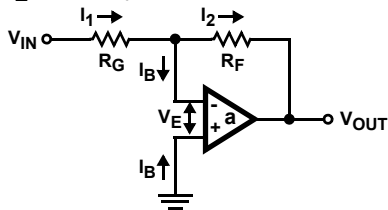


FIGURE 13. INVERTING OP AMP CIRCUIT

Assume I_B = 0, V_E = 0, a = ∞
Then:

$$I_1 = \frac{V_{IN}}{R_G} = I_2 = -\frac{V_{OUT}}{R_F} \tag{EQ. 33}$$

$$V_{IN} R_F = -V_{OUT} R_G \tag{EQ. 34}$$

$$\frac{V_{OUT}}{V_{IN}} = -\frac{R_F}{R_G} \tag{EQ. 35}$$

Equation 33 is written by applying Kirchoff's current law to the inverting node. Equation 35 is obtained through algebraic manipulation of Equations 33 and 34. Note that the ideal closed loop gain, Equation 33, does not contain the op amp gain, so it is independent of the op amp gain so long as the assumptions are valid.

The inverting op amp can be configured as an inverting adder as shown in Figure 14. The analysis is similar to that shown for the inverting amplifier, but it is easier to understand if the concept of a virtual ground is understood. Virtual is defined as "existing or resulting in effect though not in actual fact". The inverting node acts as a real ground because no voltage is developed across it, but the current path is restricted to the PC traces attached to the node. The non-inverting input of the op amp is connected to ground, thus if the error voltage is to be zero as was assumed, the inverting input functions as though it were tied to ground. Considering the virtual ground, the three currents flowing through R_{G1}, R_{G2}, and R_{G3} can be calculated separately.

Now superposition can be applied to the circuit; Equation 36 calculates the gain for each independent source, and Equation 37 recombines the separate gains.

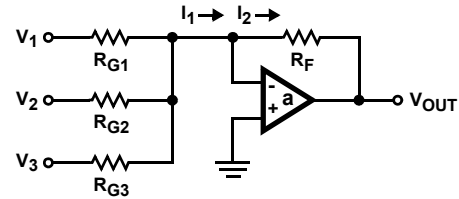


FIGURE 14. THE INVERTING ADDER

$$V_{O1} = -V_1 \frac{R_F}{R_{G1}}, V_{O2} = -V_2 \frac{R_F}{R_{G2}}, V_{O3} = -V_3 \frac{R_F}{R_{G3}} \tag{EQ. 36}$$

$$V_{OUT} = V_{O1} + V_{O2} + V_{O3} = -V_1 \frac{R_F}{R_{G1}} - V_2 \frac{R_F}{R_{G2}} - V_3 \frac{R_F}{R_{G3}} \tag{EQ. 37}$$

If R_F / R_{GX} = 1 Then;

$$V_{OUT} = -(V_1 + V_2 + V_3) \tag{EQ. 38}$$

The Non-Inverting Op Amp

Referring to Figure 15, because V_E is equal to zero the voltage at point X is equal to V_{IN}. There is voltage divider formed by the feedback resistor, R_F, and the gain setting resistor, R_G, and the voltage divider input voltage is the output voltage of the op amp. Equation 39 is written using the voltage divider rule, and Equation 40 is obtained through algebraic manipulation. Notice that the ideal closed loop gain is again independent of the op amp gain.

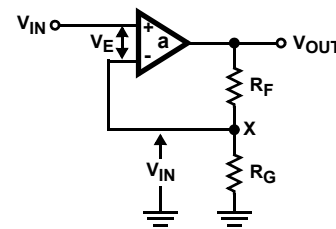


FIGURE 15. NON-INVERTING OP AMP

$$V_{IN} = \frac{V_{OUT} R_G}{R_F + R_G} \tag{EQ. 39}$$

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_F + R_G}{R_G} \tag{EQ. 40}$$

The Differential Amplifier

The differential amplifier schematic is given in Figure 16, and the analysis will be done in two parts because we will use superposition. Two output voltages, one corresponding to each input voltage source, will be calculated separately and added together. The output from V₁ is calculated in Equation 42; V+ is first calculated with the voltage divider rule, and then it is substituted into the non-inverting gain equation yielding Equation 43. The output from V₂ is calculated from the inverting gain equation in Equation 44. The

results of Equations 43 and 44 are added in Equation 45 to obtain the complete circuit equation. Notice that the output is a function of the difference between the two input voltages, this accounts for the name differential amplifier.

If a small signal is riding on a large signal, say 10mV, 0.001Hz riding on 5V_{DC}, the DC can be stripped off by putting the combined signal into the non-inverting input, and putting 5V_{DC} into the inverting input. The 5V_{DC} becomes a common mode signal (a signal which is common to both inputs), so it is rejected by the differential amplifier if $R_1 = R_3$, and $R_2 = R_4$.

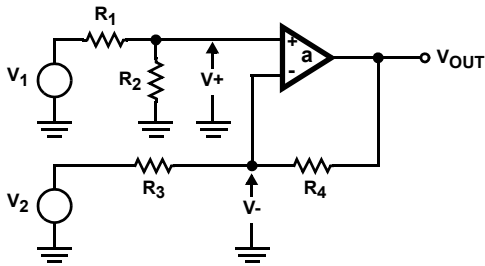


FIGURE 16. THE DIFFERENTIAL AMPLIFIER

$$V_{OUT} = V_{OUT_1} + V_{OUT_2} \tag{EQ. 41}$$

$$V_{OUT_1} = V_+ \left(1 + \frac{R_4}{R_3} \right) \quad V_+ = V_1 \frac{R_2}{R_1 + R_2} \tag{EQ. 42}$$

$$V_{OUT_1} = V_1 \frac{R_2}{R_1 + R_2} \left(\frac{R_3 + R_4}{R_3} \right) \tag{EQ. 43}$$

$$V_{OUT_2} = V_2 \left(- \frac{R_4}{R_3} \right) \tag{EQ. 44}$$

$$V_{OUT} = V_1 \frac{R_2}{R_2 + R_1} \left(\frac{R_3 + R_4}{R_3} \right) - V_2 \frac{R_4}{R_3} \tag{EQ. 45}$$

If $R_1 = R_3$ and $R_2 = R_4$

$$V_{OUT} = (V_1 - V_2) \frac{R_4}{R_3} \tag{EQ. 46}$$

This effect could be accomplished through the use of a coupling capacitor, but because the frequency of the signal is so low the capacitor value and size would be too big. The differential amplifier also rejects AC common mode signals. Data transmission schemes often use twisted pairs for the interconnections so that any noise coupled on the lines will be common mode. Differential amplifiers are used as receivers in this data transmission scheme because they reject the common mode noise while amplifying the signal.

T Networks in the Feedback Path

Putting a T network in the feedback path as shown in Figure 17 complicates the analysis, but offers the advantage of high closed loop gain coupled with low value feedback resistors. This configuration is also useful for some filter configurations. Thevenin's theorem is applied as shown in Figure 18. Look into R_4 from X, Y and calculate the

Thevenin equivalent voltage and resistance, then redraw the circuit as shown in Figure 18. Now the inverting gain can be calculated in the normal manner using the algebraic simplification shown in Equation 48.

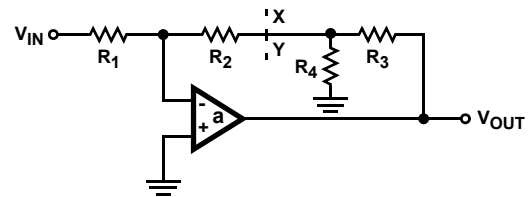


FIGURE 17. T NETWORK IN THE FEEDBACK PATH

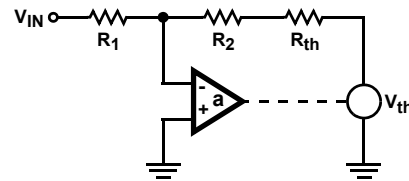


FIGURE 18. THEVENIN ANALYSIS OF T NETWORKS IN THE FEEDBACK PATH

$$V_{th} = \frac{V_0 R_4}{R_3 + R_4} \quad R_{th} = R_3 \parallel R_4 - \frac{V_{th}}{V_{IN}} = \frac{R_2 + R_{th}}{R_1} \tag{EQ. 47}$$

$$\begin{aligned} - \frac{V_{OUT}}{V_{IN}} &= \frac{R_2 + R_{th}}{R_1} \frac{R_3 + R_4}{R_4} = \frac{R_2 + \frac{R_3 R_4}{R_3 + R_4}}{R_1} \frac{R_3 + R_4}{R_4} \\ &= \frac{R_2 + R_3 + \frac{R_2 R_3}{R_4}}{R_1} \end{aligned} \tag{EQ. 48}$$

Video Amplifiers

Until now we have implicitly assumed that all op amps are the same. This is not true, but because the ideal closed loop equations are identical, it is a workable assumption. The two big classifications of op amps are voltage feedback and current feedback. The type of feedback is not the only difference between these op amps. The internal circuit configurations are dramatically different, so much so that recommended reference #1 dwells on voltage feedback while reference #2 dwells on current feedback. Whenever an op amp is used in a high frequency circuit such as a video amp there is a strong likelihood that it will be a current feedback op amp. Again, because the closed loop ideal gain equations are identical for voltage and current feedback op amps we will not distinguish between them.

In Figure 19, R_{IN} is usually the terminating resistance for the input cable, and it is usually 50Ω or 75Ω. R_M is the matching resistance for the cable being driven, and R_T is the terminating resistance for the driven cable. R_T is often shown here for gain calculations while it is physically placed at the cable end. Using Equation 49, we see that when $R_G = R_F$ and $R_M = R_T$, the overall circuit gain is one.

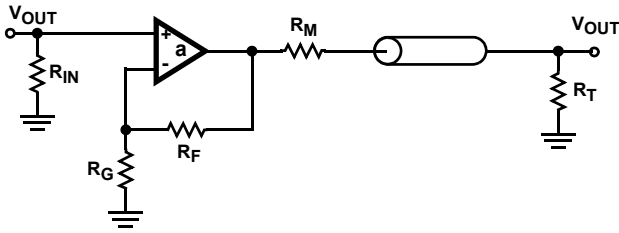


FIGURE 19. A TYPICAL VIDEO AMPLIFIER

$$\frac{V_{OUT}}{V_{IN}} = \frac{R_F + R_G}{R_G} \frac{R_T}{R_M + R_T} \quad (EQ.49)$$

AC Theory

The emphasis here is on capacitors because they are responsible for the vast majority of AC effects. The capacitor has an impedance and a phase shift both of which are a function of frequency. Although it is paramount in stability calculations, we will neglect the phase shift because you can obtain a reasonable understanding of circuit performance by just considering the impedance. Referring to Equation 50 it is apparent that when the frequency is very high, $s = j\omega$ is very high, so the capacitor impedance, X_C , is very low. The converse happens when the frequency is very low.

The key to this section of AC theory is that high frequency means low capacitive impedance, and low frequency means high capacitive impedance. At $F = \infty$, $X_C = 0$, and at $F = 0$, $X_C = \infty$. At intermediate values of frequency the capacitive impedance must be calculated with the assistance of Equation 50.

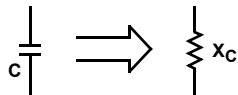


FIGURE 20. CAPACITOR IMPEDANCE

$$X_C = \frac{1}{sC} = \frac{1}{j\omega C} \quad \text{where } s = j\omega \text{ and } j = \sqrt{-1} \quad (EQ.50)$$

Op Amp Circuits Containing Capacitors

Referring to Figure 21, when $F = 0$, $X_C = \infty$ so the gain, $G = -R_F/R_G$. When $F = \infty$, $X_C = 0$ then $G = 0$. The gain starts off high and decreases to zero at very high frequencies. Very often C_F is an unwanted stray capacitor which yields an undesirable effect; namely, the circuit loses high frequency performance.

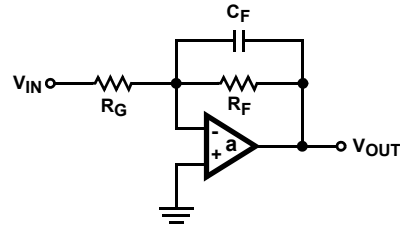


FIGURE 21. LOW PASS FILTER

A high pass filter is shown in Figure 22. At $F = 0$ the gain is $(R_F + R_G)/R_F$, and at very high frequencies the gain tries to approach the op amp gain, a . Sometimes the stray input capacitance forms this circuit, and the result is unwanted peaking or overshoot because the capacitor phase shift tends to make the circuit unstable.

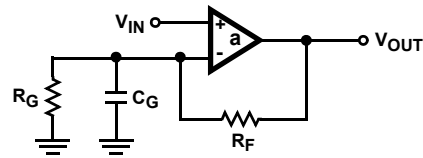


FIGURE 22. HIGH PASS FILTER

This general method is useful for analyzing the performance of op amp circuits which have capacitors. Depending on where they are connected the capacitors can stabilize or destabilize the op amp, but they always shape the transfer function in the frequency domain.

Conclusion

Some algebra, the basic laws of physics, and the basic circuit laws are adequate to gain an understanding of op amp circuits. By applying these tools to various circuit configurations it is possible to predict performance. Further in-depth knowledge is required to do op amp design, and there are many sources where this knowledge can be obtained. Don't hesitate to try some of these tricks on your local circuit design engineer, but be aware that it may result in a long lecture about circuit design.

References

- [1] Intersil Corporation, Application Note 9415.
- [2] Intersil Corporation, Application Note 9420.
- [3] Van Valkenberg, N.E., Network Analysis, Prentice-Hall, 1964.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.
(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)



SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338