

Introduction

The SPICE model for the ISL705XRH and ISL706xRH rad hard supervisory circuits were developed to help system designers evaluate the operation of this IC prior or in conjunction with proto-typing a system design. This model accurately simulates typical performance characteristics at room temperature (+25 °C) such as steady state switching, input voltage and output current transients. Behaviors not supported are temperature analysis, process variation, and AC analysis. Functionality has been tested on ORCAD 10.0 and CADENCE ORCAD 16.3. Other SPICE simulators may be used however the model may require translation.

Reference Documents

- ISL705ARH, ISL705BRH, ISL705CRH, ISL706ARH, ISL706BRH, ISL706CRH Datasheet, [FN7662](#)
- ISL705RH Voltage Supervisory Circuit Evaluation Board User's Guide, [AN1650](#)
- ISL706RH Voltage Supervisory Circuit Evaluation Board User's Guide, [AN1671](#)

License Statement

The information in this SPICE model is protected under the United States copyright laws. Intersil Corporation hereby grants users of this macro-model hereto referred to as "Licensee", a nonexclusive, nontransferable license to use this model as long as the Licensee abides by the terms of this agreement. Before using this macro-model, the Licensee should read this license. If the Licensee does not accept these terms, permission to use the model is not granted.

The Licensee may not sell, loan, rent, or license the macro-model, in whole, in part, or in modified form, to anyone outside the Licensee's company. The Licensee may modify the macro-model to suit his/her specific applications, and the Licensee may make copies of this macro-model for use within their company only.

This macro-model is provided "AS IS, WHERE IS, AND WITH NO WARRANTY OF ANY KIND EITHER EXPRESSED OR IMPLIED, INCLUDING BUY NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY AND FITNESS FOR A PARTICULAR PURPOSE."

In no event will Intersil be liable for special, collateral, incidental, or consequential damages in connection with or arising out of the use of this macro-model. Intersil reserves the right to make changes to the product and the macro-model without prior notice.

Project Files

The zip file: **ISL705xRH_ISL706xRH SPICE FILES.zip** contains the project file ISL705ARH.opj to be used in ORCAD simulator. The project file contains two schematics which correlate with the ISL705XRH and ISL706XRH evaluation boards (see Figures 8 and 9). For details on the application schematic refer to the evaluation board user's guide [AN1650](#) and [AN1671](#). Each schematic has been set up with a time domain simulation profile for quick evaluation of the model. The schematic pages may be accessed through the main directory window in ORCAD (see Figure 1).

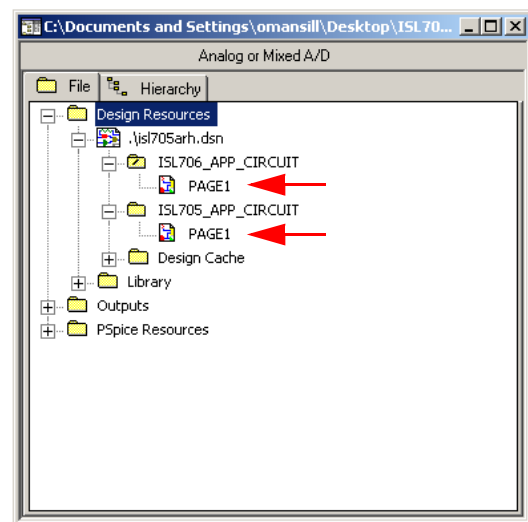


FIGURE 1. APPLICATION SCHEMATIC LOCATION

Figures 2 through 7 show simulation results of the RESET and PFI transient response. These can be compared to Figure 8 through 13 of the datasheet for model accuracy.

Model Parameter List

The model has been developed with a single netlist with multiple variables that are automatically modified to meet IC parameters when the part is placed in an ORCAD schematic from the model library. If the user would like to import the netlist to another SPICE simulator the variables must be entered manually. The parameter list spreadsheet maps the variable state to the corresponding version of the IC, so the user can easily modify the netlist and import the model to other SPICE simulators.

Simulation Performance Curves

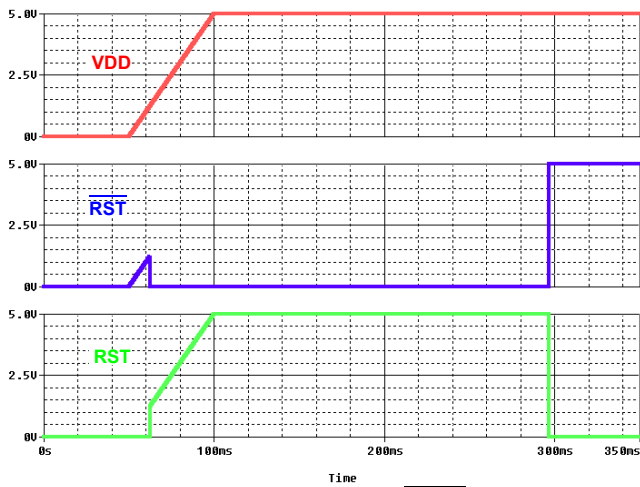


FIGURE 2. ISL705xRH RESET AND $\overline{\text{RESET}}$ ASSERTION

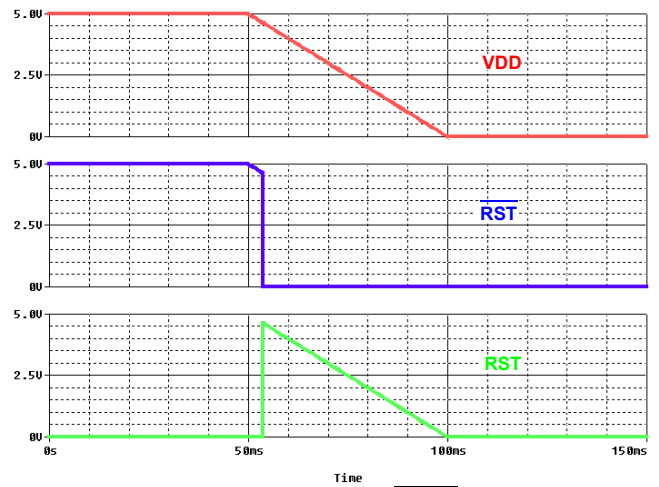


FIGURE 3. ISL705xRH RESET and $\overline{\text{RESET}}$ DEASSERTION

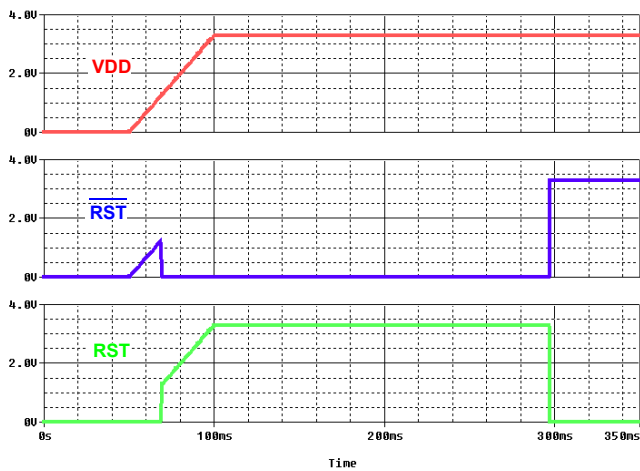


FIGURE 4. ISL706xRH RESET AND $\overline{\text{RESET}}$ ASSERTION

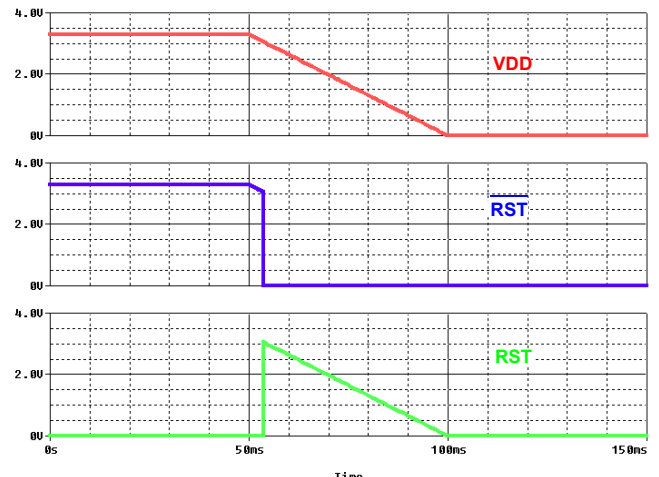


FIGURE 5. ISL706xRH RESET and $\overline{\text{RESET}}$ DEASSERTION

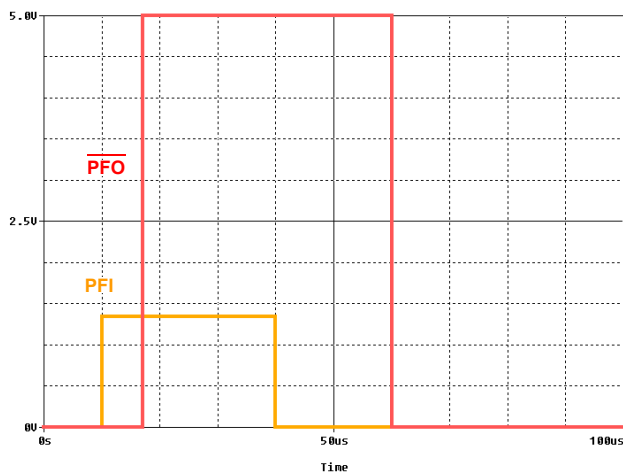


FIGURE 6. ISL705xRH PFI TO $\overline{\text{PFO}}$ RESPONSE

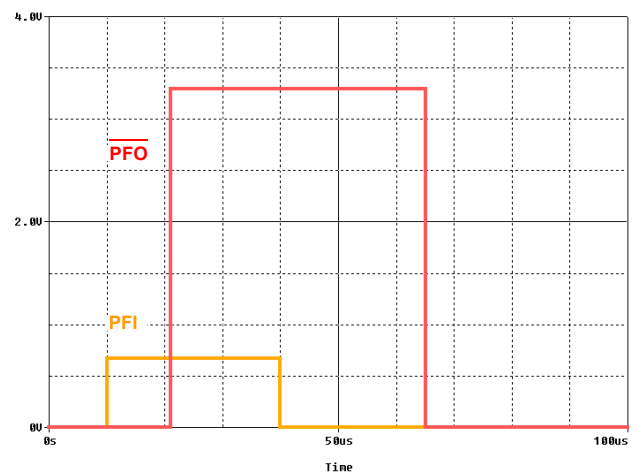
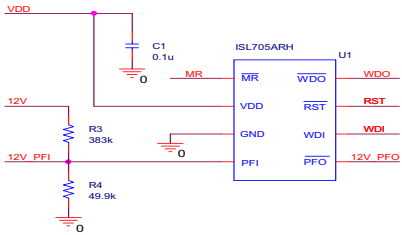
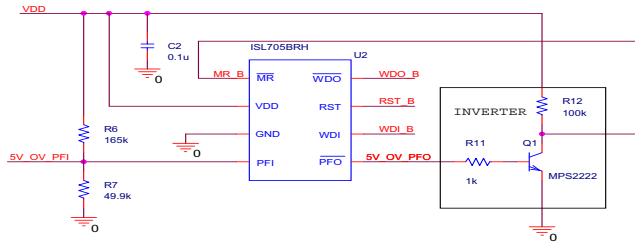


FIGURE 7. ISL706xRH PFI TO $\overline{\text{PFO}}$ RESPONSE

SECTION 1 (ISL705ARH)



SECTION 2 (ISL705BRH)



SECTION 3 (ISL705CRH)

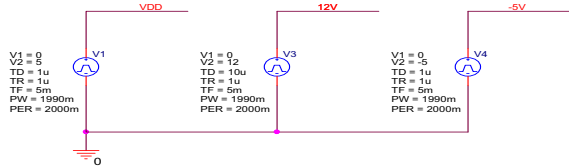
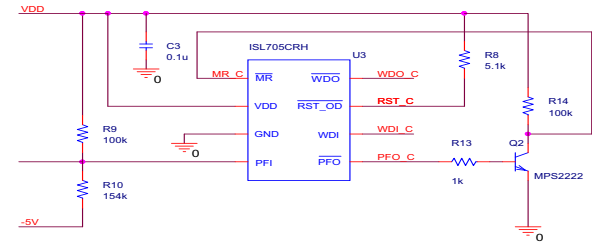
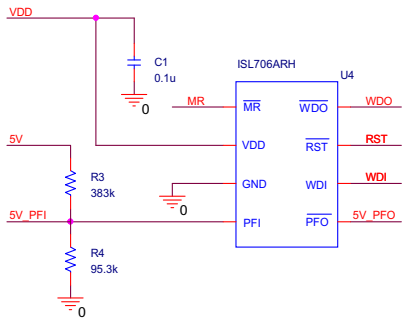
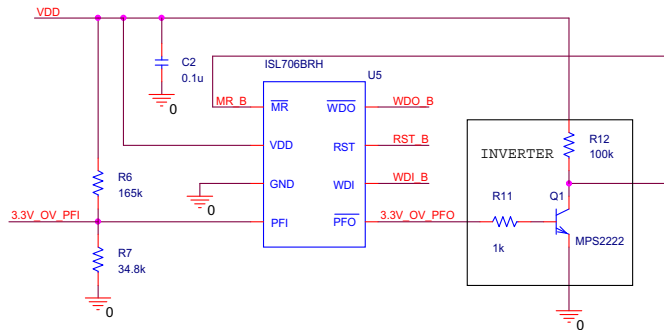


FIGURE 8. ISL705xRH SIMULATION APPLICATION SCHEMATIC

SECTION 1 (ISL706ARH)



SECTION 2 (ISL706BRH)



SECTION 3 (ISL706CRH)

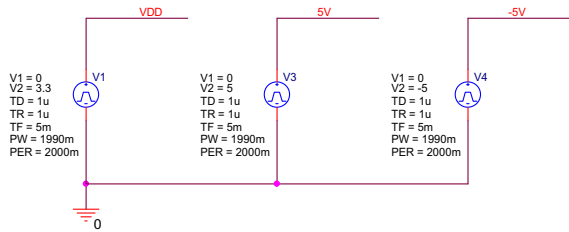
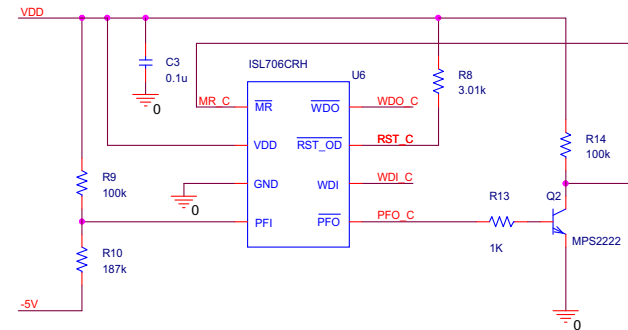


FIGURE 9. ISL706xRH SIMULATION APPLICATION SCHEMATIC

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.