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M16C/64 Group

A/D Converter Operation (Single-Sweep Mode)

1. Abstract

In single-sweep mode, any desired function can be selected from those listed in Table 1. In this application note, the operation of the function selected from the items in Table 1 (marked with a circle) is described.

Table 1. Contents of Settings

Set item	Content of setting		Set item	Content of setting	
Operating clock φAD	○	fAD divided by 12/ fAD divided by 6 /fAD divided by 4/ fAD divided by 3/ fAD divided by 2/ fAD	Analog input pin	○	2 pins (AN0, AN1/ AN0_0, AN0_1/ AN2_0, AN2_1)
					4 pins (AN0–AN3/ AN0_0–AN0_3/ AN2_0–AN2_3)
A/D conversion start condition	○	Software trigger			6 pins (AN0–AN5/ AN0_0–AN0_5/ AN2_0–AN2_5)
		$\overline{\text{ADTRG}}$ trigger			
A/D input group	○	Port P10 group (AN0–AN7)			8 pins (AN0–AN7/ AN0_0–AN0_7/ AN2_0–AN2_7)
		Port P0 group (AN0_0–AN0_7)			
		Port P2 group (AN2_0–AN2_7)			

2. Introduction

The application example presented in this document applies to the microcomputers listed below.

・Microcomputers: M16C/64 group

This application note can be used with other M16C Family MCUs which have the same special function registers (SFRs) as the above group. Check the manual for any modifications to functions. Careful evaluation is recommended before using the program described in this application note.

3. Application Example

Operation (1) When the ADCON0 register's ADST bit is set to 1 (A/D conversion start), the A/D converter starts operating, to convert the input voltage on AN0 pin from analog to digital quantities.

(2) When the A/D conversion on AN0 pin is finished, the content of the successive approximation register (conversion result) is transferred to the AD0 register. The A/D converter continues to perform an A/D conversion on the next analog input pin selected. Each time conversion on one pin is finished, the conversion result is transferred to the ADi register (i = 0–7) corresponding to the respective pins.

(3) When A/D conversions on all of selected analog input pins are finished, the ADIC register's IR bit is set to 1 (interrupt requested). At the same time, the ADCON0 register's ADST bit is cleared to 0 (A/D conversion stopped), causing the A/D converter to stop operating.

Figure 1 shows an operation timing of the A/D converter.

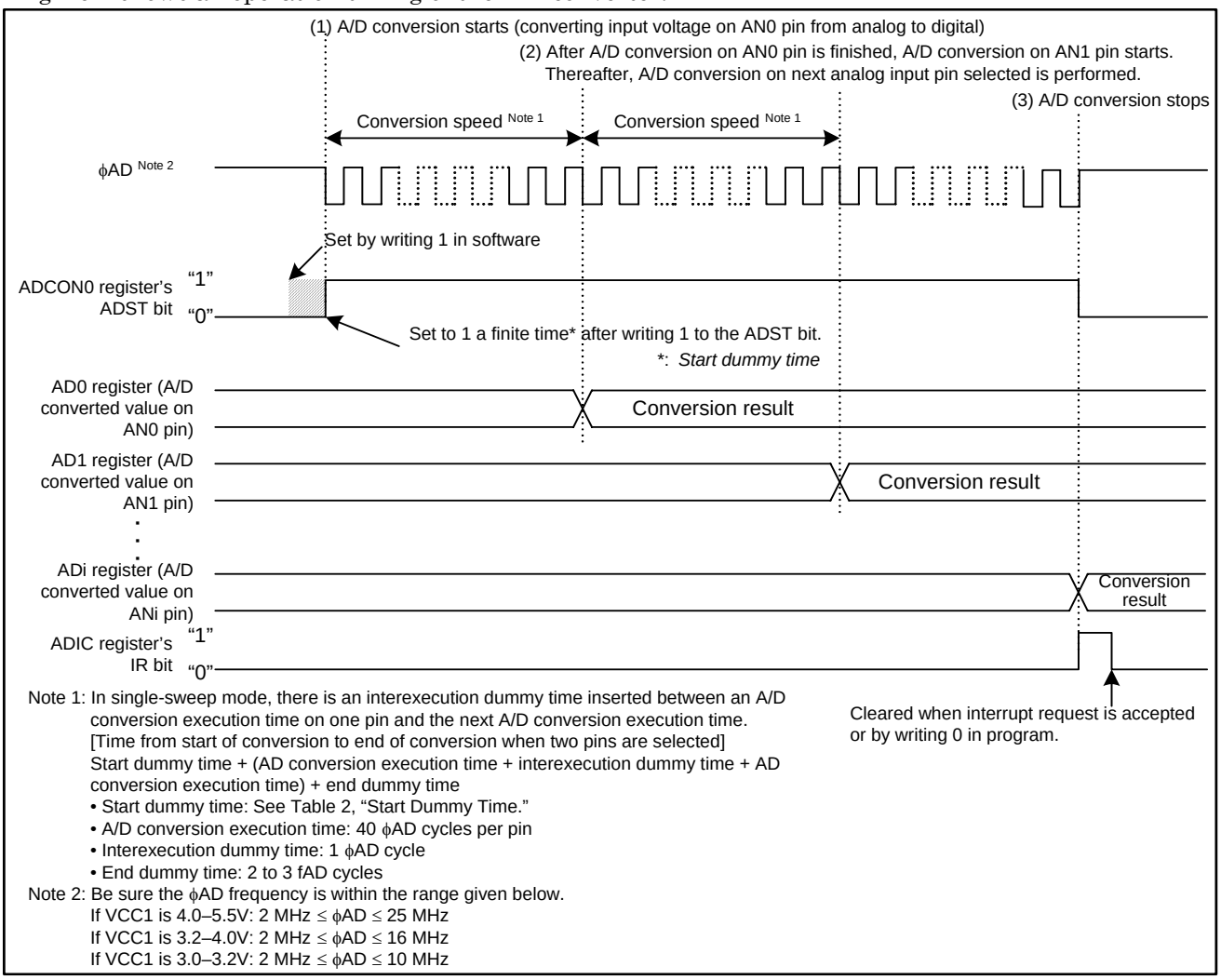


Figure 1. Operation Timing in Single-Sweep Mode

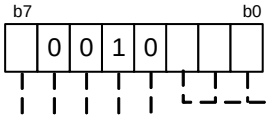
Table 2. Start Dummy Time

Selected ϕAD	Start dummy time	Selected ϕAD	Start dummy time
fAD	1 to 2 fAD cycles	fAD divided by 4	3 to 4 fAD cycles
fAD divided by 2	2 to 3 fAD cycles	fAD divided by 6	4 to 5 fAD cycles
fAD divided by 3	3 to 4 fAD cycles	fAD divided by 12	7 to 8 fAD cycles

4. How to Set Up

The following shows how to set up the registers to accomplish the operation described in Section 3, "Application Example." For details about each register, see the hardware manual of the M16C/64 group.

(1) Set up the A/D control register 0, A/D control register 1, and A/D control register 2.

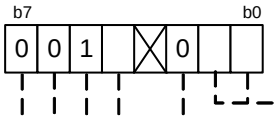


A/D control register 0 (ADCON0)

- CH2–CH0 Analog input pin select bits
  Have no effect in single-sweep mode.
- MD0–MD1 A/D operation mode select bits
  10: Single-sweep mode
- TRG Trigger select bit
  0: Software trigger
- ADST A/D conversion start flag
  0: A/D conversion stopped
- CKS0 Clock frequency select bit Note 1

Note 1: Selection of the operating clock, ϕAD
The clock ϕAD is selected using the following register bits in combination.
- ADCON0 register's CKS0 bit
- ADCON1 register's CKS1 bit
- ADCON2 register's CKS2 bit

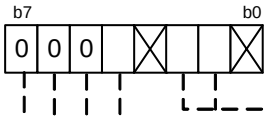
CKS2	CKS1	CKS0	ϕAD
0	0	0	fAD divided by 4
0	0	1	fAD divided by 2
0	1	0	fAD
0	1	1	
1	0	0	fAD divided by 12
1	0	1	fAD divided by 6
1	1	0	fAD divided by 3
1	1	1	



A/D control register 1 (ADCON1)

- SCAN0–SCAN1 A/D sweep pin select bits
  00: AN0–AN1 (2 pins)
  01: AN0–AN3 (4 pins)
  10: AN0–AN5 (6 pins)
  11: AN0–AN7 (8 pins)
- MD2 A/D operation mode select bit 1
  0: Other than repeat sweep mode 1
- CKS1 Clock frequency select bit 1 Note 1
- ADSTBY A/D standby bit
  1: A/D operation ready
- ADEX1–ADEX0 Extension pin select bits
  00: ANEX0, ANEX1 pins unused

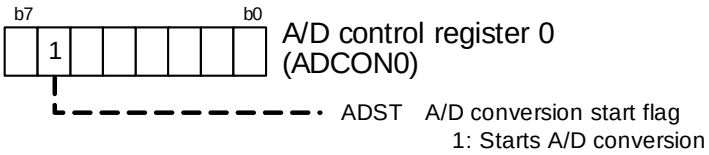
If the ADSTBY bit is changed from 0 (A/D operation stopped) to 1 (A/D operation ready), wait 1 ϕAD cycle or more before starting A/D conversion.



A/D control register 2 (ADCON2)

- ADGSEL1–ADGSEL0 A/D input group select bits
  00: Selects port P10 group
  01: Setting prohibited
  10: Selects port P0 group
  11: Selects port P2 group
- CKS2 Clock frequency select bit 2 Note 1
- Reserved bits
  Set these bits to 0.

(2) Start A/D conversion.

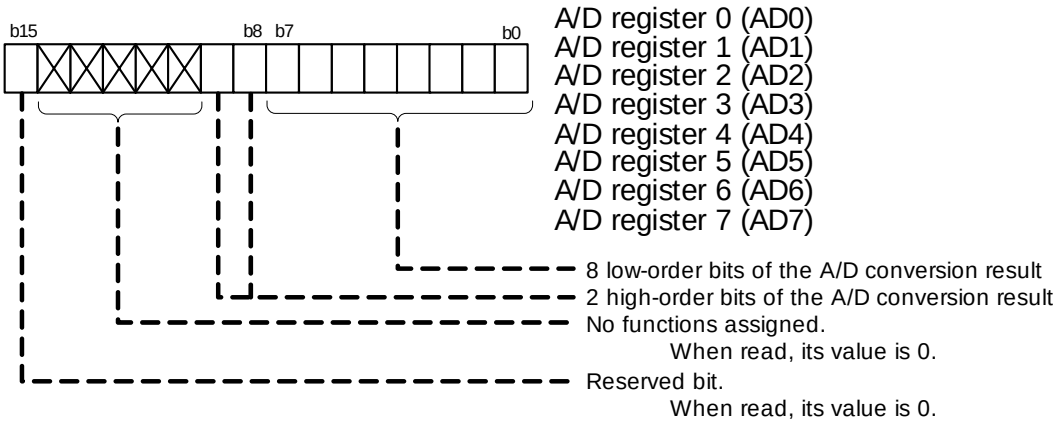


(3) Wait until A/D conversion finishes.

When A/D conversions on all of selected analog input pins are finished, the ADIC register' s IR bit is set to 1 (interrupt requested). At the same time, the ADST bit is cleared to 0 (A/D conversion stopped).

The ADST bit reads 0 when it is read before an A/D conversion starts after writing 1 to the ADST bit.

(4) Read out the conversion result.



5. Reference Sample Programs

Download reference sample programs from the Renesas Technology website.

Click the screen menu “Application Note” on the left side of the M16C family top page.

6. Reference Documents

Hardware manuals

M16C/64 Group Hardware Manual

(Obtain the latest edition from the Renesas Technology website.)

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