1 + 1 HITLESS PROTECTION SWITCHING WITHOUT RELAYS FOR TRANSCEIVER IDT82P2281/2/4/8

Application Note AN-511

INTRODUCTION

In today's telecommunication systems, ensuring no traffic loss is becoming increasingly important. More and more, people are relying on internet to conduct financial transactions, make telephone calls and perform video conferencing. Loss of data could have a devastating effect including the losing or delaying of a critical financial transaction, hearing annoying flickering noises on the telephone lines, or viewing lousy video clips.

To combat these problems, redundancy protection must be built into the systems carrying this traffic. Although there are many types of redundancy protection schemes, linear 1+1 hardware protection implementation with the IDT82P2281/2/4/8 T1/E1/J1 Long Haul / Short Haul Transceivers is the subject of this application note. As will be shown in this document, the Transceiver enables system design to achieve high reliability, low switching latency and ease of service.

The forgoing sections will discuss the implementation of T1/E1/J1 1+1 relay-less hitless protection switching (HPS) using the Transceiver series from IDT. Section 1 will discuss how the Transceiver is used in such applications. It begins by explaining the concept of 1+1 relay-less hitless protection. Then it describes implementation of redundancy protection using the IDT82P2281/2/4/8. After describing the receive line interface design, it will detail the transmit side. For both the transmit and receive line interfaces, internal and external line impedance matching will be discussed in detail. Section 2 will briefly touch on the principle of hot-switch and hot-swap. Section 3 provides some general design guidelines. Following the discussion of test results using the IDT82P2288 evaluation board in Section 4 is the conclusion of the report described in Section 5.

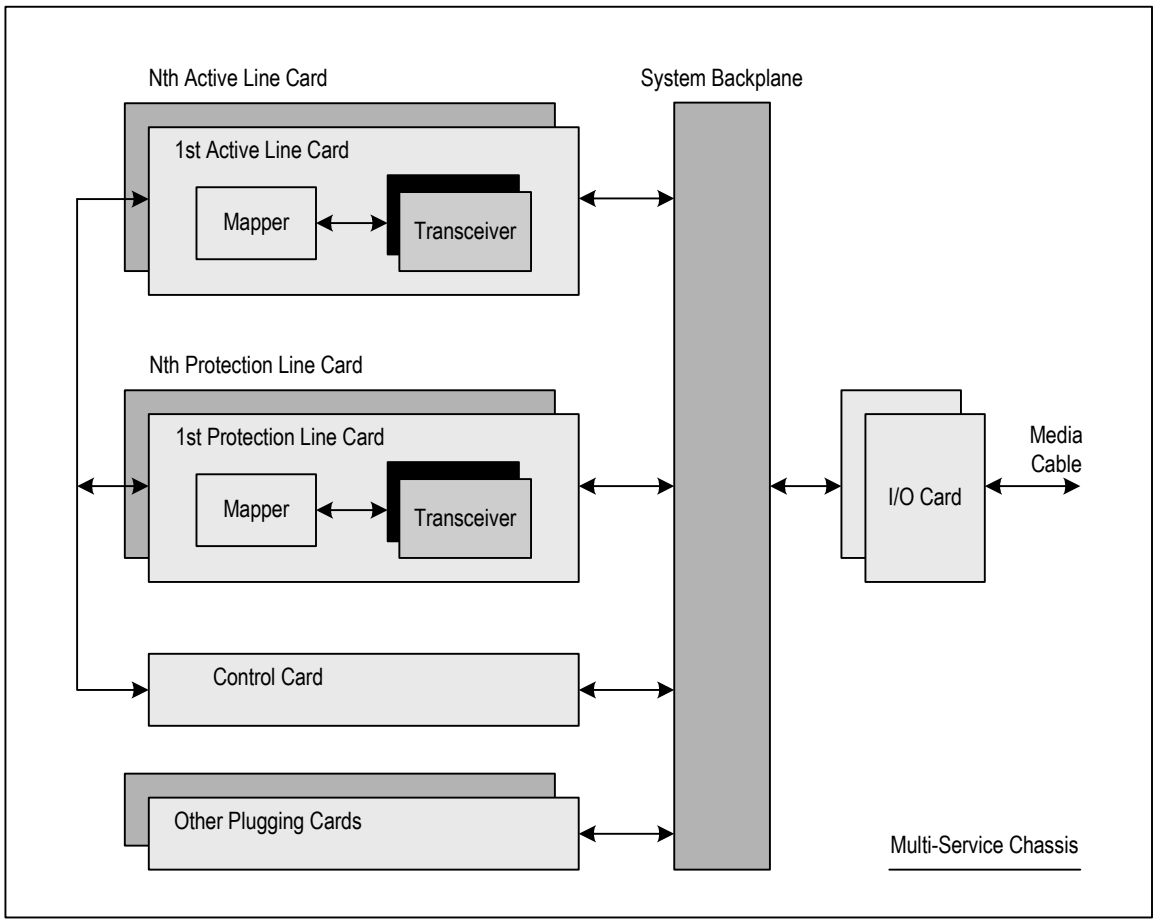

Figure 1. System Application Diagram

1 IDT82P2281/2/4/8 1 + 1 RELAY-LESS HITLESS PROTECTION SWITCHING

1.1 WHAT IS T1/E1/J1 1 + 1 RELAY-LESS HITLESS PROTECTION SWITCHING

T1/E1/J1 1+1 relay-less hitless protection switch or relay-less HPS is a means to provide 100% linear redundancy for T1/E1/J1. In the T1/E1/J1 1+1 redundancy scheme, there are two identical cards: a primary and secondary or protection card. The primary card is active and the secondary card is always in hot standby. They share the same line interface. If the primary card fails, the traffic is switched to the secondary card.

In the older generation of T1/E1/J1 line cards, the primary and secondary cards share the same line by use of multiple mechanical relays. When the primary card fails, the switching from the primary to the secondary card relies on mechanical relays. Mechanical relays are not only costly but have a lot of drawbacks as well. First, the relays require drivers to switch them. This implies bigger bill of materials and results in higher system cost as well as potentially more reliability issues from the relays and drivers. Secondly, the relays are big and take up a lot of room on PCB. Depending on the types of relay, each could take up to an area of 10 mm^2. As traffic volume grows, more channels or line cards are required to handle heavier traffic load. The mechanical relays result in bigger and more costly boxes. Finally, mechanical relays have higher switching latency. Depending on the relays, it could take up to tens of milliseconds to switch the relays. During this time, there are enough bit errors to jeopardize mission-critical traffic.

In the relay-less hitless protection switching T1/E1/J1 line cards, switching traffic from the primary to backup card is accomplished by the monolithic Transceiver. Relays are eliminated from the system resulting in a fewer components, higher reliability, better performing and cost effective system. The IDT82P2281/2/4/8 is the latest T1/E1/J1 silicon from IDT to enable low latency relay-less redundancy applications.

1.2 TRANSCEIVER

The IDT82P2281/2/4/8 T1/E1/J1 Long Haul / Short Haul Transceiver products consist of IDT82P2281 (single), IDT82P2282 (dual), IDT82P2284 (quad) and IDT82P2288 (octal). They have fast high-impedance output line drivers, arbitrary waveform generator at the transmit output, and internal/external line impedance matching capability. The transmit high impedance driver enables 1+1 redundancy applications without extra mechanical relays and still achieves excellent analog performance. Likewise, the receiver input has high-impedance and enables parallel connection with the backup receiver input without affecting the receive traffic.

Figure 1 illustrates the implementation of the IDT82P2281/2/4/8 in 1+1 relay-less hitless protection switching. It shows a typical multi-service chassis populated with T1/E1/J1 line cards. There are 2xN line cards, control card, backplane connector and I/O cards as detailed in the follows:

- 1st to Nth active cards - These are T1/E1/J1 primary cards populated with multiple IDT82P2281/2/4/8.
- 1st to Nth protection cards - These are T1/E1/J1 secondary cards populated with multiple IDT82P2281/2/4/8 and are in hot standby. Each line card has a backup line card and connects to the same traces to the backplane.
- I/O cards - These cards consist of transformer and metallic line protection devices, plugged into the backplane and are shared among the primary and secondary cards.
- Control card - If one of the active cards failed, the control card detects it, high-impedances the active card and turns on the backup card. The IDT82P2281/2/4/8 has fast high-impedance output driver to ensure hitless switching during hot-switch.
- Other Plugging Cards - These cards represent other functional cards specified by the multi-service chassis.

1.3 RECEIVE LINE SCHEMATIC

Figure 2 describes the receive line interface circuit for the IDT82P2281/2/4/8 in a 1+1 HPS implementation. The example shown in this figure consists of the primary, secondary and interface card all connecting to the same backplane. Only one transformer is required to be shared between the working and redundant cards. The recommended AC coupling capacitors are either 0.22 µF or 0.47 µF. The termination resistor Rr is recommended in Table 1. The 470 Ω resistors are recommended for DC current isolation. Furthermore, to meet some of the surge requirements of GR1089, a primary protection circuit with a transient voltage suppressor and a secondary surge protection provided by the diodes is recommended. Table 1 provides the component values and manufacturers tested by IDT to meet the above requirements.

1.3.1 INTERNAL

The IDT82P2281/2/4/8 provides internal and external line impedance matching capability. The device integrates active components to match T1/E1/J1 and high impedance by programming the R_TERM[2:0] bits. In HPS, it is recommended to use the external impedance mode of the device, where the receive input impedance is 120 kΩ. The high input impedance ensures no signal degradation in hot-switch or hot-swap. With the external impedance mode, a single 120 Ω resistor is sufficient to satisfy 100, 110 and 120 Ω requirements for T1/E1/J1 twisted pairs applications; for coax application, the recommended termination resistor is 75 Ω. Although the internal impedance mode is an option for the receive input, it is not recommended for HPS. The internal impedance mode could potentially alter the input signal and result in bit errors.

Table 1: RX Components

Components	Values
R	470 Ω
C	0.22 µF or 0.47 µF
SD	TECCOR P0640SC
D1, D2, D3, D4	International Rectifier, IR10BQ040
T1	1:1 turn ratio. 0553-0013-AC (Belfuse), T1108 (Pulse)
Rr	T1/E1/J1 - 120 Ω; Coax - 75 Ω

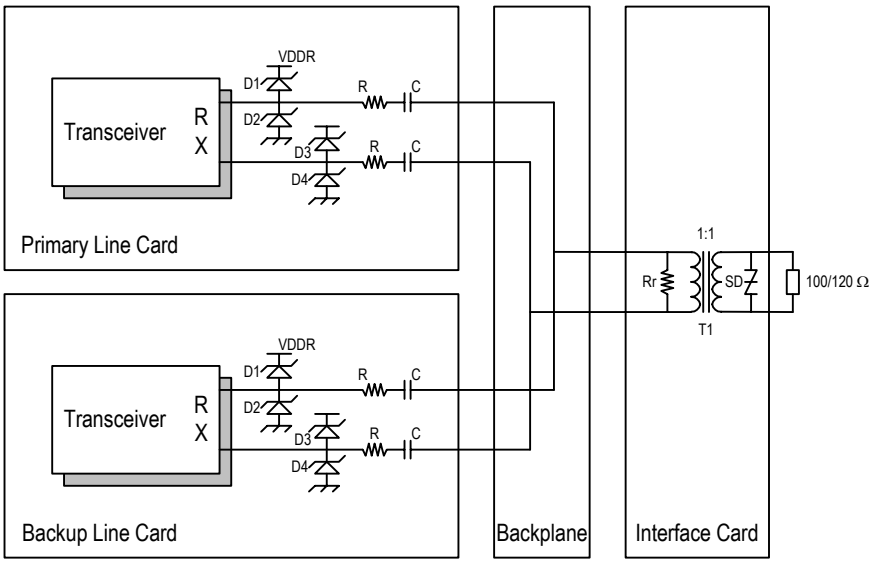

Figure 2. Receive Line Interface Schematic

1.4 TRANSMIT LINE SCHEMATIC

Figure 3 delineates the transmit line interface circuit for the IDT82P2281/2/4/8 in 1+1 HPS implementation. Primary, secondary and interface cards are connected to the same backplane. Only a single 1:2 turn ratio transformer and a single Cp capacitor are shared between the working and protection cards. The Cp value affects the pulse shape and return loss. The value can be adjusted to match different load conditions. The DC decoupling capacitors with a value of 0.47 µF are recommended to prevent DC bias difference between cards. Table 2 provides the list of component values and manufacturers tested by IDT for the above requirements.

1.4.1 INTERNAL

Internal line impedance matching is recommended as it requires fewest components. With the internal impedance matching, the primary card is programmed to be in active or normal mode, while the secondary card is programmed to be in high impedance mode.

Table 2: TX Components

Components	Values
C	0.47 µF
Cp	560 pF, 50 V (Adjustable from 0 ~ 1200 pF)
SD	TECCOR P0640SC
T1	1:2 turn ratio. 0553-0013-HC (Belfuse), T1108 (Pulse)
D1, D2, D3, D4	International Rectifier, IR10BQ040

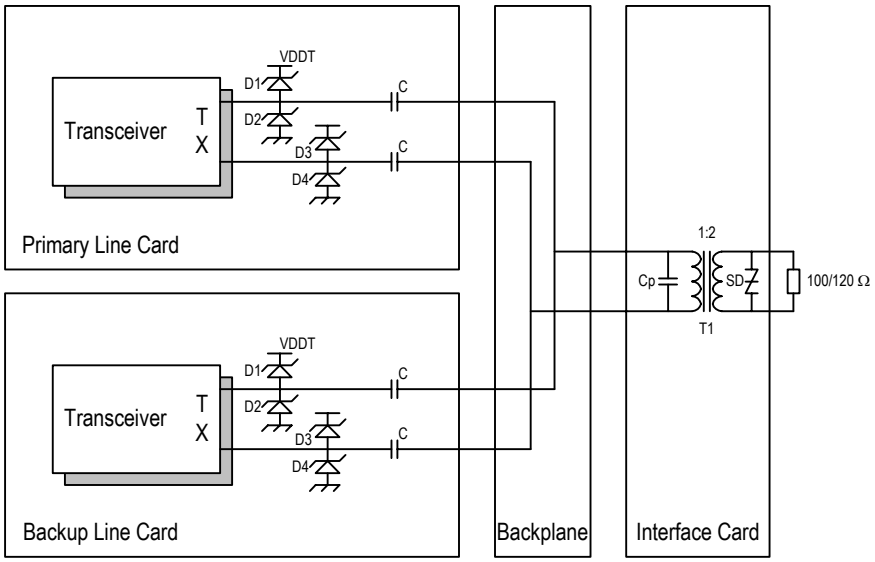

Figure 3. Transmit Line Interface Schematic

2 HOT-SWITCH AND HOT-SWAP

2.1 WHAT IS HOT-SWITCH

Hot-switch refers to the switching from an active card to a backup card or vice versa. The critical parameter in switching is the latency. GR253 and ITU-T G.783 require the total latency of less than 60 ms. The IDT82P2281/2/4/8 incurs a latency of no more than 10 µs during hot-switch. This gives the Transceiver over 100 times of the required margin for system implementation.

The IDT82P2281/2/4/8 provides both hardware and software modes for hot-switch: In hardware mode, switching the THZ pin high or low will put the device into high-impedance or active mode respectively. In software mode, writing a 1 or 0 to the THZ bit in the TCF1 register will put the output driver to high-impedance or active mode respectively. Lab tests show that there is less than 1 bit error for every 20 hot-switches using the THZ pin.

2.2 WHAT IS HOT-SWAP

Hot-swap refers to the plugging and unplugging of line cards in a powered backplane. When a card fails, a new replacement card is installed. The failed card must be removed and a new card is plugged in while the system is still running. The IDT82P2281/2/4/8 provides high transmit and receive impedance to enable hot-swap while still maintaining excellent transmit output pulse templates and producing no bit error. It should be noted that to ensure good system performance, the pins plugged into the backplane should be staggered as follows:

- Ground pins are the first to make contact (longer pin);
- VCC pins are the next to make contact;
- TTIP/TRING, RTIP/RRING and I/O pins are the last to make contact.

3 GENERAL DESIGN GUIDELINES

- Surge immunity protection should be placed close to the connector, where the source of disturbance is.
- Power supply decoupling caps should be placed as close to the power and ground pins of the chip as possible.
- simple inductor or beads and capacitors filter is recommended for power supply switching noise isolation.
- Route digital signals away from the analog signals to avoid them from crossing each other.
- Avoid power and ground planes near high voltage area as noise from high voltage area may couple noise to the power/ground planes. (Recommend to void power and ground planes underneath the RJ48 or BNC connectors).
- EMI filtering should currently be sufficient. However, if additional EMI requirement has to be met, common mode choke may be added near the connectors.
- Avoid long trace as they may reduce the transmit output amplitude. For T1/E1/J1 type of signals, less than 30 cm is recommended.

4 RESET REQUIREMENT

After power up, the device must be reset before operation. However, the master clock must be available during reset.

Table 3 lists the time in which reset is completed in different cases.

Table 3: Reset Completed Time

Different Cases	Completed Time (ms)
Hardware reset after power up.	12
Hardware reset during normal operation.	2
Software reset after mode setting change.	2

5 TEST RESULT

5.1 SUMMARY OF IDT82P2288 HPS TEST RESULT

Table 4 summarizes the test result conducted by IDT Telecom Laboratory. The 1+1 Relay-less HPS was tested using a modified IDT82P2288 octal Transceiver evaluation board. In addition to bit error rate, pulse templates, and return loss tests, additional tests to mimic hot-switch and hot-swap conditions are also performed.

Table 4: HPS Performance Test Result

#	Test	Result	Description
1	T1/E1 Power Failure Test	0 bit error / 48 hours	2^23-1 PRBS, ESF for T1 2^23-1 PRBS, PCM32CRC for E1 Primary card transmits live traffic Secondary powered on/off Duration = 48 hr Test configuration: Test setup #1
2	T1/E1 Hot-Switch Stress Test	< 1 error for every 20 switches	2^23-1 PRBS, ESF for T1 2^23-1 PRBS, PCM32CRC for E1 Switch data between primary and secondary card Duration = 8 hr Test configuration: Test setup #2

5.2 T1/E1 TRANSMIT PULSE MASKS

Figure 4 ~ Figure 7 show the captured T1 and E1 pulse masks meeting T1.102 and G.703 templates. Although only 0 ft waveforms are shown, the IDT82P2281/2/4/8 passed all pulse templates LBO. User can verify the other LBO by setting bits PULSE[3:0] of register TCF1.

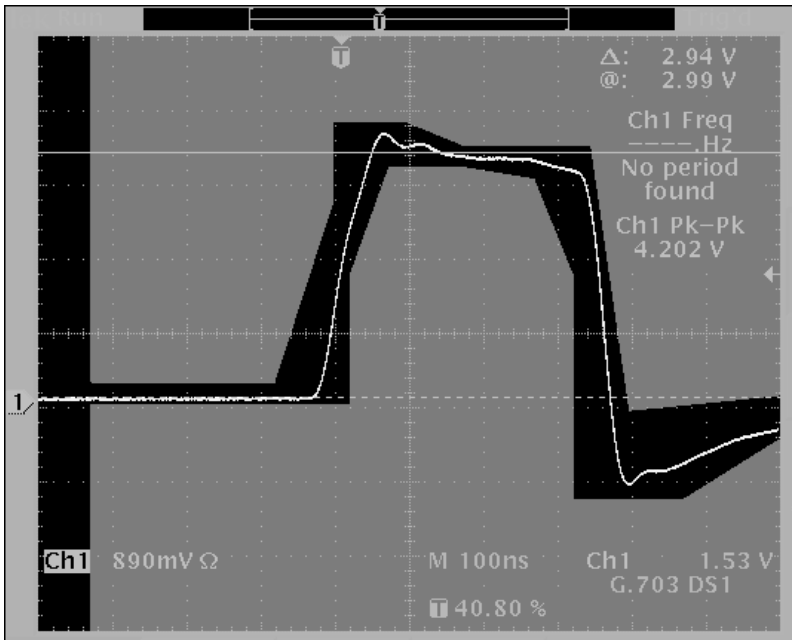

Figure 4. T1 Pulse Mask - Primary Card Transmits, Secondary Card in Stand By, for Test Setup #2

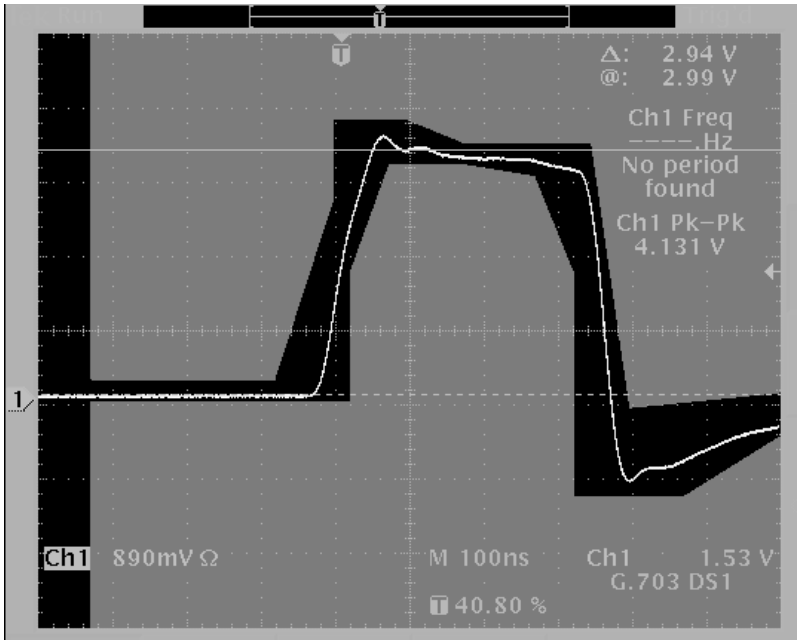

Figure 5. T1 Pulse Mask - Primary Card Transmits, Secondary Card in Stand By, for Test Setup #1

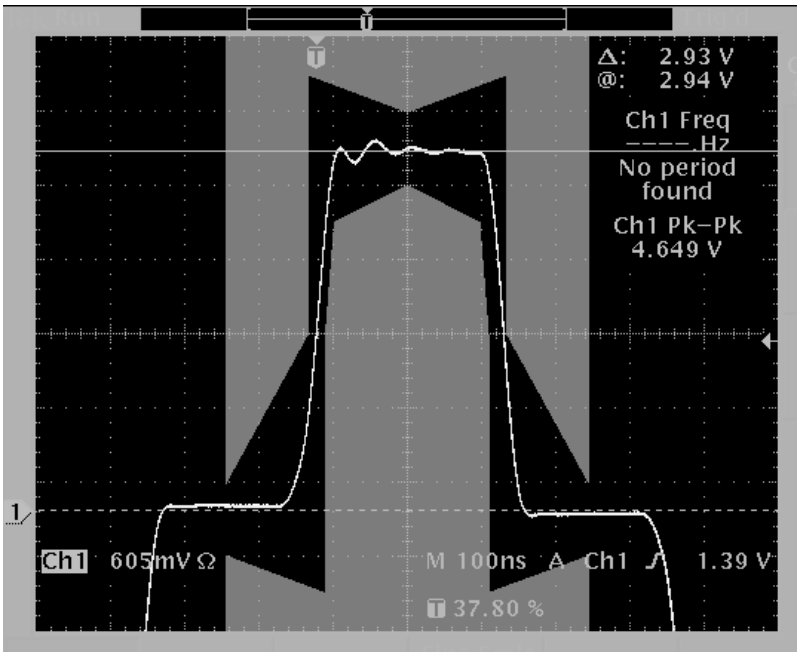

Figure 6. E1 Pulse Mask - Primary Card Transmits, Secondary Card in Stand By, for Test Setup #2

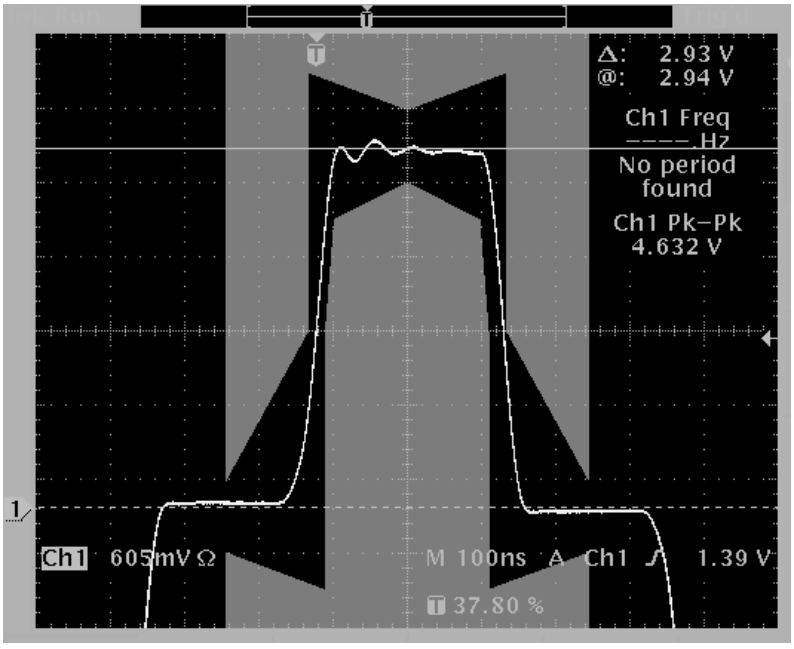

Figure 7. E1 Pulse Mask - Primary Card Transmits, Secondary Card in Stand By, for Test Setup #1

5.3 RECEIVE RETURN LOSS

Table 5: E1 / 120 Ω (Impedance - Internal Mode, Rr = 120 Ω)

Frequency (KHz)	51	90	102	1000	1024	2000	2048	2500	3000
RL (dB), Dual Board	-27.098	-28.256	-28.657	-27.134	-24.607	-24.324	-24.613	-28.741	-29.596
RL (dB), Single Board	-27.192	-28.749	-28.61	-27.532	-27.634	-27.233	-27.471	-37.215	-40.202

5.4 TRANSMIT RETURN LOSS

Table 6: E1 / 120 Ω (Impedance - Internal Mode, Cp = 560 pF)

Frequency (KHz)	51	90	102	1000	1024	2000	2048	2500	3000
Device A	-15.494	-19.736	-20.338	-22.269	-22.383	-18.591	-18.336	-16.728	-15.164
Device B	-15.983	-20.678	-21.766	-25.593	-25.64	-20.541	-20.076	-18.187	-16.279

5.5 TEST SETUP

Figure 8 ~ Figure 9 show the test setups of different HPS tests conducted by IDT Telecom Laboratory.

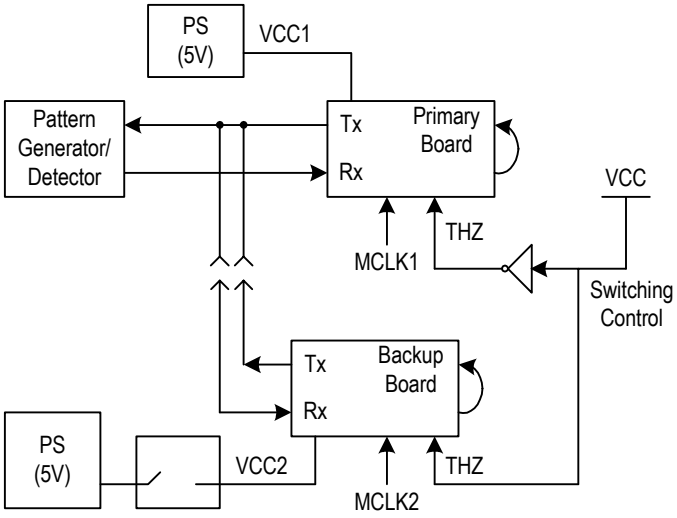

Figure 8. Test Setup #1 (Power Failure Test Setup)

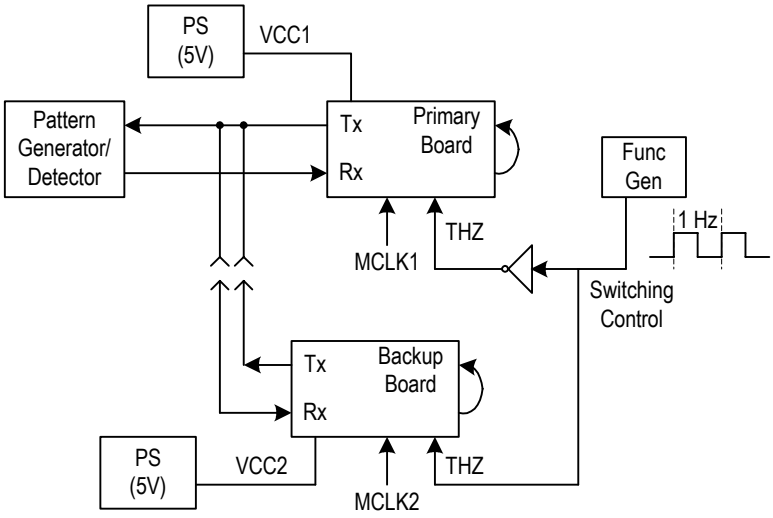

Figure 9. Test Setup #2 (Hot-Switch Test Setup)

6 CONCLUSION

The IDT82P2281/2/4/8 T1/E1/J1 Long Haul / Short Haul Transceivers are highly integrated Transceivers that enables 1+1 relay-less hitless protection. As shown by IDT laboratory test result, the integrated features maintain outstanding signal integrity in HPS application and provide excellent design margin to achieve high system availability, reliability and serviceability.

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