UNDERSTANDING THE SuperJET™ TRANSCEIVER SYSTEM INTERFACE 82P2281, 82P2282, 82P2284 AND 82P2288

Application Note AN-424

INTRODUCTION

The SuperJET system interface discussed in this document is based on IDT's 8 channel SuperJET transceiver (82P2288). These interface options are also applicable to the quad (82P2284), dual (82P2282) and single (82P2281) transceiver products. The SuperJET family of devices provides a wide variety of different modes on the system interface so that it can easily and gluelessly work with microprocessors, FPGAs, Time Slot Interchange Devices, Mappers, and other devices.

The purpose of this application note is to go over many of the different modes which the system interface can be programmed and the effect it has on the I/O direction, transmit edges, sample edges, clocks and signal priority.

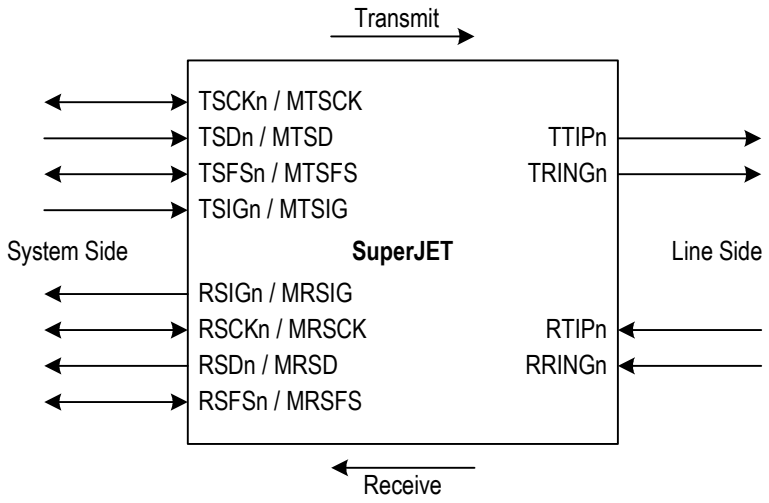


Figure 1. SuperJET Signal Names and Terminology

1 SYSTEM INTERFACE PIN SUMMARY

1.1 IN NON-MULTIPLEXED MODE

Refer to Table 1 for the receive system interface pin and Table 2 for the transmit system interface pin.

Table 1: Receive System Interface Pin Names in Non-Multiplexed Mode

Pin Name	Pin Description
RSDn	Receive Side System Data
RSIGn	Receive Side System Signaling
RSFSn	Receive Side System Frame Pulse
RSCKn	Receive Side System Clock

Table 2: Transmit System Interface Pin Names in Non-Multiplexed Mode

Pin Name	Pin Description
TSDn	Transmit Side System Data
TSIGn	Transmit Side System Signaling
TSFSn	Transmit Side System Frame Pulse
TSCKn	Transmit Side System Clock

1.2 IN MULTIPLEXED MODE

Refer to Table 3 for the receive system interface pin and Table 4 for the transmit system interface pin.

Table 3: Receive System Interface Pin Names in Multiplexed Mode

Pin Name	Pin Description
MRSD	Multiplexed Receive Side System Data
MRSIG	Multiplexed Receive Side System Signaling
MRSFS	Multiplexed Receive Side System Frame Pulse
MRSCK	Multiplexed Receive Side System Clock

Table 4: Transmit System Interface Pin Names in Multiplexed Mode

Pin Name	Pin Description
MTSD	Multiplexed Transmit Side System Data
MTSIG	Multiplexed Transmit Side System Signaling
MTSFS	Multiplexed Transmit Side System Frame Pulse
MTSCK	Multiplexed Transmit Side System Clock

2 BACKPLANE CLOCK MODE

The system interface can be set in Non-Multiplexed mode or Multiplexed mode.

In Non-Multiplexed mode, the system interface can work in Master mode (the system interface clock and frame pulse output from the device) or Slave mode (the system interface clock and frame pulse input to the device).

In Multiplexed mode, the system interface can only work in Slave mode.

Refer to Table 5 and Table 6 for the clock / data rate in different operation modes. The related registers configuration is listed in Table 7.

Table 5: System Interface Clock & Data Rate in E1 Mode

Operation Mode			Clock Rate	Data Rate
Non-Multiplexed	Master	Single Clock	2.048 MHz	2.048 MBit
	Slave	Single Clock	2.048 MHz	2.048 MBit
		Double Clock	4.096 MHz	2.048 MBit
Multiplexed	Slave	Single Clock	8.192 MHz	8.192 MBit
		Double Clock	16.384 MHz	8.192 MBit

Table 6: System Interface Clock & Data Rate in T1/J1 Mode

Operation Mode				Clock Rate	Data Rate
Non-Multiplexed	Master	T1 Mode T1 Rate	Single Clock	1.544 MHz	1.544 MBit
	Slave	T1 Mode T1 Rate	Single Clock	1.544 MHz	1.544 MBit
		T1 Mode E1 Rate	Single Clock	2.048 MHz	2.048 MBit
		T1 Mode E1 Rate	Double Clock	4.096 MHz	2.048 MBit
Multiplexed	Slave	T1 Mode E1 Rate	Single Clock	8.192 MHz	8.192 MBit
			Double Clock	16.384 MHz	16.384 MBit

Table 7: Related Registers Configuration

Operation	Configuration Registers	
	for Receive Path	for Transmit Path
Non-Multiplexed / Multiplexed mode selection	RMUX (b3, 10H)	TMUX (b0, 10H)
Master / Slave mode selection	RMODE (b0, X47H)	TMODE (b0, X43H)
Single / Double clock selection	CMS (b1, X46H)	CMS (b2, X42H)
T1 mode E1 rate mapping mode selection	MAP[1:0] (b2~1, X47H)	MAP[1:0] (b2~1, X43H)
Frame pulse active level selection	FSINV (b4, X48H)	FSINV (b1, X42H)

3 T1 TO E1 / E1 TO T1 MAPPING IN T1 MODE E1 RATE

There are three mapping modes:

- G.802 mode;
- One Filler Every Four Channels mode;
- Continuous Channels mode.

In Receive side, T1/J1 format will map to E1 format. See Figure 2 to Figure 4.

In Transmit side, E1 format will map to T1/J1 format. See Figure 5 to Figure 7.

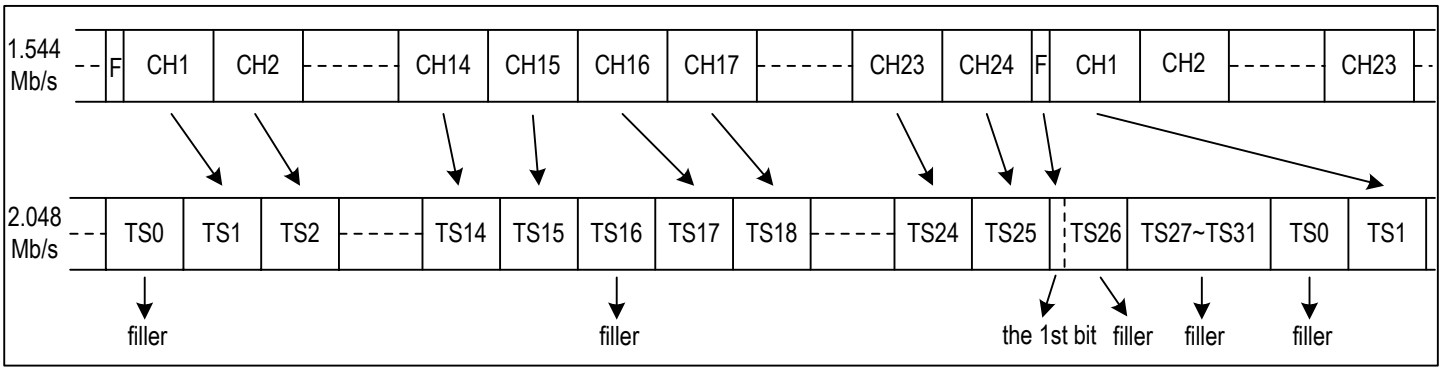


Figure 2. T1/J1 To E1 Format Mapping - G.802 Mode

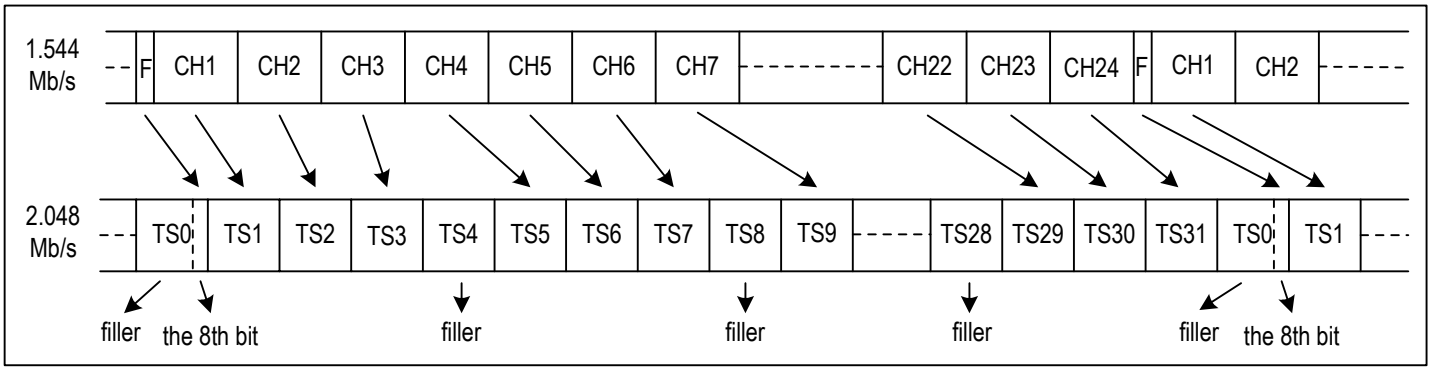


Figure 3. T1/J1 To E1 Format Mapping - One Filler Every Four Channels Mode

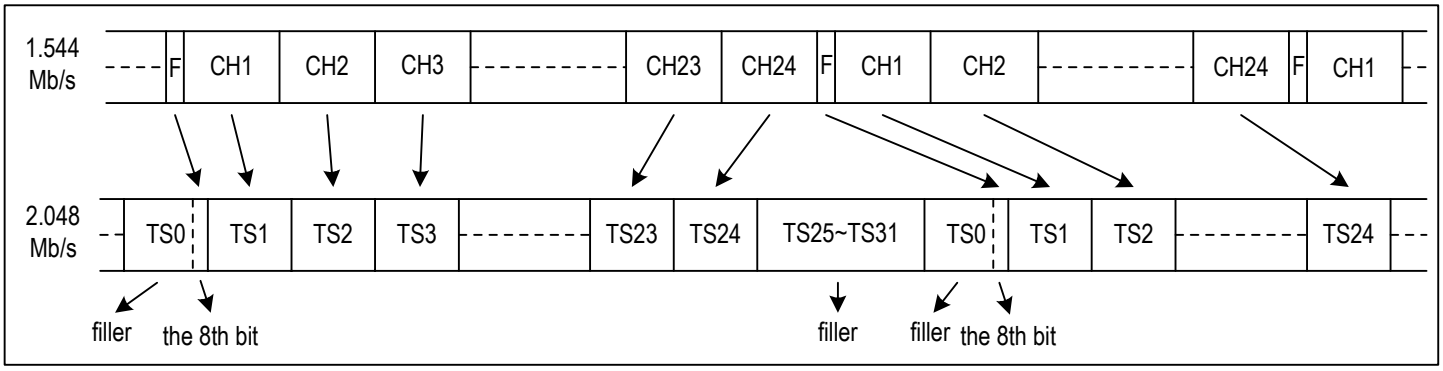


Figure 4. T1/J1 To E1 Format Mapping - Continuous Channels Mode

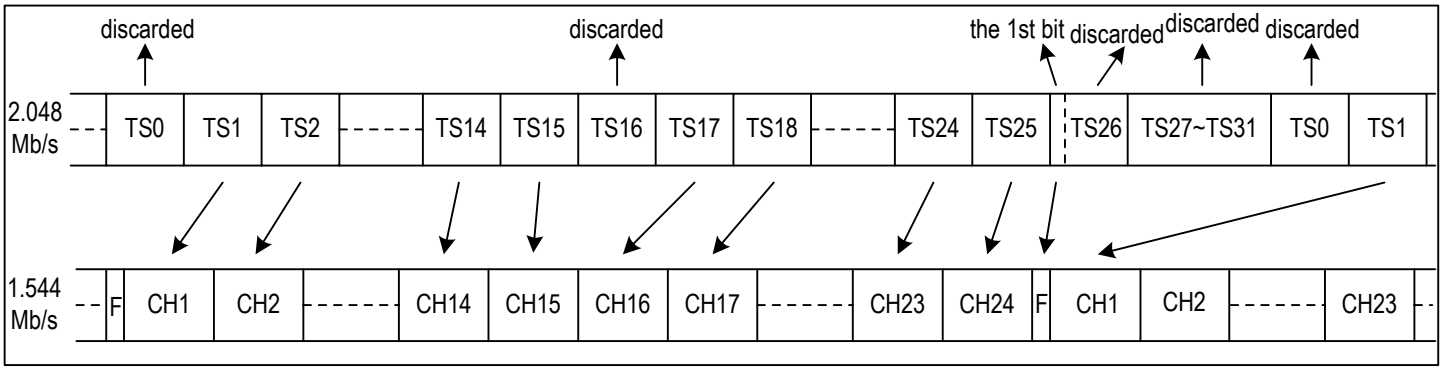


Figure 5. E1 To T1/J1 Format Mapping - G.802 Mode

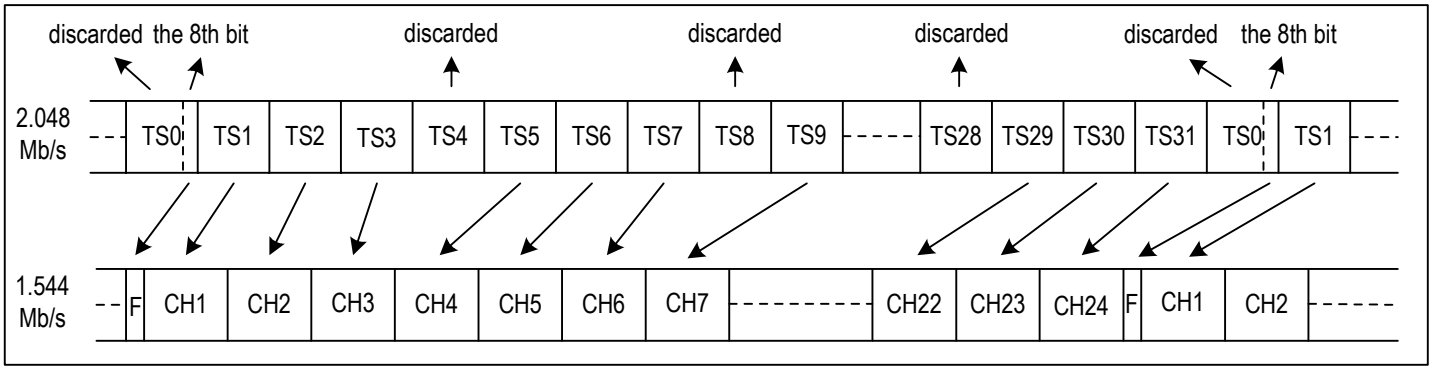


Figure 6. E1 To T1/J1 Format Mapping - One Filler Every Four Channels Mode

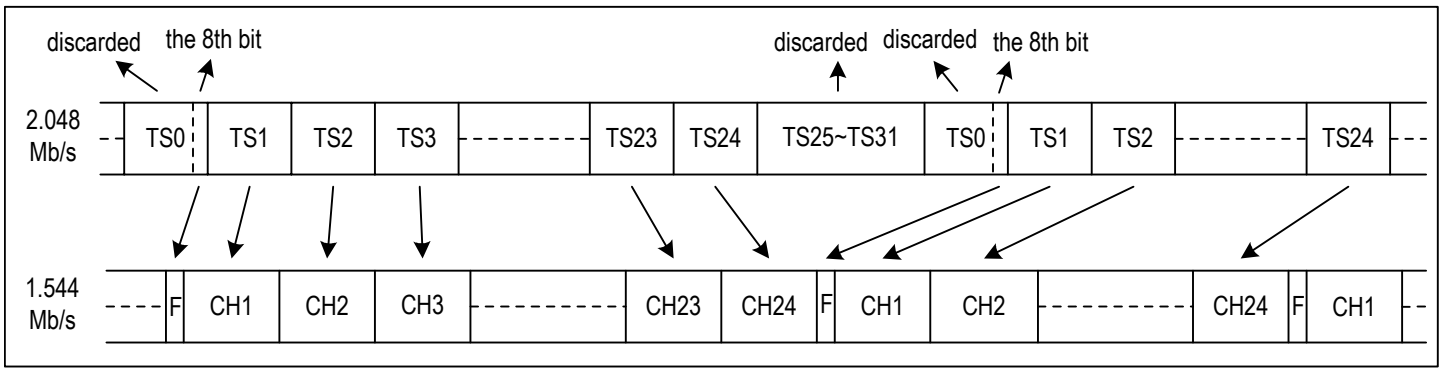


Figure 7. E1 To T1/J1 Format Mapping - Continuous Channels Mode

4 OPERATION OF SINGLE CLOCK MODE

4.1 CLOCK/DATA SAMPLE/UPDATE

The FE bit selects the active edge of (M)RSCKn/(M)TSCKn to update/sample the pulse on (M)RSFSn/(M)TSFSn. The DE bit selects the active edge of (M)RSCKn/(M)TSCKn to update/sample the data on (M)RSDn/(M)TSDn and (M)RSIGn/(M)TSIGn.

Figure 8 shows how to set FE and DE in Receive System Interface Slave mode. In this mode, RSCKn/MRSCK and RSFSn/MRSFS input clock and frame pulse from external, and RSDn/MRSD output data. If the RSCKn/MRSCK rising edge samples the RSFSn/MRSFS at middle, then set FE to '1'. If the RSCKn/MRSCK falling edge samples the RSFSn/MRSFS at middle, then set FE to '0'. If set DE to '1', the RSDn/MRSD will be updated after RSCKn/MRSCK rising edge. If set DE to '0', the RSDn/MRSD will be updated after RSCKn/MRSCK falling edge.

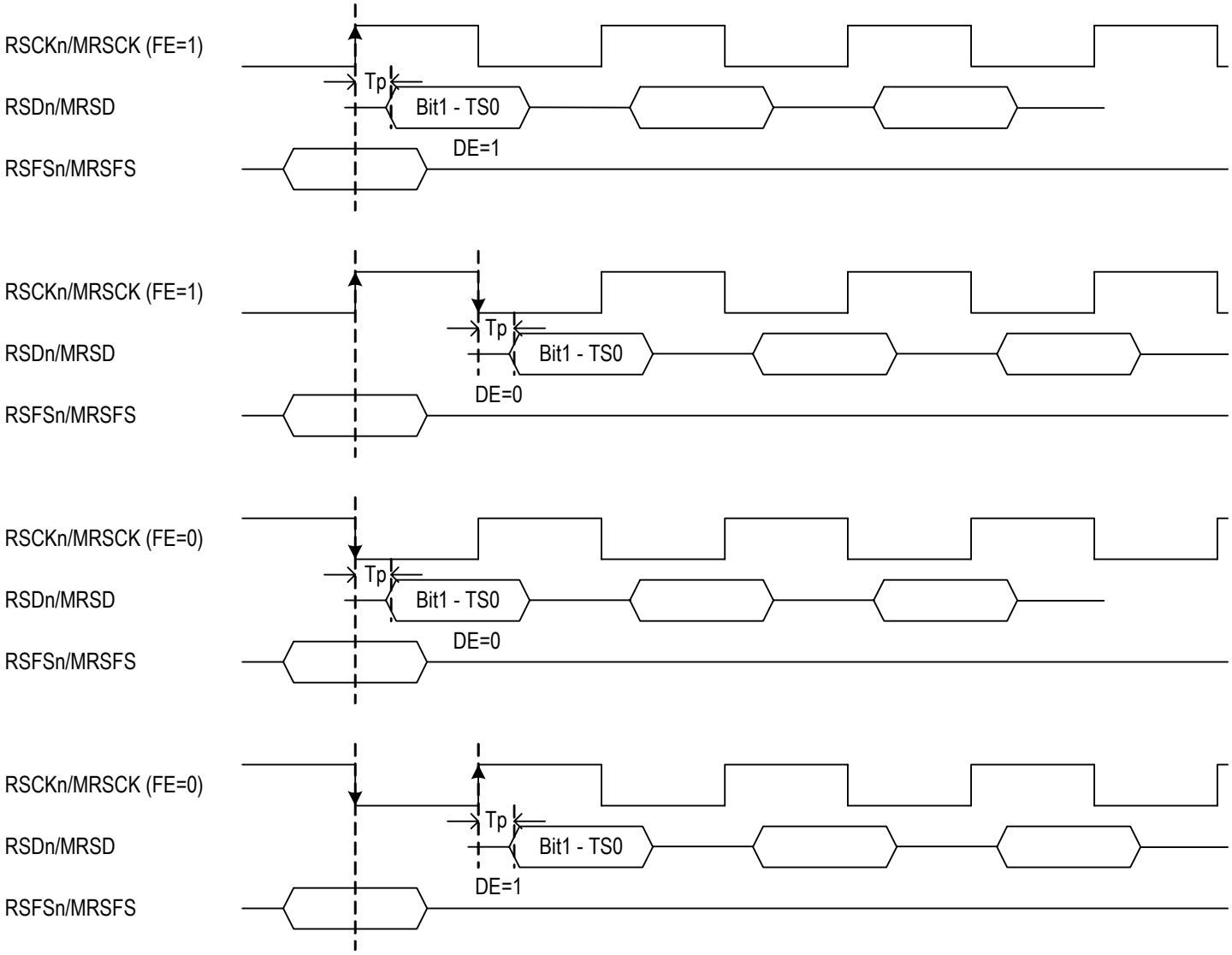


Figure 8. Receive Clock Slave Mode (Single Clock)

Figure 9 shows how to set FE and DE in Receive System Interface Master mode. In this mode, RSCKn and RSFSn output clock and frame pulse, and RSDn output data. If set FE to '1', RSFSn will be updated after RSCKn rising edge. If set FE to '0', RSFSn will be updated after RSCKn falling edge. If set DE to '1', RSDn will be updated after RSCKn rising edge. If set DE to '0', RSDn will be updated after RSCKn falling edge.

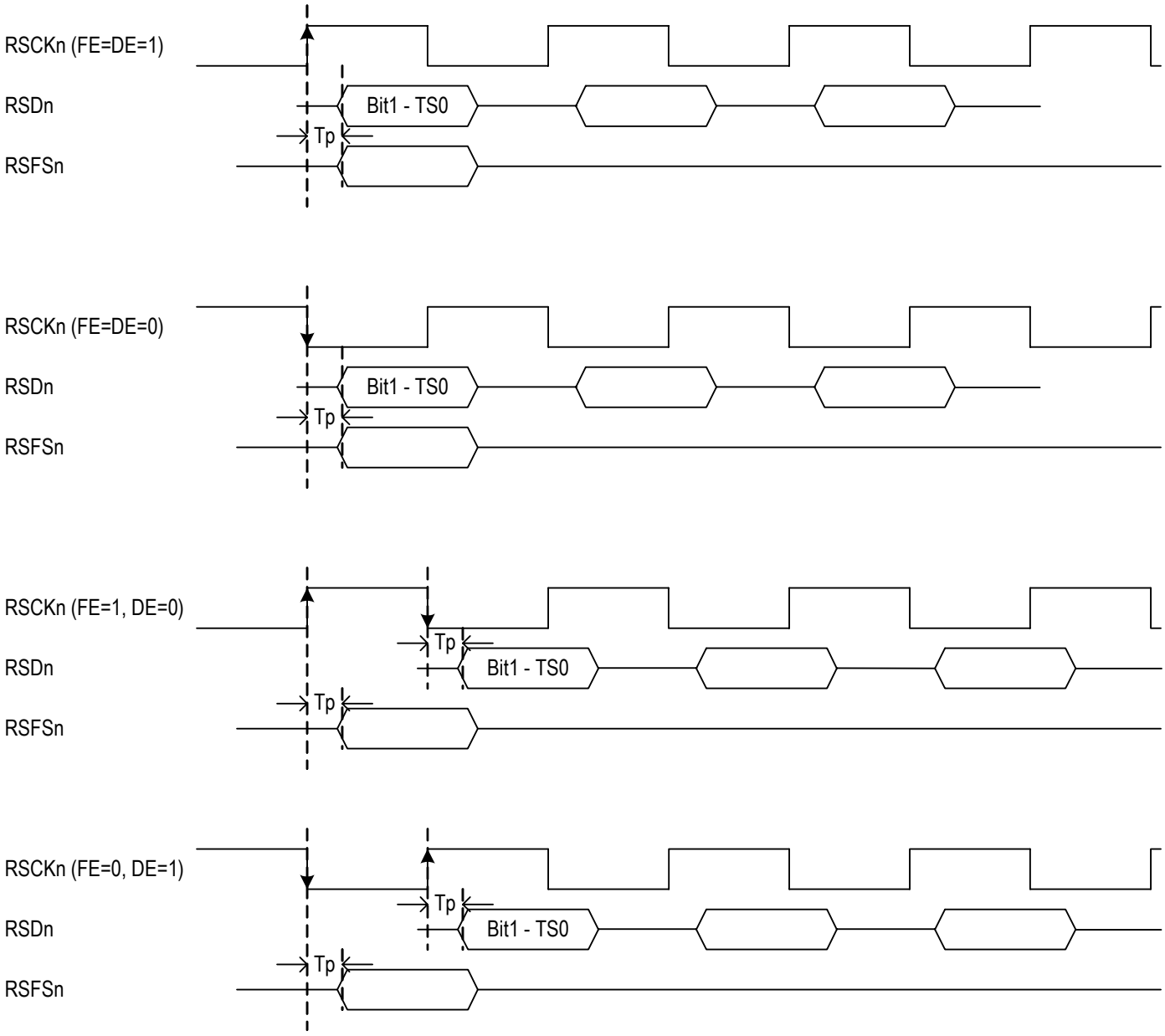


Figure 9. Receive Clock Master Mode (Single Clock)

Figure 10 shows how to set FE and DE in Transmit System Interface Slave mode. In this mode, TSCKn/MTSCK and TSFSn/MTSFS input clock and frame pulse from external, and TSDn/MTSD input data from external. If the TSCKn/MTSCK rising edge samples TFSn/MTSFS at middle, then set FE to '1'. If the TSCKn/MTSCK falling edge samples TSFSn/MTSFS at middle, then set FE to '0'. If the TSCKn/MTSCK rising edge samples TSDn/MTSD at middle, then set DE to '1'. If the TSCKn/MTSCK falling edge samples TSDn/MTSD at middle, then set DE to '0'.

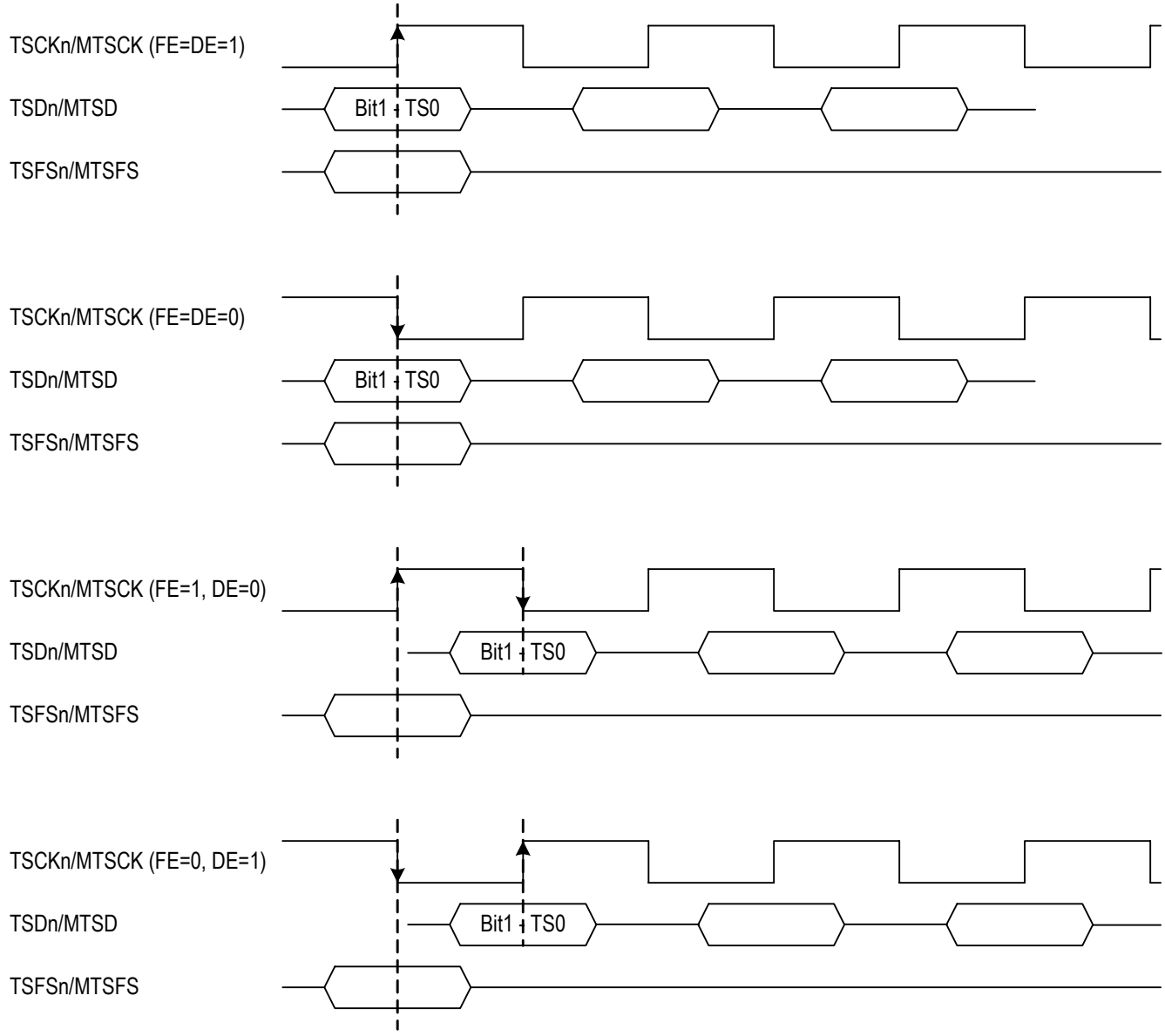


Figure 10. Transmit Clock Slave Mode (Single Clock)

Figure 11 shows how to set FE and DE bits in Transmit System Interface Master mode. In this mode, TSCKn and TSFSn output clock and frame pulse, and TSDn input data. If set FE to '1', TSFSn will be updated after TSCKn rising edge. If set FE to '0', TSFSn will be updated after TSCKn falling edge. If the TSCKn rising edge samples TSDn at middle, then set DE to '1'. If the TSCKn falling edge samples TSDn at middle, then set DE to '0'.

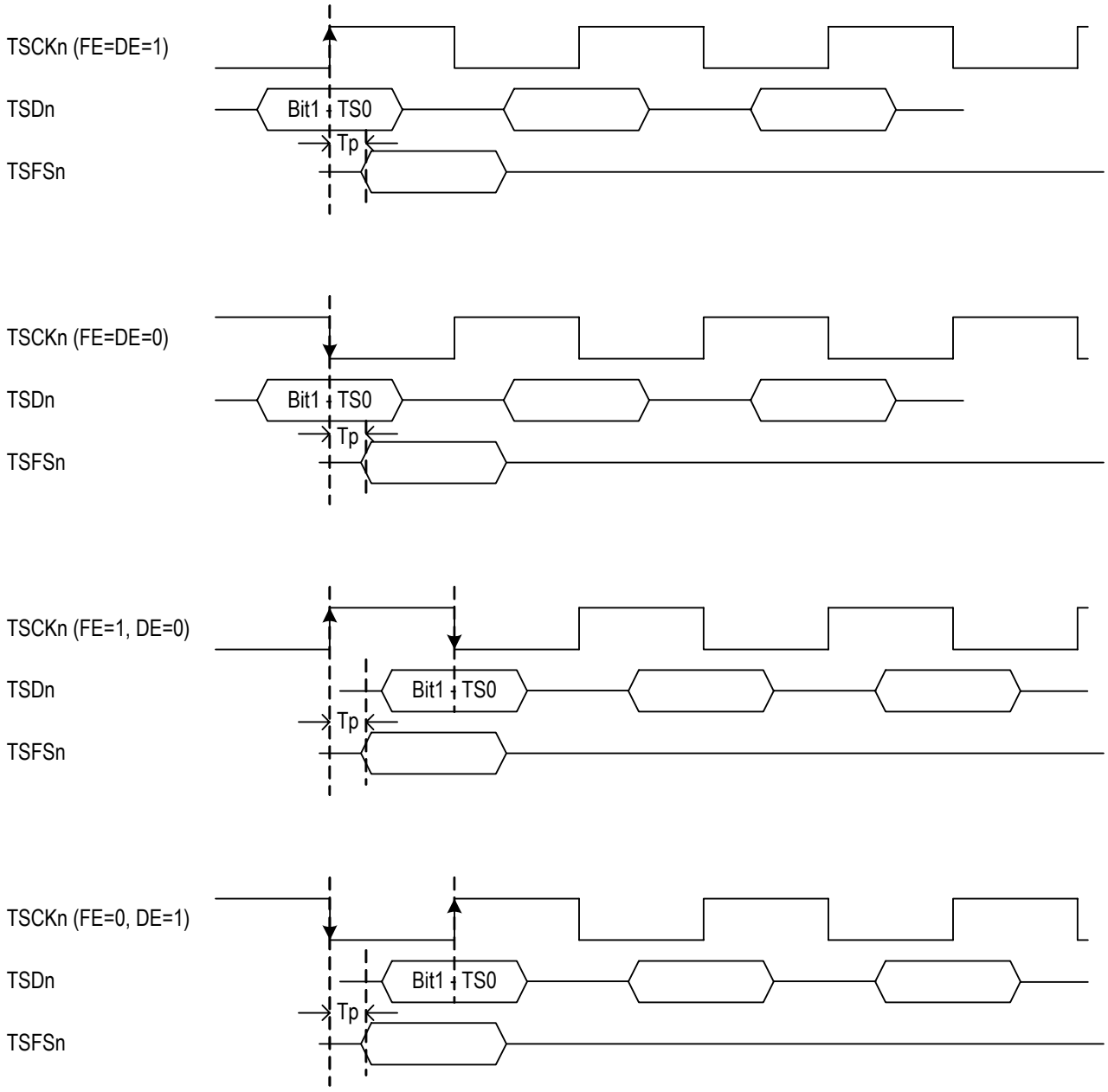


Figure 11. Transmit Clock Master Mode (Single Clock)

4.2 TIMESLOT/CHANNEL OFFSET & BIT OFFSET

Timeslot/channel offset and bit offset are both supported in all operation modes. Figure 12 and Figure 13 show some examples of TS/CH offset and bit offset in receive system interface.

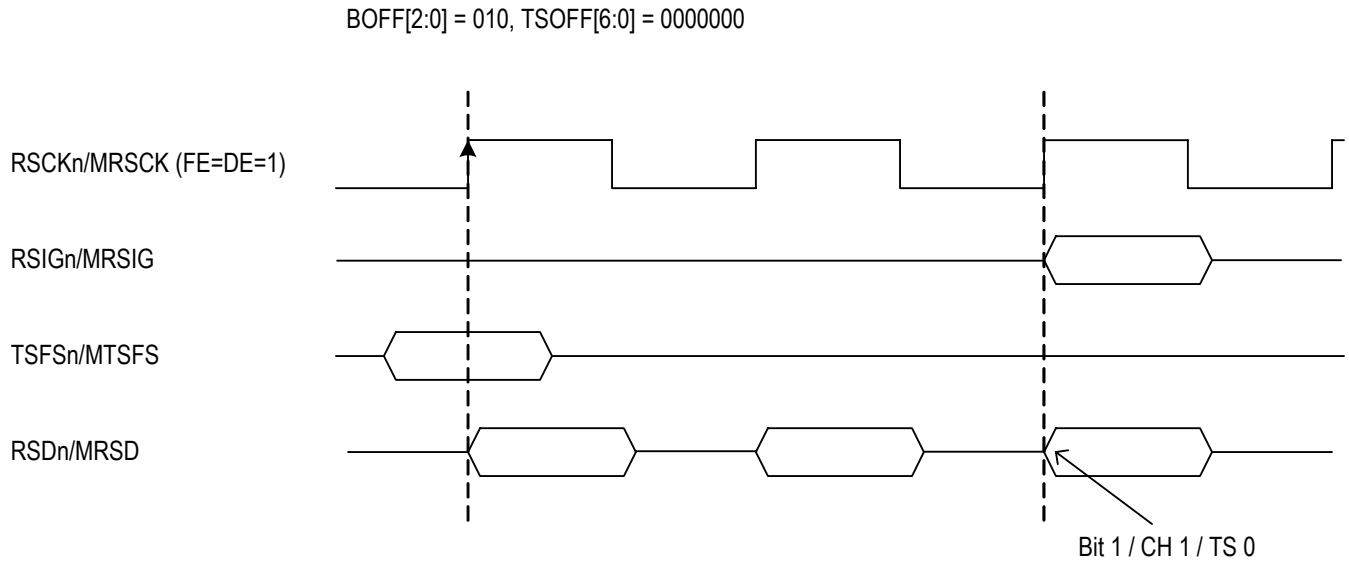


Figure 12. TS/CH Offset & Bit Offset - Example 1

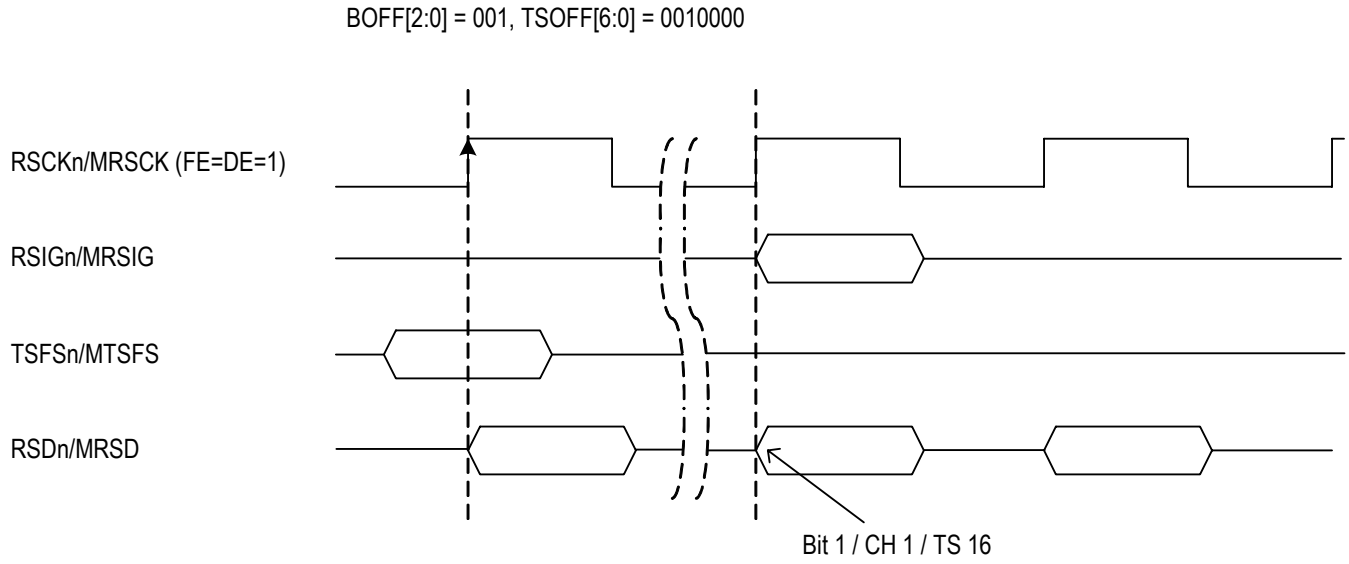


Figure 13. TS/CH Offset & Bit Offset - Example 2

In Multiplexed mode, the TS/CH offset of each link should be set to different value to avoid data conflict. For example:

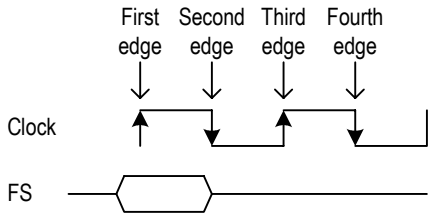
Set TSOFF of Link 1 to 0;
Set TSOFF of Link 2 to 1;
Set TSOFF of Link 3 to 2;
Set TSOFF of Link 4 to 3;
Set TSOFF of Link 5 to 0;
Set TSOFF of Link 6 to 1;
Set TSOFF of Link 7 to 2;
Set TSOFF of Link 8 to 3;

5 OPERATION OF DOUBLE CLOCK MODE

The SuperJET device can operate with either a single-bit / single-clock mode of operation or a single-bit / double-clock mode of operation. In the double clock mode of operation, the FE bit determines if the frame sync is sampled on the rising edge (FE = 1) or falling edge (FE = 0). Since each "bit cycle" now contains four edges the EDGE bit and DE bit together select one of the four edges to sample data.

Below are two drawings showing two possible frame selections and the data sample edges for those cycles. It should be noted that double clock mode is not supported in Master Mode or in the T1/J1 rate (1.544Mbps clock and data) in Slave Mode.

when FE = 1

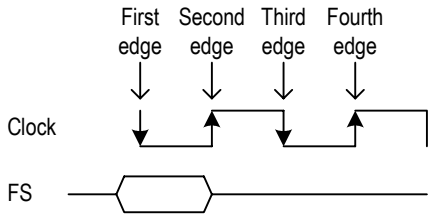


The data sample edge is:

Edge \ DE	0	1
0	2nd	1st
1	4th	3rd

Figure 14. Data Sample Edge When FE = 1

when FE = 0



The data sample edge is:

Edge \ DE	0	1
0	1st	2nd
1	3rd	4th

Figure 15. Data Sample Edge When FE = 0

Table 8: CMS in RBIF Operation (b1, X46H) & in TBIF Operation (b2, X42H)

CMS	RSCKn	MRSCK
0	2.048 MHz	8.192 MHz
1	4.096 MHz	16.384 MHz

Table 9: EDGE in RBIF Bit Offset (b3, X4AH) & in TBIF Option (b3, X45H)

EDGE Bit	Edge Selection of RSCKn / MRSCK
0	first active edge
1	second active edge

Table 10: Edge Selection Based on EDGE, FE & DE Bits

EDGE Bit	FE = DE	FE ≠ DE
0	1st Edge	2nd Edge
1	3rd Edge	4th Edge

6 SUPERJET ST-BUS® EXAMPLE

6.1 RECEIVE DIRECTION

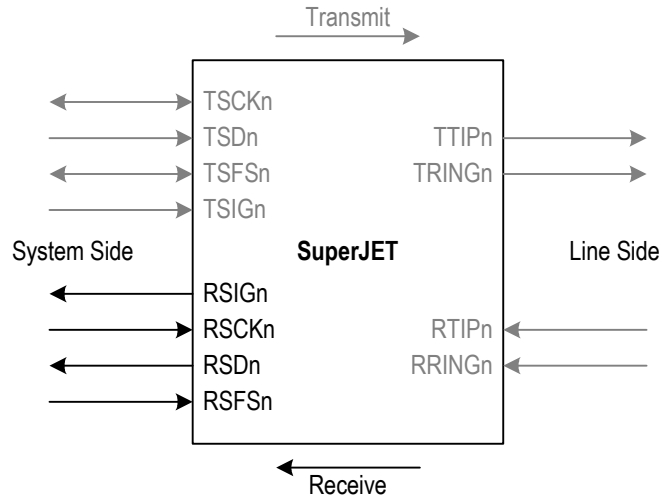


Figure 16. Receive Slave Mode

Table 11: Receive Slave & Multiplexed Modes

RSFSn / MRSFS	input to SuperJET
RSCKn / MRSCK	input to SuperJET
RSDn / MRSD	output from SuperJET

Frame pulse is sampled on the falling edge of clock, so:
FE (b2, X46H) = 0;
Frame pulse active state is low, so:
FSINV (b4, X48H) = 1;
Data is transmitted on the falling clock edge, so:
DE (b3, X46H) = 0;
So for ST-BUS® we want double clock, so:
Data needs to be updated on the first active edge, so:
EDGE (b3, X4AH) = 0;
CMS (b1, X46H) = 1;
RSCKn = 4.096 MHz;
MRSCK = 16.384 MHz.
Summary:
FE (b2, X46H) = 0;
FSINV (b4, X48H) = 1;
DE (b3, X46H) = 0;
EDGE (b3, X4AH) = 0;
CMS (b1, X46H) = 1.

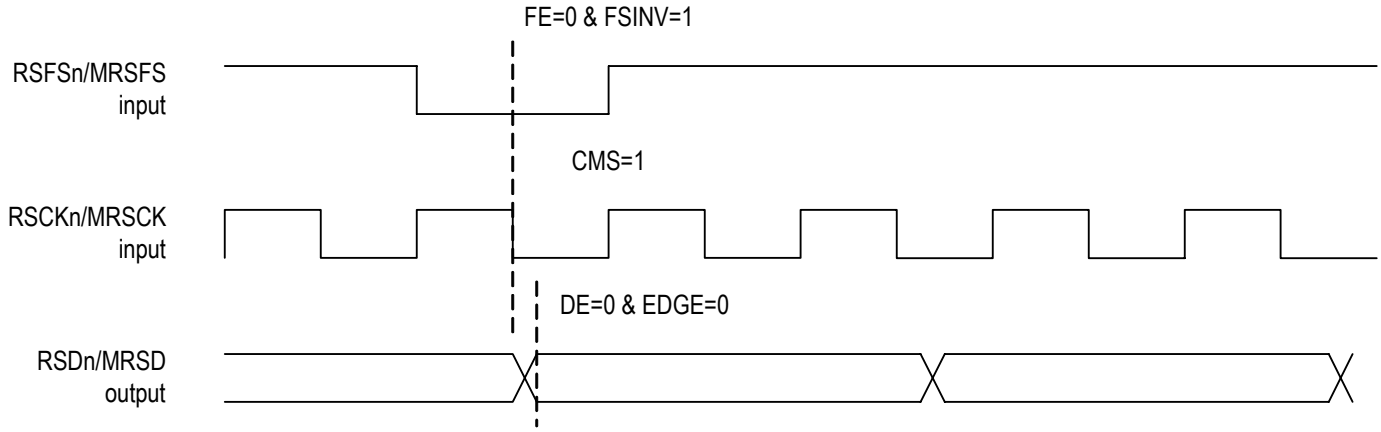


Figure 17. ST-BUS® Receive Timing aka System Side RX

6.2 TRANSMIT DIRECTION

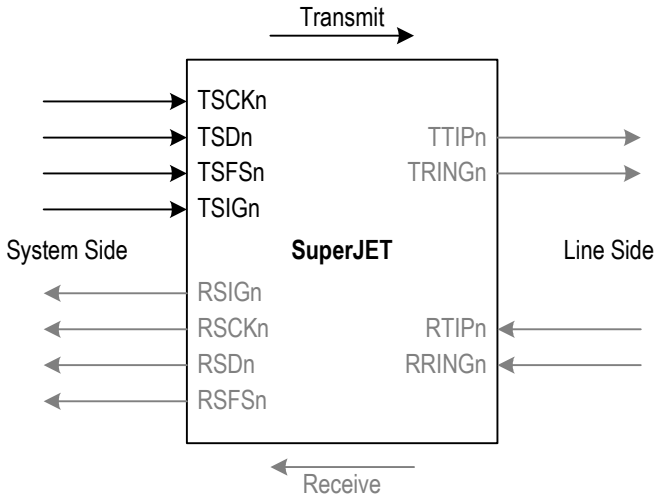


Figure 18. Transmit Slave Mode

Table 12: Transmit Slave & Multiplexed Modes

TSFSn / MTSFS	input to SuperJET
TSCKn / MTSCK	input to SuperJET
TSDn / MTSD	input to SuperJET

Frame pulse is sampled on the falling edge of clock, so:
FE (b3, X42H) = 0;
Frame pulse active state is low, so:
FSINV (b1, X42H) = 1;
Data is sampled on the rising clock edge, so:
DE (b4, X42H) = 1;
So for ST-BUS® we want double clock, so:
Data needs to be updated on the second active edge, so:
EDGE (b3, X45H) = 0;
CMS (b2, X42H) = 1;
TSCKn = 4.096 MHz;
MTSCK = 16.384 MHz.
Summary:
FE (b3, X42H) = 0;
FSINV (b1, X42H) = 1;
DE (b4, X42H) = 1;
EDGE (b3, X45H) = 0;
CMS (b2, X42H) = 1.

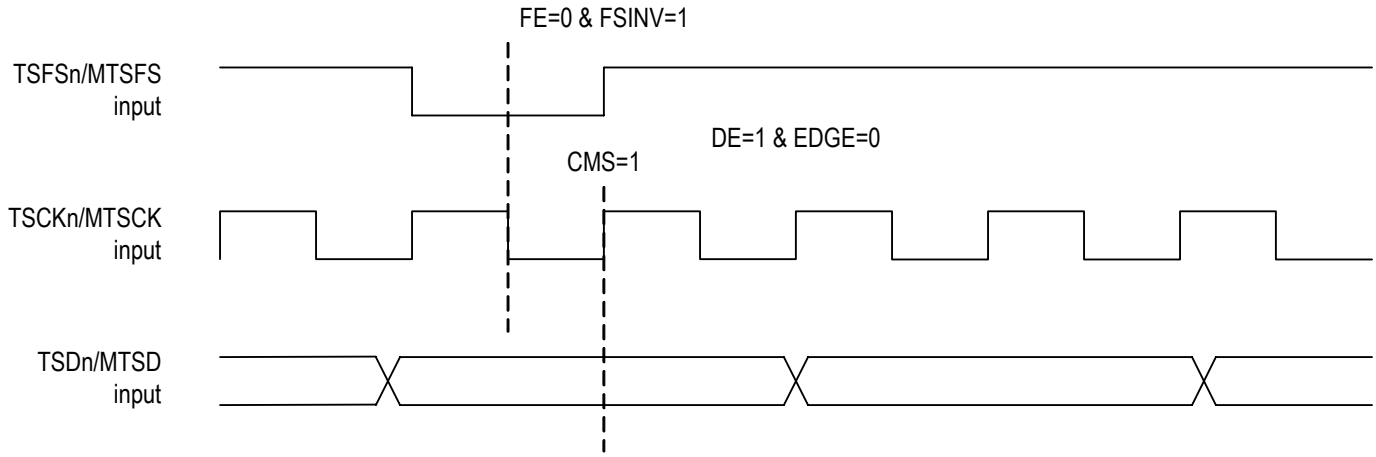


Figure 19. ST-BUS® Transmit Timing aka System Side TX

7 SUPETJET GCI EXAMPLE

7.1 RECEIVE DIRECTION

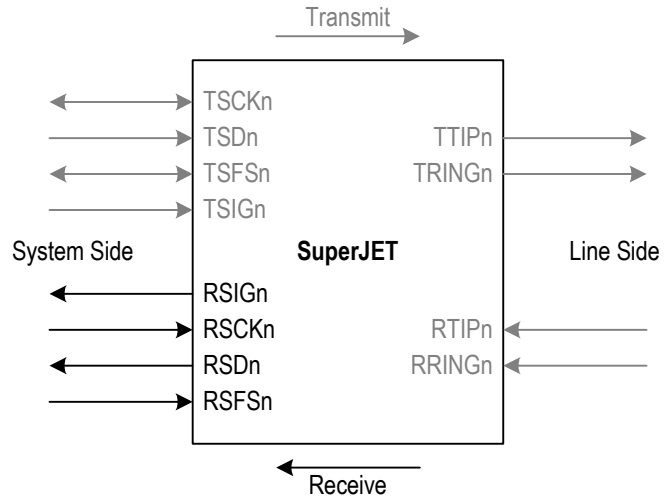


Figure 20. Receive Slave Mode

Table 13: Receive Slave & Multiplexed Modes

RSFSn / MRSFS	input to SuperJET
RSCKn / MRSCK	input to SuperJET
RSDn / MRSD	output from SuperJET

Frame pulse is sampled on the falling edge of clock, so:
FE (b2, X46H) = 0;
Frame pulse active state is high, so:
FSINV (b4, X48H) = 0;
Data is transmitted on the falling clock edge, so:
DE (b3, X46H) = 0;
So for GCI we want double clock, so:
Data needs to be sampled on the first active edge, so:
EDGE (b3, X4AH) = 0;
CMS (b1, X46H) = 1;
RSCKn = 4.096 MHz;
MRSCK = 16.384 MHz.
Summary:
FE (b2, X46H) = 0;
FSINV (b4, X48H) = 0;
DE (b3, X46H) = 0;
EDGE (b3, X4AH) = 0;
CMS (b1, X46H) = 1.

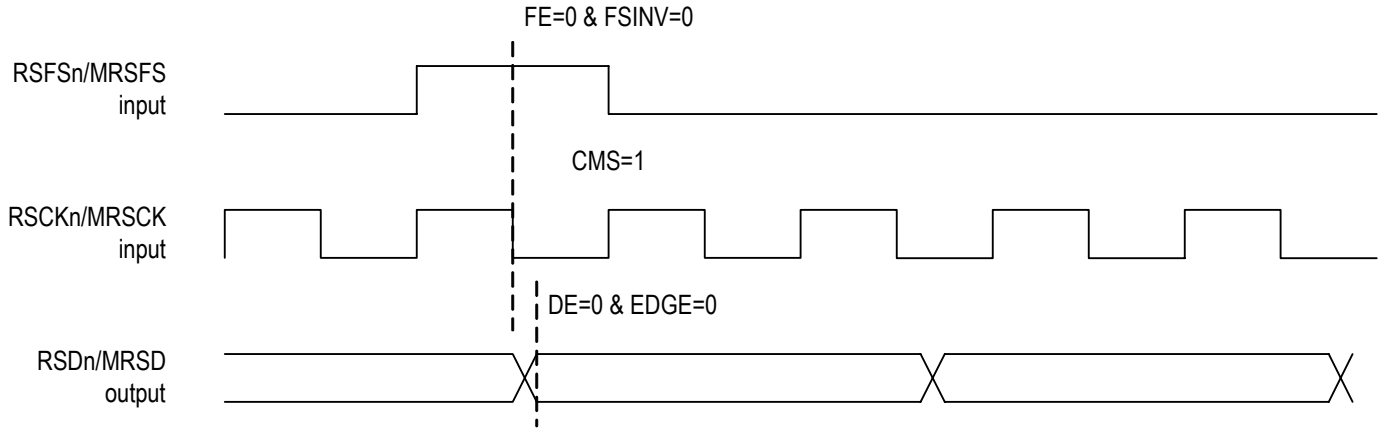


Figure 21. Receive Timing aka System Side RX

7.2 TRANSMIT DIRECTION

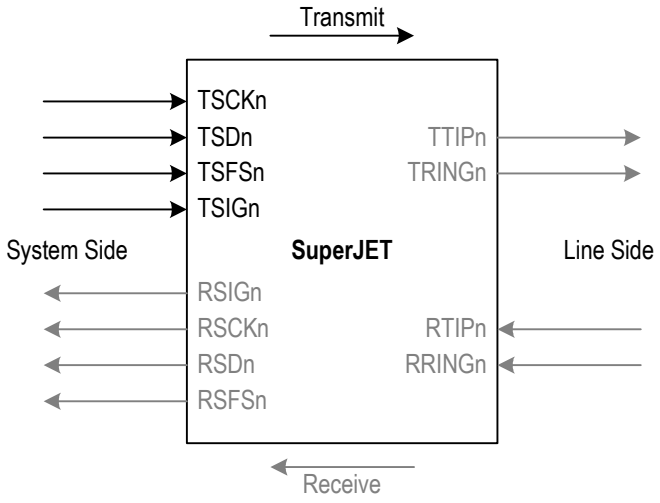


Figure 22. Transmit Slave Mode

Table 14: Transmit Slave & Multiplexed Modes

TSFSn / MTSFS	input to SuperJET
TSCKn / MTSCK	input to SuperJET
TSDn / MTSD	input to SuperJET

Frame pulse is sampled on the falling edge of clock, so:
FE (b3, X42H) = 0;
Frame pulse active state is high, so:
FSINV (b1, X42H) = 0;
Data is sampled on the falling clock edge, so:
DE (b4, X42H) = 0;
So for GCI we want double clock, so:
Data needs to be sampled on the second active edge, so:
EDGE (b3, X45H) = 1;
CMS (b2, X42H) = 1;
TSCKn = 4.096 MHz;
MTSCK = 16.384 MHz.
Summary:
FE (b3, X42H) = 0;
FSINV (b1, X42H) = 0;
DE (b4, X42H) = 0;
EDGE (b3, X45H) = 1;
CMS (b2, X42H) = 1.

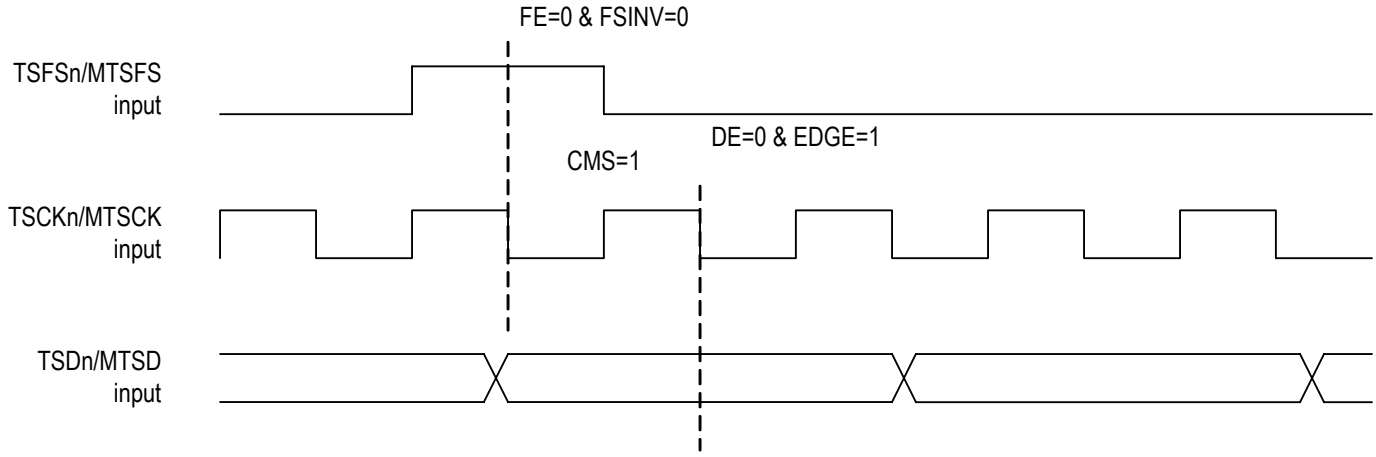


Figure 23. GCI Transmit Timing aka System Side TX

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