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1. Introduction

This application note discusses how to use an IDT 82P228x Transceiver in BITS/SSU applications. In this document, 82P228x refers to the 82P2281, 82P2282, 82P2284, and 82P2288. Building-Integrated Timing Supply (BITS) refers to a type of clock that is used extensively in network synchronization. It is a master timing supply for all deployed equipment within a network requiring synchronization. The term BITS is used in North America; outside of North America, this type of clock is referred to as a Synchronization Supply Unit (SSU).

There are two specifications in the ITU-G.703 standard for T1/E1 BITS applications: the normal T1/J1/E1 operation mode (chapters 5 and 9 in the standard) and the operation mode specified in chapter 13 of the standard. These two modes of operation are introduced in the following sections of this document.

Recommendation: Read the datasheet for the specific 82P228x product before using this application note.

2. OSCI Clock

In BITS applications, the crystal oscillator input (OSCI pin) clock accuracy should be within ± (10 to 100 ppm).

3. Normal T1/E1 Mode Operation

In normal T1/E1 operation, the BITS/SSU clock is recovered from a T1/E1 trunk and outputs on the REFA_OUT pin. At the same time, Synchronization Status Messages (SSM) can also be extracted from the same trunk. If transmission of a BITS/SSU clock is required on a T1/E1 trunk, this clock should be fed to the TSCK pin. An SSM code could be also inserted into the same trunk.

3.1 Configuration of the 82P228x Registers

All 82P228x registers have a default value after power up. Some registers must be re-configured for normal T1/E1 operation as specified in Table 1.

Table 1. Configuration for BITS/SSU in Normal T1/E1 Mode Operation

<table>
<tr><th>Operation</th><th>Register</th><th>Value</th><th>Definitions</th></tr>
<tr><td>Write</td><td>0x020</td><td>(See the next column for options)</td><td>
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0x00</td><td>E1 Mode</td></tr>
<tr><td>0x01</td><td>T1 SF</td></tr>
<tr><td>0x03</td><td>T1 ESF</td></tr>
</table>
</td></tr>
<tr><td>Write</td><td>0x023</td><td>(See the next column for options)</td><td>
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0x00</td><td>2.048M, 75Ω</td></tr>
<tr><td>0x01</td><td>2.048M, 120Ω</td></tr>
<tr><td>0x02</td><td>1.544M, 0 to 133 ft</td></tr>
</table>
</td></tr>
</table>

<table>
<tr><th>Operation</th><th>Register</th><th>Value</th><th>Definitions</th></tr>
<tr><td>Write</td><td>0x032</td><td>(See the next column for options)</td><td>
<table>
<tr><th>Value</th><th>Definition</th></tr>
<tr><td>0x00</td><td>75Ω</td></tr>
<tr><td>0x09</td><td>120Ω</td></tr>
<tr><td>0x12</td><td>100Ω</td></tr>
<tr><td>0x1B</td><td>110Ω</td></tr>
</table>
</td></tr>
<tr><td>Write</td><td>0x046</td><td>0x0C</td><td>Enable receive system side output</td></tr>
<tr><td>Write</td><td>0x047</td><td>0x00</td><td>Receive system side master clock mode</td></tr>
<tr><td>Write</td><td>0x03E</td><td>0x01</td><td>The REFA_OUT pin outputs a high level in the loss-of signal (LOS) condition</td></tr>
</table>

3.2 SSM Insertion and Extraction

In BITS applications, in addition to timing, the incoming line can carry Synchronization Status Messages (SSM). These messages, which are defined in various standards (see Table 2 and Table 5), indicate the quality level of the incoming clock. Messages (in code words) are transmitted and/or received through the data link bits (DS1 ESF formats) in T1 Mode or the Sa bits in time slot 0 of the E1 format. These code words in T1 and E1 operations are shown in Table 2 and Table 5, respectively.

Table 2. SSM Code Word in T1/J1 Mode (ESF Frame Format)

Quality Level	Description	FDL Code Word (DS1 ESF)
1	Stratum 1 traceable	0 ***000010*** 0 11111111
2	Synchronized traceability unknown	0 ***000100*** 0 11111111
3	Stratum 2 traceable	0 ***000110*** 0 11111111
4	Stratum 3 traceable	0 ***001000*** 0 11111111
5	SONET minimum clock traceable	0 ***010001*** 0 11111111
6	Stratum 4 traceable	0 ***010100*** 0 11111111
7	Do not use for synchronization	0 ***011000*** 0 11111111
User Assignable	Reserved for network synchronization use	0 ***100000*** 0 11111111

3.2.1 Bit-Oriented Message for T1/J1 Mode

IDT transceivers include the Bit-Oriented Message (BOM) feature for transmission and reception. The BOM pattern is “111111110xxxxxx0” which occupies the DL bits of F-bit positions in the ESF frame format. In the BOM pattern, each of the six “x” positions represents a bit in a 6-bit code.

In the receive direction, when a complete code is received, BOC[5:0] will store the received code. Every time that the BOC[5:0] bits are updated, it will be indicated by the BOCI bit.

In the transmit direction, 6-bit code words can be transmitted through the DL bit of the T1 ESF F-bit positions. XBOC[5:0] contains the 6-bit code in the BOM pattern described above. The BOM pattern is transmitted only if the XBOC[5:0] bits are not all ones.

3.2.1.1 Register Configurations for BITS/SSU in T1/J1 Mode

Table 3. Configuration for BITS/SSU in T1/J1 Mode

Operation	Register	Value	Definitions
Write	0x020	0x03	T1 ESF
Write	0x023	0x02	T1 ESF, 0 to 133 ft
Write	0x032	0x12	100Ω
Write	0x046	0x0C	Enable receive system side output
Write	0x047	0x00	Receive system side master clock mode
Write	0x03E	0x01	REFA_OUT pin outputs high level in the event of an LOS condition

Table 4. SSM Code Transmission and Reception for T1/J1 Mode

Operation	Register	Value	Definitions
SSM Code Transmission			
Write	0x080	0x08	0x08 = Stratum3 traceable
SSM Code Extraction			
Write	0x081	0x01	Interrupt enable
Read	0x082		BOCI bit[0] = 1 indicates the new SSM code has been received; write '1' to this bit to clear the interrupt indication for the next extraction
Read	0x083		Read the SSM code

The user can use the interrupt of the 82P228x to obtain the SSM code. The $\overline{INT}$ pin must be connected to the controller for this purpose. The steps to use in the T1/J1 Mode are as follows:

1. Set the BOCE bit (register 0x081, bit 0) to high to enable the interrupt on the $\overline{INT}$ pin.
2. The controller waits for the interrupt.
3. If the interrupt is detected by the controller, read the 0x082 register.
4. Check the BOCI bit (register 0x082, bit 0). If this bit is 1, the 82P228x has received the new SSM code.
5. Write '1' to the BOCI bit to clear the bit.
6. Read the 0x083 register. This register contains the value of the received SSM code.
7. Repeat steps 2 through 6.

3.2.2 SSM Transmission and Receive in the E1 Mode

In the E1 frame format, NFAS frames contain Sa[8:4] bits in time slot 0 (TS0). One of the Sa bits can be used to carry the code word (transmission and reception). In the 82P228x transceiver, the E1 Sa4 code word register is a 4-bit (Sa41, Sa42, Sa43, Sa44) code word that holds the received E1 SSM code word (see Table 2 for the E1 SSM code words). Each of other Sa bits (Sa5 to Sa8) can be used as well. Refer to the datasheet for the specific 82P228x product for the E1 Sa4 code word and application details.

Table 5. SSM Code Word in E1 Mode

Note: In the last column, S_{an1} to S_{an4} refer to the 4-bit code word in the E1 Sa code word register bits. The *n* can be 4 (for Sa4), 5 (for Sa5), 6 (for Sa6), 7 (for Sa7), or 8 (for Sa8). Each of the Sa bits in the TS0 of the E1 NFS frames can be used for this purpose.

Quality Level	Description	S_{an1}, S_{an2}, S_{an3}, S_{an4} Where n = bit number 4, 5, 6, 7, or 8
0	Quality unknown (existing synchronized network)	0000
1	Reserved	0001
2	Rec. G.811 (traceable to PRS)	0010
3	Reserved	0011
4	SSU-A (traceable to SSU type A, see G.812)	0100
5	Reserved	0101
6	Reserved	0110
7	Reserved	0111
8	SSU-B (traceable to SSU type B, see G.812)	1000
9	Reserved	1001
10	Reserved	1010
11	Synchronous Equipment Timing Source (SETS)	1011
12	Reserved	1100
13	Reserved	1101
14	Reserved	1110
15	Do not use for synchronization	1111

3.2.2.1 Register Configurations for BITS/SSU in the E1 Mode

Table 6. Configuration for BITS/SSU in E1 Mode

Operation	Register	Value	Definitions
Write	0x020	0x00	E1 Mode
Write	0x023	(See the next column for options)	Value: 0x00 – Definition: 2.048M, 75Ω; Value: 0x01 – Definition: 2.048M, 120Ω
Write	0x032	(See the next column for options)	Value: 0x00 – Definition: 75Ω; Value: 0x09 – Definition: 120Ω
Write	0x046	0x0C	Enable receive system side output
Write	0x047	0x00	Receive system side master clock mode
Write	0x03E	0x01	The REFA_OUT pin outputs a high level in the event of an LOS condition

Table 7. SSM Code Transmission and Reception for E1 Mode

Operation	Register	Value	Definitions
SSM Code Transmission			
Write	0x064	0x10	Sa4 insertion enable
Write	0x065	0x04	0x04 = SSU-A (traceable to SSU type A)
SSM Code Extraction			
Write	0x05C	0x10	Sa4 interrupt enable
Read	0x05D		Sa4I = 1 indicates the new SSM code has been received; write '1' to this bit to clear interrupt indication for the next extraction
Read	0x056		Read the SSM code

The user can use the interrupt of the 82P228x to obtain the SSM code. The INT pin must be connected to the controller for this purpose. The steps to use in E1 Mode are as follows:

1. Set the Sa4E bit (register 0x05C, bit 4) (5CH-b4) to enable the interrupt to the INT pin.
2. The controller waits for the interrupt.
3. If the interrupt is detected by the controller, read the 0x05D register.
4. Check the Sa4I bit (register 0x05D, bit 4). If this bit is 1, the 82P228x has received the new SSM code.
5. Write '1' to this Sa4I bit to clear this bit.
6. Read the 0x056 register. This register contains the value of the received SSM code.
7. Repeat steps 2 through 6.

4. G.703 – Chapter 13 Mode Operation

In G.703 – Chapter 13 operation, the reception and transmission of a 2048kHz clock, as described in G.703 Chapter 13, is required.

4.1 2048kHz Digital Clock Specifications

The transmit port (82P228x output) of a 2048kHz digital clock meets the following specifications. The signal is measured at the line side of the transmit transformer, at the near end of the cable, with a 75Ω or 120Ω resistive load in place of the cable.

Table 8. Digital 2048kHz Clock Interfaces

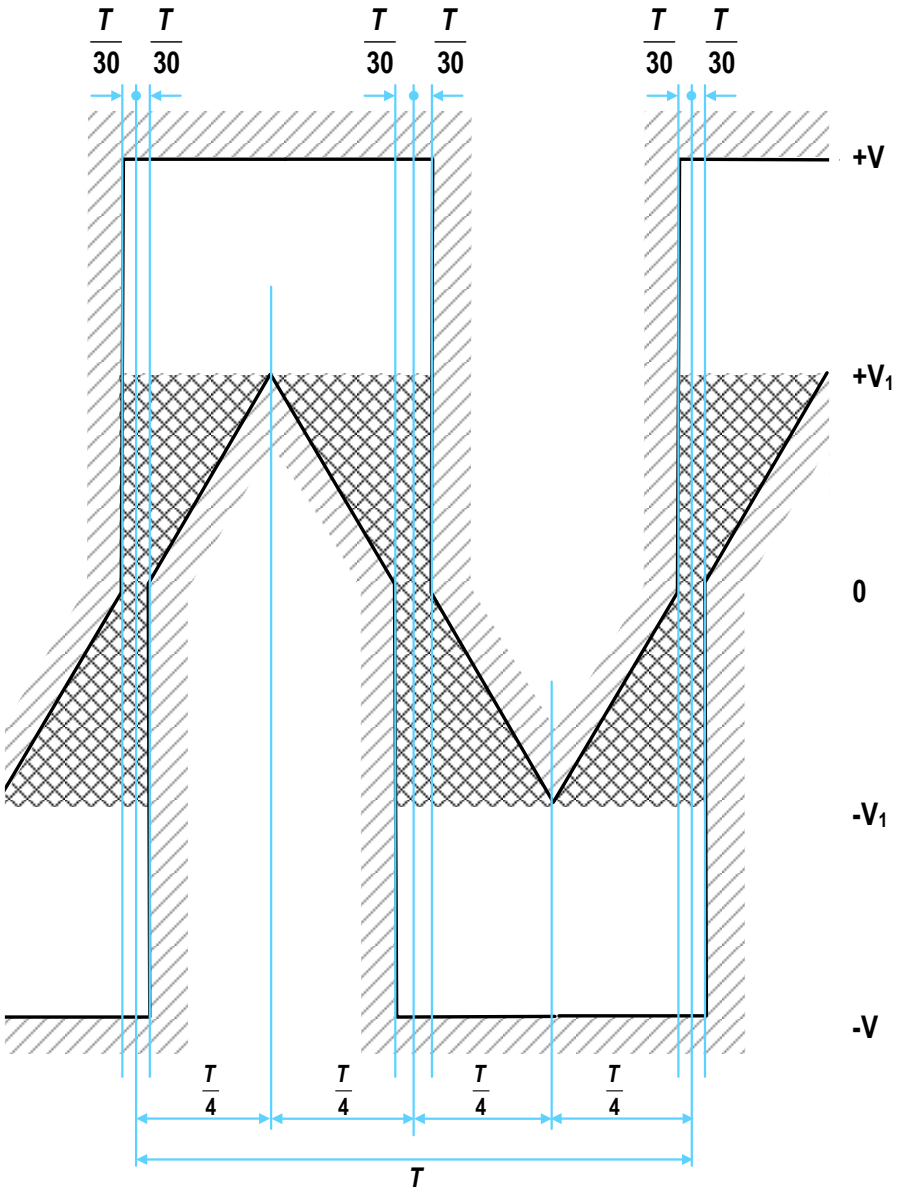
Parameter	Requirements	
Pulse Shape	▪ The signal must conform to the mask (see Figure 1). ▪ The value V corresponds to the maximum peak value. ▪ The value V_1 corresponds to the minimum peak value.	
Type of Interface	**Coaxial Pair**	**Symmetrical Pair**
Impedance	75Ω	120Ω
Maximum Peak Voltage (V)	1.5V	1.9V
Minimum Peak Voltage (V_1)	0.75V	1.0V
Maximum Jitter at Output	(See Table 9)	

Table 9. Maximum Permissible Jitter at Synchronization Interfaces

Output Interfaces	Frequency Accuracy	Measurement Bandwidth -3dB Frequencies	Peak-to-Peak Amplitude (Ulpp)
PRC	G.811	20Hz to 100kHz	0.05
SSU	G.812	20Hz to 100kHz	0.05
SEC	4.6 ppm (refer to G.813)	20Hz to 100kHz	0.5
		49Hz to 100kHz	0.2
PDH Synchronization	±50ppm	20Hz to 100kHz	1.5
		18Hz to 100kHz	0.2

Note: For other specifications (e.g., noise tolerance at input ports), refer to G.812 and G.813 for SSU and SEC, respectively.

Figure 1. Wave Shape at an Output Port of the 2048kHz Synchronization Interface



T = Average period of synchronizing signal

= Area where the signal should be monotonic

4.2 Configuration for G.703 Chapter 13 Mode

In G.703 Chapter 13 Mode, the 82P228x RSCK pin outputs a 4.096MHz clock, and duty cycle is from 60% to 95%. This clock should be divided into a 2048kHz clock as the received BITS/SSU clock. In the transmit direction, if transmission of a BITS/SSU clock is required, the 2048kHz clock should be input to the 82P228x TSCK pin.

Table 10. Configuration for G.703 Chapter 13 Mode

<table>
<tr><th>Operation</th><th>Register</th><th>Value</th><th>Definitions</th></tr>
<tr><td>Write</td><td>0x020</td><td>0x00</td><td>E1 Mode</td></tr>
<tr><td colspan="4">Transmission</td></tr>
<tr><td>Write</td><td>0x062</td><td>0x01</td><td>Un-frame</td></tr>
<tr><td>Write</td><td>0x06C</td><td>0x01</td><td>Transmit all ones</td></tr>
<tr><td>Write</td><td>0x022</td><td>0x02</td><td>Tx Dual Rail Mode</td></tr>
<tr><td>Write</td><td>0x023</td><td>(See the next column for options)</td><td><table><tr><th>Value</th><th>Definition</th></tr><tr><td>0x00</td><td>2.048M, 75Ω</td></tr><tr><td>0x01</td><td>2.048M, 120Ω</td></tr></table></td></tr>
<tr><td>Write</td><td>0x032</td><td>(See the next column for options)</td><td><table><tr><th>Value</th><th>Definition</th></tr><tr><td>0x00</td><td>75Ω</td></tr><tr><td>0x09</td><td>120Ω</td></tr></table></td></tr>
<tr><td>Write</td><td>0x021</td><td>0x08</td><td>Enable TJA</td></tr>
<tr><td colspan="4">Reception</td></tr>
<tr><td>Write</td><td>0x027</td><td>0x08</td><td>Enable RJA</td></tr>
<tr><td>Write</td><td>0x04D</td><td>0x08</td><td>Un-frame Mode</td></tr>
<tr><td>Write</td><td>0x046</td><td>0x0C</td><td>Enable receive system side output</td></tr>
<tr><td>Write</td><td>0x047</td><td>0x00</td><td>Receive system side clock master</td></tr>
<tr><td>Write</td><td>0x028</td><td>0x03</td><td>Receiver slicer mode</td></tr>
<tr><td>Write</td><td>0x02A</td><td>0x19</td><td>0x19 sets the following:
Pulse threshold = 50% for a ‘1’
Monitoring period = 128-bit long
Monitor gain = 22dB</td></tr>
</table>

5. Revision History

Revision Date	Description of Change
September 25, 2019	Updated the first sentence in “Configuration for G.703 Chapter 13 Mode”
January 14, 2019	Initial release.

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