

Thank you for purchasing the PG-FP6 flash memory programmer.

This document describes specifications that have been added or changed, along with restrictions and points for caution when using the PG-FP6. Also see the user's manual of the PG-FP6 regarding points for caution when using the PG-FP6.

See the following documents for restrictions applying to particular target MCUs.

- User's manuals of the target MCUs
- Documents in which restrictions applying to particular target MCUs are listed

See the following Web page for an outline of the PG-FP6.

<https://www.renesas.com/pg-fp6>

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Chapter 1. Product Version

Item No.	Programming GUI (FP6 Terminal)	Remark
1	V1.00.xx	—
2	V1.01.xx	—
3	V1.02.00	—
4	V1.02.01	—
5	V1.03.00	—
6	V1.03.01	—
	V1.03.02	—

Chapter 2. Additions and Changes to Specifications

2.1 List of additions and changes to specifications

No.	Additions and Changes to Specifications	Applicable MCUs	Product Version (Item No.)					
			1	2	3	4	5	6
1	Addition of an import function	All	×	✓	✓	✓	✓	✓
2	Addition of the saving of flash option information in an ESF file	All	×	✓	✓	✓	✓	✓
3	Addition of the writing of RPI files to MCUs	All	×	✓	✓	✓	✓	✓
4	Support for Renesas Synergy MCUs	Renesas Synergy	×	✓	✓	✓	✓	✓
5	Designating target blocks one by one	RH850 RX64M RX65N RX651 RX71M	×	✓	✓	✓	✓	✓
6	Change to the verify options	RH850 RX64M RX71M	×	×	✓	✓	✓	✓
7	Change to filling with 0xFF	RH850 RX64M RX65N RX651 RX71M Renesas Synergy	×	×	✓	✓	✓	✓
8	Addition of the feature for selecting the setup files that have recently been used	All	×	×	✓	✓	✓	✓
9	Change to the method for displaying and selecting programming areas	All	×	×	✓	✓	✓	✓
10	Addition of the feature for searching for the target MCU	All	×	×	✓	✓	✓	✓
11	Addition of gang-processing capabilities	All	×	×	×	×	✓	✓
12	Addition of the speed_mode command	V850 78K	×	×	×	×	✓	✓
13	Addition of the add option to the lod command	All	×	×	×	×	✓	✓
14	Improvement of the read function	RH850 RX R8C SuperH Renesas Synergy V850	×	×	×	×	✓	✓
15	Addition of a function for specifying the source of the clock signal	78K	×	×	×	×	✓	✓
16	Addition of a function for clearing the console window	All	×	×	×	×	✓	✓
17	Improvement of the file checksum function	All	×	×	×	×	✓	✓
18	Improvement of the function for uploading files	All	×	×	×	×	✓	✓
19	Improvement to the [File] menu	All	×	×	×	×	✓	✓

×: No additions or changes to specifications, ✓: Supported

2.2 Details of additions and changes

No. 1 Addition of an import function

Applicable MCUs: All

Description: [Import] was added to [Setup] on the [File] menu. Selecting [Import] allows you to open an ESF file created by using the FP5 or FP6, with the parameters in the corresponding PR5 file being updated at the same time.

Resolution: V1.01.00 and later versions of the FP6 Terminal support this feature.

No. 2 Addition of the saving of flash option information in an ESF file

Applicable MCUs: All

Description: You can now save the flash option information obtained by executing [Get Flash Options] on the [Target] menu as a new ESF file.

Resolution: V1.01.00 and later versions of the FP6 Terminal support this feature.

No. 3 Addition of the writing of RPI files to MCUs

Applicable MCUs: All

Description: A function for writing RPI files to MCUs was added. An RPI file is an image file in which data for programming in flash memory and flash options are combined, so can be managed as a single file for programming that includes the flash options. RPI files can be generated by V3.01.00 and later versions of Renesas Flash Programmer, a software tool for programming flash memory.

Resolution: V1.01.00 and later versions of the FP6 Terminal support this feature.

No. 4 Support for Renesas Synergy MCUs

Applicable MCUs: Renesas Synergy

Description: FP6 Terminal V1.01.00 supports SCI boot mode connection of Renesas Synergy MCUs.

Resolution: V1.01.00 and later versions of the FP6 Terminal support this feature.

No. 5 Designating target blocks one by one

Applicable MCUs: RH850, RX64M, RX65N, RX651, RX71M

Description: Target blocks can now be designated one by one on the [Block Setting] tabbed page of the [Setup] dialog box, instead of only having [Start Block] and [End Block] to set up a range.

Resolution: V1.01.00 and later versions of the FP6 Terminal support this feature.

No. 6 Change to the verify options

Applicable MCUs: RH850, RX64M, RX71M

Description: Options [Verify Flash Options] and [Skip ID Code Verify] are now supported.

Resolution: V1.02.00 and later versions of the FP6 Terminal support this feature.

No. 7 Change to filling with 0xFF

Applicable MCUs: RH850, RX64M, RX65N, RX651, RX71M, Renesas Synergy

Description: When you fill the ranges that do not contain program file data with 0xFF, programming or verification can be individually specified for the code flash and user-boot areas or the data flash area.

Resolution: V1.02.00 and later versions of the FP6 Terminal support this feature.

No. 8 Addition of the feature for selecting the setup files that have recently been used

Applicable MCUs: All

Description: The setup files that have most recently been used (up to four filenames) can be displayed and directly edited.

Resolution: V1.02.00 and later versions of the FP6 Terminal support this feature.

No. 9 Change to the method for displaying and selecting programming areas

Applicable MCUs: All

Description: All programming areas are displayed in a list; you can directly change the specified areas.

Resolution: V1.02.00 and later versions of the FP6 Terminal support this feature.

No. 10 Addition of the feature for searching for the target MCU

Applicable MCUs: All

Description: Searching for the target MCU in the [Create New Setting] dialog box is now possible.

Resolution: V1.02.00 and later versions of the FP6 Terminal support this feature.

No. 11 Addition of gang-processing capabilities

Applicable MCUs: All

Description: The FP6 gang programmer, which is software included with this product, enables the simultaneous control of multiple PG-FP6 units.

Resolution: V1.03.00 and later versions of the FP6 Terminal support this feature.

No. 12 Addition of the speed_mode command

Applicable MCUs: V850, 78K

Description: This command is used to adjust the wait time and timeout time in communications with the target MCU.

Resolution: V1.03.00 and later versions of the FP6 Terminal support this feature.

No. 13 Addition of the add option to the lod command

Applicable MCUs: All

Description: Specifying the add option with the lod command leads to omission of the erasure of the target programming area before downloading of the file for programming.

Resolution: V1.03.00 and later versions of the FP6 Terminal support this feature.

No. 14 Improvement of the read function

Applicable MCUs: RH850, RX, R8C, SuperH, Renesas Synergy, V850

Description: Data can be read after information on the memory to be read has been specified in the [Read Memory] dialog box.

Resolution: V1.03.00 and later versions of the FP6 Terminal support this feature.

No. 15 Addition of a function for specifying the source of the clock signal

Applicable MCU: 78K

Description: Specifying whether the source of the clock signal for the target device is within the target system or on the FP6 side is now possible.

Resolution: V1.03.00 and later versions of the FP6 Terminal support this feature.

No. 16 Addition of a function for clearing the console window

Applicable MCUs: All

Description: This allows clearing of the displays in the console window and status bar and the states of the LEDs of the FP6.

Resolution: V1.03.00 and later versions of the FP6 Terminal support this feature.

No. 17 Improvement of the file checksum function

Applicable MCUs: All

Description: The checksum can be calculated according to conditions specified in the [File Checksum] dialog box.

Resolution: V1.03.00 and later versions of the FP6 Terminal support this feature.

No. 18 Improvement of the function for uploading files

Applicable MCUs: All

Description: A file can be uploaded by specifying the name in the [File Upload] dialog box.

Resolution: V1.03.00 and later versions of the FP6 Terminal support this feature.

No. 19 Improvement to the [File] menu

Applicable MCUs: All

Description: The ease of use of the PG-FP6 has been improved by integrating the functionality of the [Import Setup File...] menu item into the [Open Setup File...] menu item.

Resolution: V1.03.00 and later versions of the FP6 Terminal support this feature.

Chapter 3. Restrictions

3.1 List of restrictions

No.	Restrictions	Applicable MCUs	Product Version (Item No.)					
			1	2	3	4	5	6
1	Point to note regarding a battery management IC	Battery management IC	×	✓	✓	✓	✓	✓
2	RH850/F1K group	RH850/F1K	×	×	✓	✓	✓	✓
3	Reset vector setting for V850ES/Dx2, V850/Fx2, and V850ES/Hx2	V850ES/Dx2, V850ES/Fx2, V850ES/Hx2	×	×	×	✓	✓	✓
4	RH850/F1K group, RH850/F1KM-S1 group and RH850/F1KM-S4 group	RH850/F1K, RH850/F1KM-S1, RH850/F1KM-S4	×	×	×	×	✓	✓
5	Point for caution regarding enabling of the intelligent cryptographic unit slave E (ICUSE) of the RH850/C1M-A, RH850/F1K, RH850/F1KM-S1, RH850/P1L-C, and RH850/P1M-E groups	RH850/C1M-A, RH850/F1K, RH850/F1KM-S1, RH850/P1L-C, RH850/P1M-E	×	×	×	×	×	✓
6	Reading PG-FP5 setting files for the RX64M, RX651, RX65N, RX66T, and RX71M groups	RX64M, RX651, RX65N, RX66T, RX71M	—	—	—	—	×	×

×: Not fixed, ✓: Fixed, —: Not supported

3.2 Details of restrictions

No. 1 Point to note regarding a battery management IC

Applicable MCU:

Group	Part Number
Battery management IC	RAJ240045

Description: The error below occurs and connection fails when commands are executed for the IC.
"ERROR(E024): Invalid signature code."

Resolution: This problem has been fixed and does not arise with V1.01.00 and later versions of the FP6 Terminal.

No. 2 RH850/F1K group

Applicable MCU:

Group	Part Number
RH850/F1K	R7F701611

Description: Details on this problem are given in the issue of Renesas Tool News (document no.: R20TS0339EJ0100) at the following URL.

<https://www.renesas.com/search/keyword-search.html#genre=document&q=r20ts0339>

Resolution: This problem has been fixed and does not arise with V1.02.00 and later versions of the FP6 Terminal.

No. 3 Reset vector setting for V850ES/Dx2, V850/Fx2, and V850ES/Hx2

Applicable MCUs:

Group	Part Number
V850ES/Dx2	UPD70F3319A
V850ES/Fx2	UPD70F3231, UPD70F3232, UPD70F3233, UPD70F3234, UPD70F3235, UPD70F3237
V850ES/Hx2	UPD70F3700, UPD70F3701, UPD70F3702, UPD70F3703, UPD70F3704, UPD70F3706, UPD70F3707, UPD70F3709, UPD70F3710

Description: Details on this problem are given in the issue of Renesas Tool News (document no.: R20TS0339EJ0100) at the following URL.
<https://www.renesas.com/search/keyword-search.html#genre=document&q=r20ts0339>

Resolution: This problem has been fixed and does not arise with V1.02.01 and later versions of the FP6 Terminal.

No. 4 RH850/F1K group, RH850/F1KM-S1 group and RH850/F1KM-S4 group

Applicable MCUs:

Group	Part Number
RH850/F1K	R7F701542, R7F701543, R7F701546, R7F701547, R7F701557, R7F701560, R7F701561, R7F701562, R7F701563, R7F701566, R7F701567, R7F701577, R7F701580, R7F701581, R7F701582, R7F701583, R7F701586, R7F701587, R7F701597, R7F701602, R7F701603, R7F701610, R7F701611, R7F701612, R7F701613, R7F701620, R7F701621, R7F701622, R7F701623
RH850/F1KM-S1	R7F701684, R7F701685, R7F701686, R7F701687, R7F701688, R7F701689, R7F701690, R7F701691, R7F701692, R7F701693, R7F701694, R7F701695
RH850/F1KM-S4	R7F701644, R7F701645, R7F701646, R7F701647, R7F701648, R7F701649, R7F701650, R7F701651

Description: Details on this problem are given in the issue of Renesas Tool News (document no.: R20TS0388EJ0100) at the following URL.
<https://www.renesas.com/search/keyword-search.html#genre=document&q=r20ts0388>

Resolution: This problem has been fixed and does not arise with V1.03.00 and later versions of the FP6 Terminal.

No. 5 Point for caution regarding enabling of the intelligent cryptographic unit slave E (ICUSE) of the RH850/C1M-A, RH850/F1K, RH850/F1KM-S1, RH850/P1L-C, and RH850/P1M-E groups

Applicable MCUs: RH850/C1M-A, RH850/F1K, RH850/F1KM-S1, RH850/P1L-C, and RH850/P1M-E groups
 For the part numbers, refer to the issue of Renesas Tool News stated in [Description] below.

Description: Details on this problem are given in the issue of Renesas Tool News (document no.: R20TS0399EJ0100) at the following URL.
<https://www.renesas.com/search/keyword-search.html#genre=document&q=r20ts0399>

Resolution: This problem has been fixed and does not arise with V1.03.01 and later versions of the FP6 Terminal.

No. 6 [Reading PG-FP5 setting files for the RX64M, RX651, RX65N, RX66T, and RX71M groups](#)

Applicable MCUs: RX64M, RX651, RX65N, RX66T, and RX71M groups

For the part numbers, refer to the issue of Renesas Tool News stated in [Description] below.

Description: Details on this problem are given in the issue of Renesas Tool News

(document no.: R20TS0410EJ0101) at the following URL.

<https://www.renesas.com/search/keyword-search.html#genre=document&q=r20ts0410>

Resolution: This problem will be fixed in the version of Programming GUI for PG-FP6 (FP6 Terminal) scheduled to be released in October 2019.

Chapter 4. Points for Caution

This chapter introduces requirements for the supported MCU groups.

For the range of values that can be selected for "Input Frequency" and "Multiplier", refer to the user's manual for the MCU.

4.1 RX110, RX111, RX113, RX130

Input Frequency	Multiplier
2-wire UART: 16 MHz FINE: 8 MHz (VCC < 3V), 32 MHz (VCC ≥ 3V)	CPU 1.0 Peripheral 1.0

4.2 RX220

Input Frequency	Multiplier
32 MHz	CPU 0.5 (VCC < 3 V), 1.0 (VCC ≥ 3 V) Peripheral 0.5 (VCC < 3 V), 1.0 (VCC ≥ 3 V)

4.3 RX230, RX231, RX23E-A, RX23W

Input Frequency	Multiplier	Speed
8 MHz (VCC < 3 V), 32 MHz (VCC ≥ 3 V)	2-wire UART: CPU 2.0, peripheral 2.0 FINE: CPU 1.0, peripheral 1.0	When the input frequency is 8 MHz, do not select 1,000,000 bps or a higher rate.

4.4 RX23T, RX24T, RX24U

Input Frequency	Multiplier
32 MHz	2-wire UART: CPU 2.0, peripheral 2.0 FINE: CPU 1.0, peripheral 1.0

4.5 RX610, RX621, RX62N

Input Frequency	Multiplier
8 MHz ≤ f _x ≤ 14 MHz	CPU 1.0, 2.0, 4.0, 8.0 Peripheral 1.0, 2.0, 4.0, 8.0

Ensure that [Input Frequency] × [Multiplier (CPU)] = 8 MHz to 100 MHz (for ICLK) and [Input Frequency] × [Multiplier (Peripheral)] = 8 MHz to 50 MHz (for PCLK).

4.6 RX62G, RX62T

Input Frequency	Multiplier
8 MHz ≤ f _x ≤ 12.5 MHz	CPU 1.0, 2.0, 4.0, 8.0 Peripheral 1.0, 2.0, 4.0, 8.0

Ensure that [Input Frequency] × [Multiplier (CPU)] = 8 MHz to 100 MHz (for ICLK) and [Input Frequency] × [Multiplier (Peripheral)] = 8 MHz to 50 MHz (for PCLK).

4.7 RX630, RX631, RX63N

RX631: R5F56316, R5F56317, R5F56318, R5F5631F, R5F5631G, R5F5631J, R5F5631W, R5F5631Y
 RX63N: R5F563NF, R5F563NG, R5F563NJ, R5F563NW, R5F563NY

Input Frequency	Multiplier
4 MHz ≤ f_x ≤ 16 MHz	CPU 1.0, 2.0, 4.0, 8.0, 16.0 Peripheral 1.0, 2.0, 4.0, 8.0

Ensure that [Input Frequency] × [Multiplier (CPU)] = 4 MHz to 100 MHz (for ICLK) and [Input Frequency] × [Multiplier (Peripheral)] = 4 MHz to 50 MHz (for PCLK).

RX630

RX631: Other than the R5F56316, R5F56317, R5F56318, R5F5631F, R5F5631G, R5F5631J, R5F5631W, and R5F5631Y

RX63N: Other than the R5F563NF, R5F563NG, R5F563NJ, R5F563NW, and R5F563NY

Input Frequency	Multiplier
4 MHz ≤ f_x ≤ 16 MHz	CPU 1.0, 2.0, 4.0, 8.0, 16.0 Peripheral 1.0, 2.0, 4.0, 8.0

Ensure that [Input Frequency] × [Multiplier (CPU)] = 8 MHz to 100 MHz (for ICLK) and [Input Frequency] × [Multiplier (Peripheral)] = 8 MHz to 50 MHz (for PCLK).

4.8 RX634

Input Frequency	Multiplier
4 MHz ≤ f_x ≤ 16 MHz	CPU 1.0, 2.0, 4.0, 8.0, 16.0 Peripheral 1.0, 2.0, 4.0, 8.0

Ensure that [Input Frequency] × [Multiplier (CPU)] = 4 MHz to 54 MHz (for ICLK) and [Input Frequency] × [Multiplier (Peripheral)] = 4 MHz to 32 MHz (for PCLK).

4.9 RX63T

RX63T: R5F563TB, R5F563TC, R5F563TE

Input Frequency	Multiplier
8 MHz ≤ f_x ≤ 12.5 MHz	CPU 1.0, 2.0, 4.0, 8.0, 16.0 Peripheral 1.0, 2.0, 4.0, 8.0

Ensure that [Input Frequency] × [Multiplier (CPU)] = 8 MHz to 100 MHz (for ICLK) and [Input Frequency] × [Multiplier (Peripheral)] = 8 MHz to 50 MHz (for PCLK).

RX63T: Other than the R5F563TB, R5F563TC, and R5F563TE

Input Frequency	Multiplier
4 MHz ≤ f_x ≤ 16 MHz	CPU 1.0, 2.0, 4.0, 8.0, 16.0 Peripheral 1.0, 2.0, 4.0, 8.0

Ensure that [Input Frequency] × [Multiplier (CPU)] = 4 MHz to 100 MHz (for ICLK) and [Input Frequency] × [Multiplier (Peripheral)] = 4 MHz to 50 MHz (for PCLK).

4.10 RX651, RX65N, RX72M

RX651: R5F5651C, R5F5651E
 RX65N: R5F565NC, R5F565NE
 RX72M: R5F572MD, R5F572MN

When you create a new setting file for the FP6 Terminal, select a target device name that matches the bank mode selected by the Bank Mode Select bits in the option-setting memory.

Bank Mode Select	Target Device	Parameter File
Linear mode	R5F5651C (Linear Mode)	R5F5651_L_2.pr6
	R5F5651E (Linear Mode)	R5F5651_L_2.pr6
	R5F565NC (Linear Mode)	R5F565N_L_2.pr6
	R5F565NE (Linear Mode)	R5F565N_L_2.pr6
	R5F572MD (Linear Mode)	R5F572M_L.pr6
	R5F572MN (Linear Mode)	R5F572M_L.pr6
Dual mode	R5F5651C (Dual Mode)	R5F5651_D_2.pr6
	R5F5651E (Dual Mode)	R5F5651_D_2.pr6
	R5F565NC (Dual Mode)	R5F565N_D_2.pr6
	R5F565NE (Dual Mode)	R5F565N_D_2.pr6
	R5F572MD (Dual Mode)	R5F572M_D.pr6
	R5F572MN (Dual Mode)	R5F572M_D.pr6

The following error messages will appear when the FP6 is connected to an MCU with a different bank mode.

Message displayed on the FP6: ERROR:023 Inv. Sig. addr.
 FP6 Terminal: ERROR(E023): Connection or synchronisation failed.

The bank mode for the MCU is changed by the following actions.

- Resetting the MCU after a setting for bank mode which differs from the current setting has been written to the Bank Mode Select bits
- Resetting the MCU after selecting [Erase Chip] to erase a chip that is currently in dual mode

How to switch a chip from the linear mode to the dual mode

1. Create a new ESF file for an MCU in the linear mode.
2. Select the erasure option as [Erase Chip] to erase the chip.
3. Program the option-setting memory with a file that specifies the dual mode.
4. Reset the MCU.

4.11 78K0/Dx2, 78K0/Fx2, 78K0/Kx2, 78K0/Kx2-C, 78K0/Lx2, 78K0/Lx3, 78K0/Lx3-M, UPD78F0730, UPD78F8019, UPD78F8020, UPD78F8024/UPD78F8025, UPD78F8032, UPD78F8077

Interface	Clock	Multiplier
CSI Internal OSC	Internal oscillation circuit	Do not change
UART EXCLK	External clock	
UART X1 OSC	External oscillation circuit	
UART Internal OSC	Internal oscillation circuit	

4.12 V850E/IA3, V850E/IA4, V850ES/Dx2, V850ES/Fx2, V850ES/IK1, V850E/Sx2-H, V850E/lx3, V850ES/Hx2, V850ES/IE2

Multiplier	Speed
Do not change	For 2-wire UART communications, do not select 115,200 or 500,000 bps.

4.13 V850E/Sx3-H

Input Frequency	Multiplier
$3 \text{ MHz} \leq f_x \leq 6 \text{ MHz}$	CPU 8.0
$6 \text{ MHz} < f_x \leq 10 \text{ MHz}$	CPU 4.0

4.14 V850ES/Sx2, V850ES/Jx2

Input Frequency	Multiplier	Speed
$2.5 \text{ MHz} \leq f_x \leq 5 \text{ MHz}$	CPU 4.0	For 2-wire UART communications, do not select 115,200 or 500,000 bps.
$5 \text{ MHz} < f_x \leq 10 \text{ MHz}$	CPU 2.0	

4.15 V850ES/Jx3, V850ES/Sx3

Input Frequency	Multiplier	Speed
$2.5 \text{ MHz} \leq f_x \leq 4 \text{ MHz}$	CPU 8.0	For 2-wire UART communications, do not select 500,000 bps.
$4 \text{ MHz} < f_x \leq 5 \text{ MHz}$	CPU 4.0	
$5 \text{ MHz} < f_x \leq 10 \text{ MHz}$	CPU 1.0	

Changing reset vector values in the [Setup] dialog box of the FP6 has no effect since it is not possible with these MCUs.

4.16 V850ES/Kx1, V850ES/Kx1+, V850ES/Kx2

Input Frequency	Multiplier	Speed
$2 \text{ MHz} \leq f_x \leq 5 \text{ MHz}$	CPU 4.0	For 2-wire UART communications, do not select 115,200 or 500,000 bps.
$5 \text{ MHz} < f_x \leq 10 \text{ MHz}$	CPU 1.0	

4.17 V850ES/Jx3-L

Input Frequency	Multiplier	Speed
$2.5 \text{ MHz} \leq f_x \leq 5 \text{ MHz}$	CPU 4.0	For 2-wire UART communications, do not select 500,000 bps.
$5 \text{ MHz} < f_x \leq 10 \text{ MHz}$	CPU 1.0	

Changing reset vector values in the [Setup] dialog box of the FP6 has no effect since it is not possible with these MCUs.

4.18 V850ES/Hx3, V850ES/Fx3

V850ES/Hx3: UPD70F3757

V850ES/Fx3: UPD70F3376A, UPD70F3377A, UPD70F3379, UPD70F3380, UPD70F3381, UPD70F3382, UPD70F3383, UPD70F3384, UPD70F3385

Input Frequency	Multiplier	Speed
$4 \text{ MHz} \leq f_x \leq 6 \text{ MHz}$	CPU 8.0	For 2-wire UART communications, do not select 500,000 bps.
$6 \text{ MHz} < f_x \leq 12 \text{ MHz}$	CPU 4.0	
$12 \text{ MHz} < f_x \leq 16 \text{ MHz}$	CPU 2.0	

V850ES/Hx3: Other than the UPD70F3757

V850ES/Fx3: UPD70F3370A, UPD70F3371, UPD70F3372, UPD70F3373, UPD70F3374, UPD70F3375, UPD70F3378

Input Frequency	Multiplier	Speed
4 MHz	CPU 8.0	For 2-wire UART communications, do not select 500,000 bps.
$4 \text{ MHz} < f_x \leq 8 \text{ MHz}$	CPU 4.0	
$8 \text{ MHz} < f_x \leq 16 \text{ MHz}$	CPU 2.0	

4.19 V850ES/Jx3-H, V850ES/Jx3-U, V850ES/Jx3-E

Multiplier	Speed
Do not change	For 2-wire UART communications, do not select 500,000 bps.

Changing reset vector values in the [Setup] dialog box of the FP6 has no effect since it is not possible with these MCUs.

4.20 V850E/Dx3, V850E/lx4, V850E/lx4-H

Multiplier	Speed
Do not change	For 2-wire UART communications, do not select 500,000 bps.

4.21 V850ES/Fx3-L

Input Frequency	Multiplier	Speed
$4 \text{ MHz} \leq f_x \leq 5 \text{ MHz}$	CPU 4.0	For 2-wire UART communications, do not select 500,000 bps.
$5 \text{ MHz} < f_x \leq 10 \text{ MHz}$	CPU 2.0	
$10 \text{ MHz} < f_x \leq 16 \text{ MHz}$	CPU 1.0	

4.22 V850ES/Dx4, V850ES/Dx4-H

Speed
For 1-wire UART communications, do not select 2,000,000 bps.

4.23 V850E2/Fx4, V850E2/Fx4-M

Input Frequency	Multiplier	Speed
4 MHz	CPU 20.0	For 1-wire UART communications, do not select 2,000,000 bps.
$4 \text{ MHz} < f_x \leq 5 \text{ MHz}$	CPU 16.0	
$5 \text{ MHz} < f_x \leq 8 \text{ MHz}$	CPU 10.0	
$8 \text{ MHz} < f_x \leq 16 \text{ MHz}$	CPU 5.0	
$16 \text{ MHz} < f_x \leq 20 \text{ MHz}$	CPU 4.0	

4.24 V850E2/Fx4-L

UPD70F3579, UPD70F3580, UPD70F3584, UPD70F3585

Input Frequency	Multiplier	Speed
4 MHz	CPU 16.0	For 1-wire UART communications, do not select 2,000,000 bps.
$4 \text{ MHz} < f_x \leq 5 \text{ MHz}$	CPU 9.0	
$5 \text{ MHz} < f_x \leq 8 \text{ MHz}$	CPU 8.0	
$8 \text{ MHz} < f_x \leq 16 \text{ MHz}$	CPU 4.0	
$16 \text{ MHz} < f_x \leq 20 \text{ MHz}$	CPU 1.0	

Other than the UPD70F3579, UPD70F3580, UPD70F3584, UPD70F3585

Input Frequency	Multiplier	Speed
4 MHz	CPU 12.0	For 1-wire UART communications, do not select 2,000,000 bps.
$4 \text{ MHz} < f_x \leq 5 \text{ MHz}$	CPU 9.0	
$5 \text{ MHz} < f_x \leq 8 \text{ MHz}$	CPU 5.0	
$8 \text{ MHz} < f_x \leq 16 \text{ MHz}$	CPU 2.0	
$16 \text{ MHz} < f_x \leq 20 \text{ MHz}$	CPU 1.0	

4.25 V850E2/Fx4-G

UPD70F3592

Input Frequency	Multiplier	Speed
4 MHz	CPU 20.0	For 1-wire UART communications, do not select 2,000,000 bps.
4 MHz < fx ≤ 5 MHz	CPU 16.0	
5 MHz < fx ≤ 8 MHz	CPU 10.0	
8 MHz < fx ≤ 16 MHz	CPU 5.0	
16 MHz < fx ≤ 20 MHz	CPU 4.0	

Other than the UPD70F3592

Input Frequency	Multiplier	Speed
4 MHz	CPU 16.0	For 1-wire UART communications, do not select 2,000,000 bps.
4 MHz < fx ≤ 5 MHz	CPU 9.0	
5 MHz < fx ≤ 8 MHz	CPU 8.0	
8 MHz < fx ≤ 16 MHz	CPU 4.0	
16 MHz < fx ≤ 20 MHz	CPU 1.0	

4.26 V850E2/Mx4

Multiplier	Speed
Do not change	For 1-wire UART communications, do not select 2,000,000 bps.

4.27 SH7146, SH7149

Input Frequency	Multiplier
5 MHz ≤ fx ≤ 12.5 MHz	CPU 1.0, 2.0, 4.0, 8.0 Peripheral 1.0, 2.0, 4.0, 8.0

Ensure that [Input Frequency] × [Multiplier (CPU)] = 10 MHz to 80 MHz (for ICLK) and [Input Frequency] × [Multiplier (Peripheral)] = 10 MHz to 40 MHz (for PCLK).

4.28 SH7214, SH7216

SH7214: R5F72145A, R5F72146A, R5F72147A, R5F72145B, R5F72146B, R5F72147B

SH7216: R5F72165A, R5F72166A, R5F72167A, R5F72165B, R5F72166B, R5F72167B

Input Frequency	Multiplier
10 MHz ≤ fx ≤ 12.5 MHz	CPU 2.0, 4.0, 8.0, 16.0 Peripheral 2.0, 4.0

Ensure that [Input Frequency] × [Multiplier (CPU)] = 20 MHz to 200 MHz (for ICLK) and [Input Frequency] × [Multiplier (Peripheral)] = 20 MHz to 50 MHz (for PCLK).

SH7214: R5F72145G, R5F72146G, R5F72147G, R5F72145H, R5F72146H, R5F72147H

SH7216: R5F72165G, R5F72166G, R5F72167G, R5F72165H, R5F72166H, R5F72167H

Input Frequency	Multiplier
10 MHz ≤ fx ≤ 12.5 MHz	CPU 2.0, 4.0, 8.0, 16.0 Peripheral 2.0, 4.0

Ensure that [Input Frequency] × [Multiplier (CPU)] = 20 MHz to 100 MHz (for ICLK) and [Input Frequency] × [Multiplier (Peripheral)] = 20 MHz to 50 MHz (for PCLK).

4.29 SH7253

Input Frequency	Multiplier	Pin Setting
16 MHz ≤ f _x ≤ 20 MHz	CPU 6.0 Peripheral 1.0	MD_CLK0: 0 MD_CLKP: 0
	CPU 6.0 Peripheral 2.0	MD_CLK0: 0 MD_CLKP: 1
	CPU 8.0 Peripheral 1.0	MD_CLK0: 1 MD_CLKP: 0
	CPU 8.0 Peripheral 2.0	MD_CLK0: 1 MD_CLKP: 1

4.30 SH72A0

Input Frequency	Multiplier
8 MHz, 10 MHz	CPU 8.0 Peripheral 4.0

4.31 SH72A2

Input Frequency	Multiplier
8 MHz, 10 MHz	CPU 10.0 Peripheral 5.0

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