

ISL71090SEH75

7.5V Radiation Hardened Ultra Low Noise, Precision Voltage Reference

The ISL71090SEH75 is an ultra low noise, high DC accuracy precision voltage reference with a wide input voltage range from 9.2V to 30V. The ISL71090SEH75 uses the advanced bipolar technology to achieve $1.0\mu\text{V}_{\text{P-P}}$ noise at 0.1Hz with an accuracy over temperature of 0.15%.

The ISL71090SEH75 offers a 7.5V output voltage with 10ppm/°C temperature coefficient and also provides excellent line and load regulation. The device is offered in an 8 Ld flatpack package.

The ISL71090SEH75 is ideal for high-end instrumentation, data acquisition and applications requiring high DC precision where low noise performance is critical.

Applications

- RH voltage regulators precision outputs
- Precision voltage sources for data acquisition system for space applications
- Strain and pressure gauge for space applications

Features

- Reference output voltage: 7.5V $\pm 0.05\%$
- Accuracy over temperature: $\pm 0.15\%$
- Output voltage noise: $1.0\mu\text{V}_{\text{P-P}}$ typ (0.1Hz to 10Hz)
- Supply current: 930 μA (typical)
- Tempco (box method): 10ppm/°C max
- Output current capability: 20mA
- Line regulation: 8ppm/V
- Load regulation: 10ppm/mA
- Operating temperature range: -55°C to +125°C
- Radiation acceptance testing (see TID report)
 - High dose rate (50-300rad(Si)/s): 100krad(Si)
 - Low dose rate (0.01rad(Si)/s): 50krad(Si)
- SEE hardness (see SEE report for details)
 - SET/SEL/SEB 86MeV•cm²/mg
- Electrically screened to SMD 5962-13211

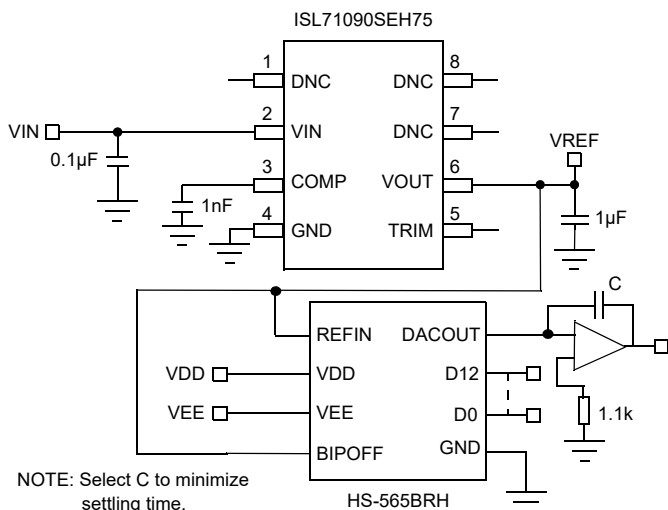


Figure 1. ISL71090SEH75 Typical Application Diagram

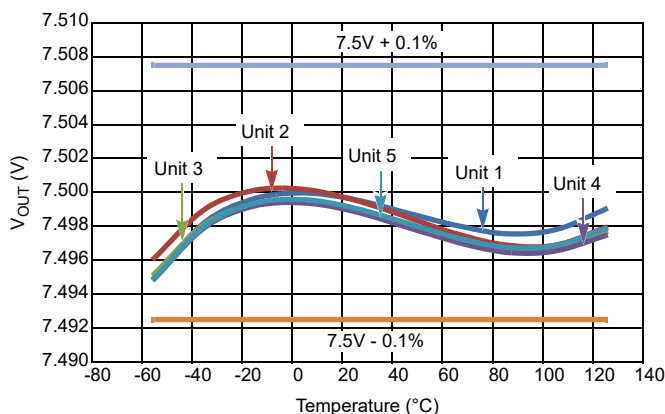


Figure 2. V_{OUT} vs Temperature

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1. Overview

1.1 Functional Block Diagram

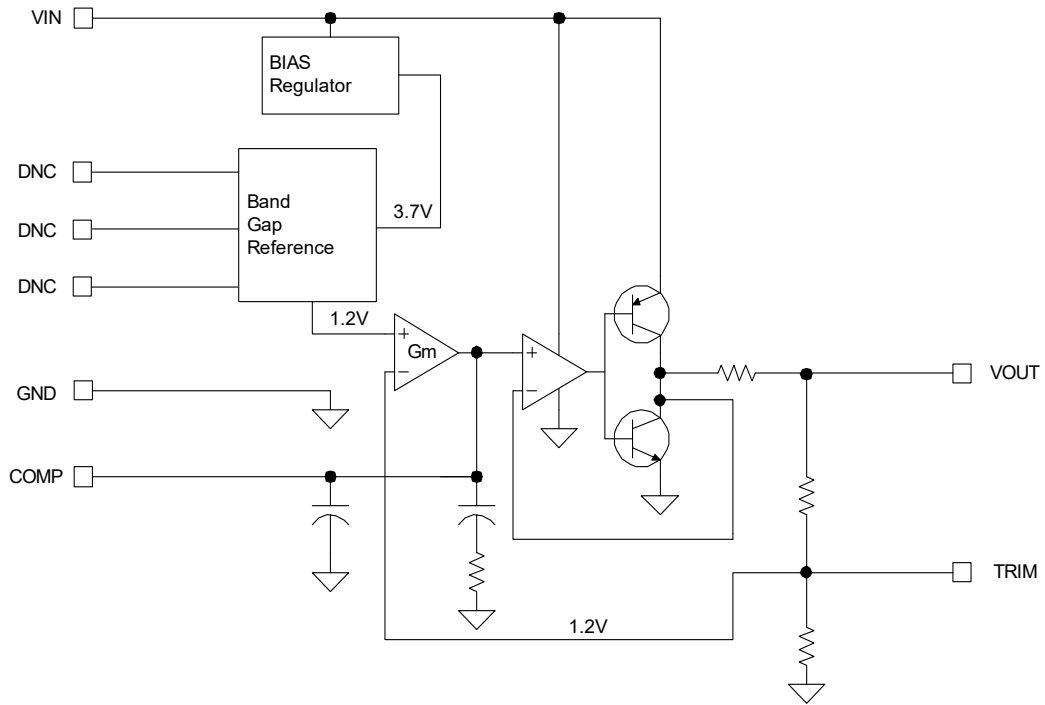


Figure 3. Functional Block Diagram

1.2 Typical Trim Application Diagram

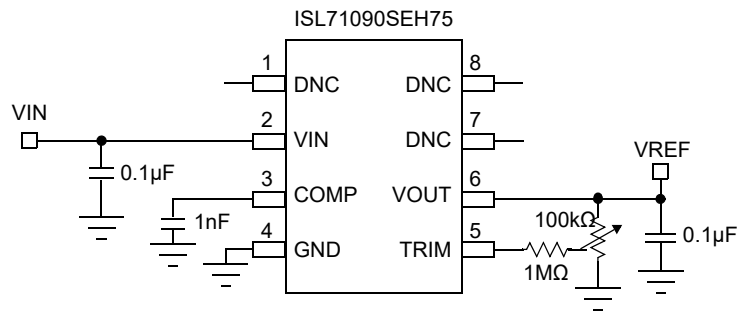
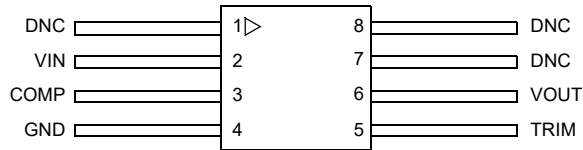


Figure 4. Typical Trim Application Diagram

2. Pin Information

2.1 Pin Assignments

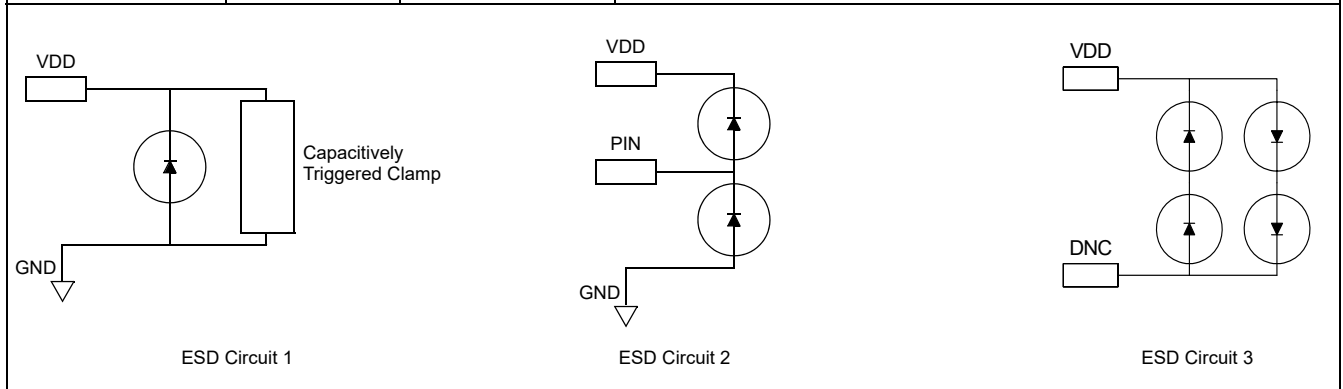


Note: The ESD triangular mark is indicative of pin #1. It is a part of the device marking and is placed on the lid in the quadrant where pin #1 is located.

Figure 5. Pin Assignments- Top View

2.2 Pin Descriptions

Pin Number	Pin Name	ESD Circuit	Description
1, 7, 8	DNC	3	Do not connect. Internally terminated.
2	VIN	1	Input voltage connection
3	COMP	2	Compensation and noise reduction capacitor
4	GND	1	Ground connection. also connected to the lid.
5	TRIM	2	Voltage reference trim input
6	VOUT	2	Voltage reference output



3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter ^{[1][2]}	Minimum	Maximum	Unit
V _{IN} to GND	-0.5	40	V
V _{IN} to GND at an LET = 86MeV•cm ² /mg	-0.5	36	V
V _{OUT} to GND (10s)	-0.5	V _{OUT} + 0.5V	V
Voltage on any Pin to Ground	-0.5	V _{OUT} + 0.5V	V
Voltage on DNC Pins ^[3]	-	-	-
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per MIL-PRF-883 3015.7)	-	2	kV
Machine Model (Tested per JESD22-A115-A)	-	200	V
Charged Device Model (Tested per JESD22-C101D)	-	750	V

- Product capability established by initial characterization. Radiation acceptance tested on a wafer-by-wafer basis to 100krad(Si) at high dose rate and to 50krad(Si) at low dose rate.
- The output capacitance used for SEE testing is C_{IN} = 0.1μF and C_{OUT} = 1μF.
- No connections permitted to these pins.

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Input Voltage, V _{IN}	9.2	30	V
Ambient Temperature	-55	+125	°C

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	8 Ld Flatpack Package	θ _{JA} ^[1]	Junction to ambient	140	°C/W
		θ _{JC} ^[2]	Junction to case	15	°C/W

- θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See [TB379](#) for details.
- For θ_{JC}, the case temperature location is the center of the ceramic on the package underside.

3.4 Electrical Specifications

3.4.1 Flatpack Packaged Device

$V_{IN} = 15V$, $I_{OUT} = 0mA$, $C_L = 0.1\mu F$ and $C_C = 1nF$ unless otherwise specified. **Boldface limits apply after radiation at +25°C and across the operating temperature range, -55°C to +125°C without radiation, unless otherwise specified.**

Parameter	Symbol	Test Conditions	Min ^[1]	Typ	Max ^[1]	Unit
Output Voltage	V_{OUT}			7.5		V
V_{OUT} Accuracy at	V_{OA}	$V_{OUT} = 7.5V^{[2]}$, $T_A = +25^\circ C$	-0.05		+0.05	%
		$V_{OUT} = 7.5V^{[2]}$, $T_A = -55^\circ C$ to $+125^\circ C$	-0.15		+0.15	
		$V_{OUT} = 7.5V^{[2]}$, $T_A = +25^\circ C$, Post Radiation	-0.3		+0.3	
Output Voltage Temperature Coefficient ^[3]	TC V_{OUT}				10	ppm/°C
Input Voltage Range	V_{IN}		9.2		30	V
Supply Current	I_{IN}			0.930	1.500	mA
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$	$V_{IN} = 9.2V$ to $30V$		8	20	ppm/V
Load Regulation	$\Delta V_{OUT} / \Delta I_{OUT}$	Sourcing: $0mA \leq I_{OUT} \leq 20mA$		10	20	ppm/mA
		Sinking: $-10mA \leq I_{OUT} \leq 0mA$		21	40	
Dropout Voltage ^[4]	V_D			1.5	1.7	V
Short-Circuit Current	I_{SC+}	$T_A = +25^\circ C$, V_{OUT} tied to GND		53		mA
Short-Circuit Current	I_{SC-}	$T_A = +25^\circ C$, V_{OUT} tied to V_{IN}		-63		mA
Turn-On Settling Time	t_R	90% of final value, $C_L = 1.0\mu F$, $C_C = open$		250		μs
Ripple Rejection	PSRR	$f = 120Hz$		90		dB
Output Voltage Noise	e_N	$0.1Hz \leq f \leq 10Hz$		1.0		μV_{P-P}
Broadband Voltage Noise	V_N	$10Hz \leq f \leq 1kHz$		1.2		μV_{RMS}
Noise Density		$f = 1kHz$, $V_{IN} = 9.5V$		38		nV/\sqrt{Hz}
Long Term Drift	$\Delta V_{OUT} / \Delta t$	$T_A = +125^\circ C$, 1000hrs		15		ppm

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
2. Post-reflow drift for the ISL71090SEH75 devices can be 100 μV typical based on experimental results with devices on FR4 double sided boards. The engineer must take this into account when considering the reference voltage after assembly.
3. Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in $V_{OUT(max)} - V_{OUT(min)}$ is divided by the temperature range; in this case, $-55^\circ C$ to $+125^\circ C = +180^\circ C$.
4. Dropout Voltage is the minimum $V_{IN} - V_{OUT}$ differential voltage measured at the point where V_{OUT} drops 1mV from $V_{IN} = nominal$ at $T_A = +25^\circ C$.

3.4.2 Die

$V_{IN} = 15V$, $I_{OUT} = 0mA$, $C_L = 0.1\mu F$ and $C_C = 1nF$ unless otherwise specified. **Boldface limits apply after radiation at +25°C and across the operating temperature range, -55°C to +125°C without radiation, unless otherwise specified. Specifications over temperature are guaranteed but not production tested on die.**

Parameter	Symbol	Test Conditions	Min ^[1]	Typ	Max ^[1]	Unit
Output Voltage	V_{OUT}			7.5		V
V_{OUT} Accuracy	V_{OA}	$V_{OUT} = 7.5V^{[2]}$, $T_A = +25^\circ C$	-0.05		+0.05	%
		$V_{OUT} = 7.5V^{[2]}$, $T_A = -55^\circ C$ to $+125^\circ C$	-0.15		+0.15	
		$V_{OUT} = 7.5V^{[2]}$, $T_A = +25^\circ C$, Post Radiation	-0.3		+0.3	
Output Voltage Temperature Coefficient ^[3]	TC V_{OUT}				10	ppm/°C
Input Voltage Range	V_{IN}		9.2		30	V
Supply Current	I_{IN}			0.930	1.500	mA
Line Regulation	$\Delta V_{OUT} / \Delta V_{IN}$	$V_{IN} = 9.2V$ to $30V$		8	20	ppm/V
Load Regulation	$\Delta V_{OUT} / \Delta I_{OUT}$	Sourcing: $0mA \leq I_{OUT} \leq 20mA$		10	20	ppm/mA
		Sinking: $-10mA \leq I_{OUT} \leq 0mA$		21	40	
Dropout Voltage ^[4]	V_D			1.5	1.7	V

- Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
- The V_{OUT} accuracy is based on die mount with Silver Glass die attach material such as QMI 2569 or equivalent in a package with an Alumina ceramic substrate.
- Over the specified temperature range. Temperature coefficient is measured by the box method whereby the change in $V_{OUT(max)} - V_{OUT(min)}$ is divided by the temperature range; in this case, $-55^\circ C$ to $+125^\circ C = +180^\circ C$.
- Dropout Voltage is the minimum $V_{IN} - V_{OUT}$ differential voltage measured at the point where V_{OUT} drops 1mV from $V_{IN} = \text{nominal}$ at $T_A = +25^\circ C$.

4. Typical Performance Curves

$V_{OUT} = 7.5V$, $T_A = +25^\circ C$, $C_{OUT} = 1\mu F$, $COMP = 1nF$, unless otherwise specified.

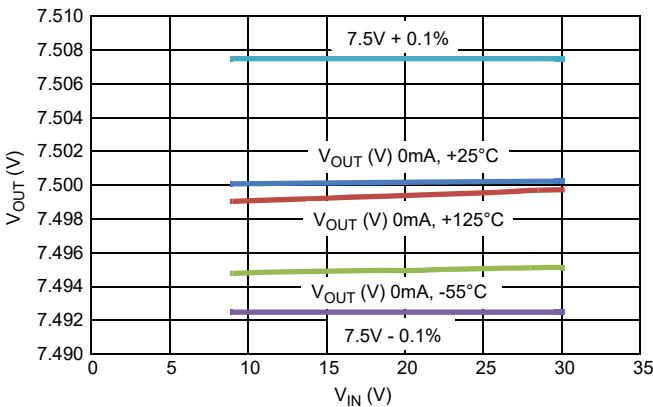


Figure 6. V_{OUT} Accuracy Over Temperature

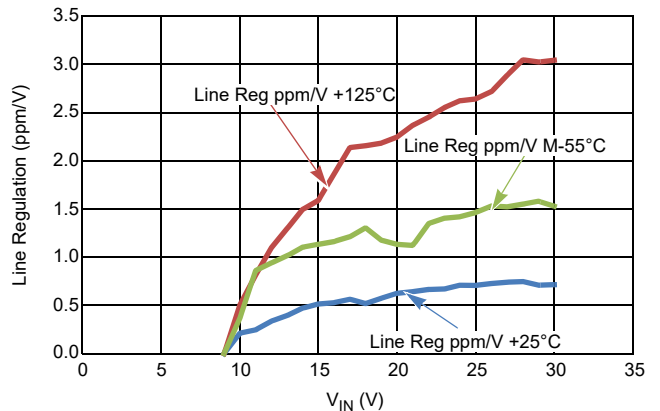


Figure 7. Line Regulation Over Temperature at $V_{IN} = 5V$ (ppm/mA)

$V_{OUT} = 7.5V$, $T_A = +25^\circ C$, $C_{OUT} = 1\mu F$, $COMP = 1nF$, unless otherwise specified. (Cont.)

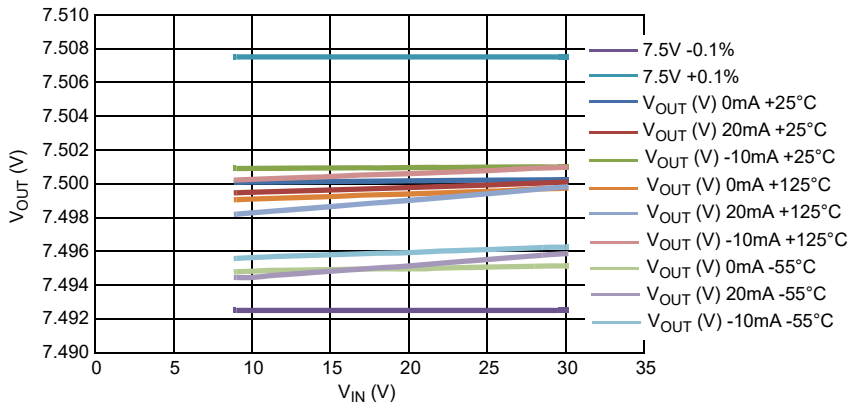


Figure 8. V_{OUT} vs V_{IN} at 0mA, 20mA and -10mA

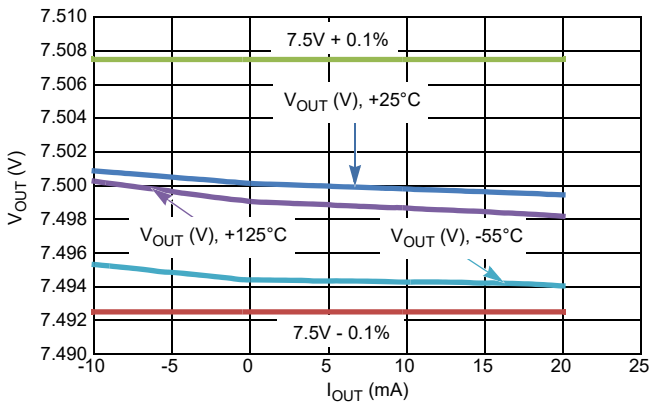


Figure 9. Load Regulation Over Temperature at $V_{IN} = 9.2V$

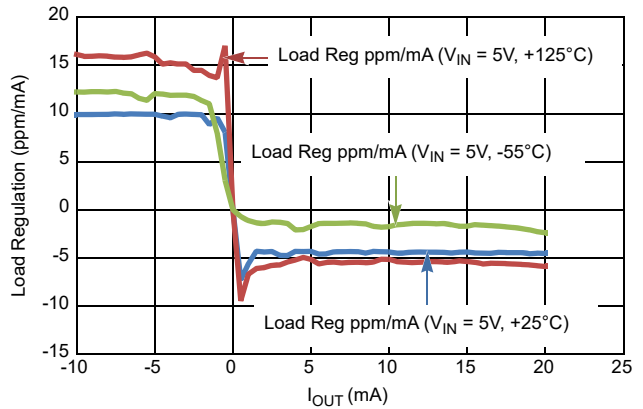


Figure 10. Load Regulation Over Temperature at $V_{IN} = 9.2V$ (ppm/mA)

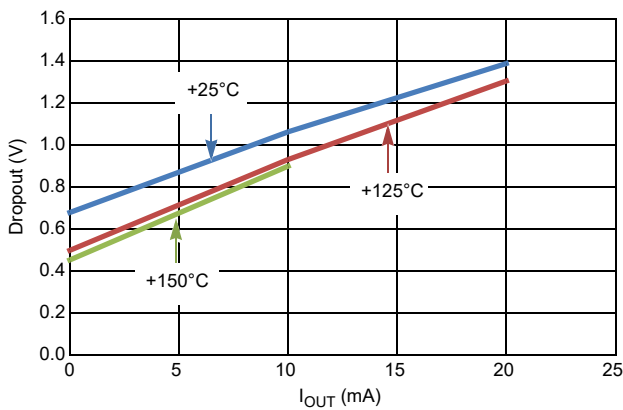


Figure 11. Dropout Voltage for 7.5V

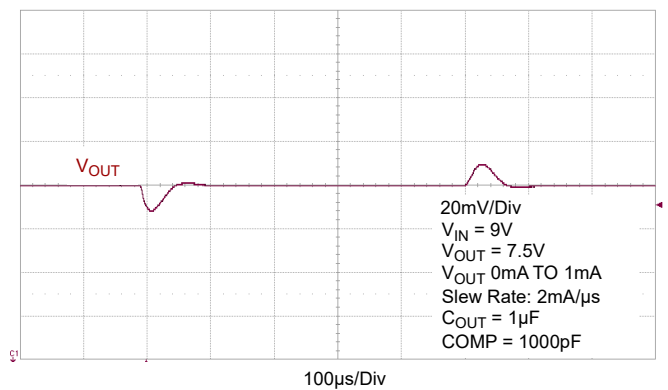


Figure 12. Load Transient 0 to 1mA

$V_{OUT} = 7.5V$, $T_A = +25^\circ C$, $C_{OUT} = 1\mu F$, $COMP = 1nF$, unless otherwise specified. (Cont.)

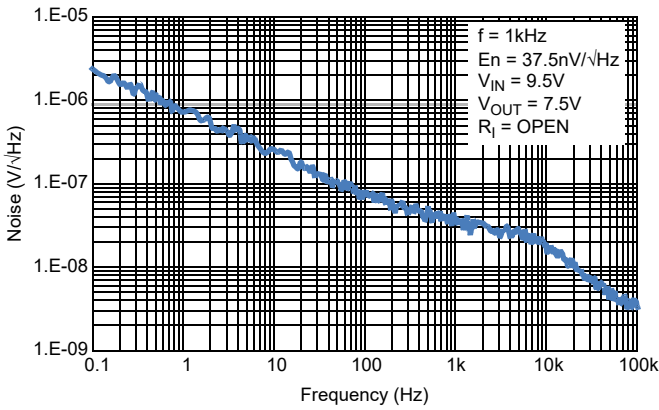


Figure 13. Noise Density vs Frequency ($V_{IN} = 9.5V$, $V_{OUT} = 7.5V$, $I_{OUT} = 0mA$)

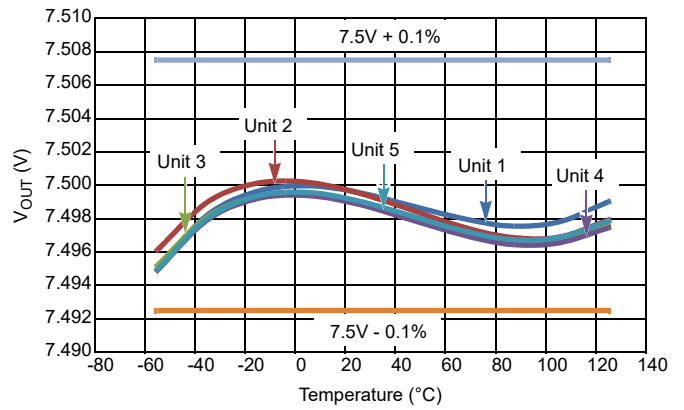


Figure 14. V_{OUT} vs Temperature

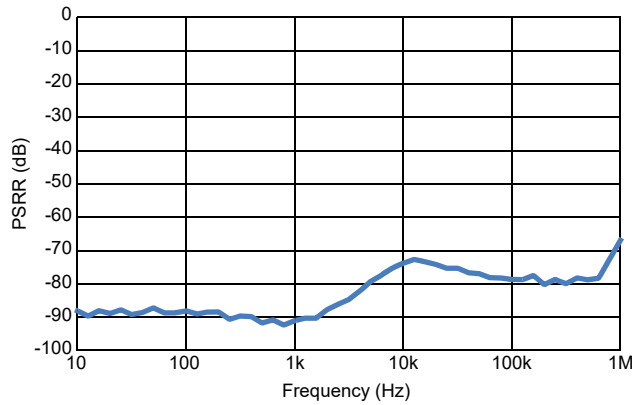


Figure 15. PSRR ($+25^\circ C$, $V_{IN} = 9.5V$, $V_{OUT} = 7.5V$, $I_{OUT} = 0mA$, $C_{IN} = 0.1\mu F$, $C_{OUT} = 1.0\mu F$, $COMP = 1nF$, $V_{SIG} = 300mV_{P-P}$)

5. Device Operation

5.1 Bandgap Precision Reference

The ISL71090SEH75 uses a bandgap architecture and special trimming circuitry to produce a temperature compensated, precision voltage reference with high input voltage capability and moderate output current drive.

6. Applications Information

6.1 Board Mounting Considerations

For applications requiring the highest accuracy, board mounting location should be reviewed. The device uses a ceramic flatpack package. Generally, mild stresses to the die when the Printed Circuit (PC) board is heated and cooled, can slightly change the shape. Because of these die stresses, placing the device in areas subject to slight twisting can cause degradation of reference voltage accuracy. It is normally best to place the device near the edge of a board, or on the shortest side, because the axis of bending is most limited in that location. Mounting the device in a cutout also minimizes flex. Obviously, mounting the device on flexprint or extremely thin PC material will likewise cause loss of reference accuracy.

6.2 Board Assembly Considerations

Some PC board assembly precautions are necessary. Normal output voltage shifts of typically 100 μ V can be expected with Pb-free reflow profiles or wave solder on multilayer FR4 PC boards. Precautions should be taken to avoid excessive heat or extended exposure to high reflow or wave solder temperatures.

6.3 Noise Performance and Reduction

The output noise voltage over the 0.1Hz to 10Hz bandwidth is typically 1.0 μ V_{P-P} ($V_{OUT} = 7.5V$). The noise measurement is made with a 9.9Hz bandpass filter. Noise in the 10Hz to 1kHz bandwidth is approximately 1.2 μ V_{RMS}, with 1 μ F capacitance on the output. This noise measurement is made with a bandpass filter of 990Hz. Load capacitance up to 10 μ F (with COMP capacitor listed in [Table 1](#)) can be added but will result in only marginal improvements in output noise and transient response.

6.4 Turn-On Time

Normal turn-on time is typically 250 μ s, the circuit designer must take this into account when looking at power-up delays or sequencing.

6.5 Temperature Coefficient

The limits stated for temperature coefficient (Tempco) are governed by the method of measurement. The overwhelming standard for specifying the temperature drift of a reference is to measure the reference voltage at two temperatures, which provide for the maximum voltage deviation and take the total variation, ($V_{HIGH} - V_{LOW}$), this is then divided by the temperature extremes of measurement ($T_{HIGH} - T_{LOW}$). The result is divided by the nominal reference voltage (at $T = +25^{\circ}C$) and multiplied by 10^6 to yield ppm/ $^{\circ}C$. This is the Box method for specifying temperature coefficient.

6.6 Output Voltage Adjustment

The output voltage can be adjusted above and below the factory-calibrated value via the trim terminal. The trim terminal is the negative feedback divider point of the output op amp. The voltage at the trim pin is set at approximately 1.216V by the internal bandgap and amplifier circuitry of the voltage reference. The suggested method to adjust the output is to connect a 1M Ω external resistor directly to the trim terminal and connect the other end to the wiper of a potentiometer that has a 100k Ω resistance and whose outer terminals connect to

V_{OUT} and ground. If a 1M Ω resistor is connected to trim, the output adjust range will be ± 6.3 mV. The TRIM pin should not have any capacitor tied to its output, also it is important to minimize the capacitance on the trim terminal during layout to preserve output amplifier stability. It is also best to connect the series resistor directly to the trim terminal to minimize that capacitance and also to minimize noise injection. Small trim adjustments will not disturb the factory-set temperature coefficient of the reference, but trimming near the extreme values can.

6.7 Output Stage

The output stage of the device has a push-pull configuration with an high-side PNP and a low-side NPN. This helps the device to act as a source and sink. The device can source 20mA.

6.8 Use of COMP Capacitor

The reference can be compensated for the C_{OUT} capacitors used by adding a capacitor from COMP pin to GND. See [Table 1](#) for recommended values. of the COMP capacitor.

Table 1. Recommended Values of COMP Capacitor

C _{OUT} (μ F)	C _{COMP} (nF)
0.1	1
1	1
10	10

6.9 SEE Testing

The SET result is based on the ISL71090SEH25. The ISL71090SEH25 and ISL71090SEH75 share the same active circuitry consisting of a precision bandgap circuit and a trimmable amplifier to set the output reference with only a resistor change to scale the output. The SET test was done under an ion beam having an LET of 86MeV \cdot cm²/mg. The device did not latch up or burn out to a V_{DD} of 36V and at +125°C. Single Event transients were observed and are summarized in the [Table 2](#):

Table 2. Observation of Single Event Transients

V _{IN} (V)	I _{OUT} (mA)	C _{OUT} (μ F)	SET (% V _{OUT})
4	5	1	-4.6
30	5	1	-4.4
30	5	10	-1.0

6.10 DNC Pins

These pins are for trimming purposes and for factory use only. Do not connect these to the circuit in any way. It will adversely effect the performance of the reference.

7. Package and Die Characteristics

Table 3. Die and Assembly Related Information

Die Information	
Dimensions	1464 μ m×1744 μ m (58 mils×69 mils) Thickness: 483 μ m \pm 25 μ m (19 mils \pm 1 mil)
Interface Materials	
Glassivation	Type: Nitrox Thickness: 15kÅ
Top Metallization	Type: AlCu (99.5%/0.5%) Thickness: 30kÅ
Backside Finish	Silicon
Process	Dielectrically Isolated Advanced Bipolar Technology- PR40 SOI
Assembly Information	
Substrate Potential	Floating
Additional Information	
Worst Case Current Density	<2×10 ⁵ A/cm ²
Transistor Count	182
Weight of Packaged Device	0.31 grams (Typical)
Lid Characteristics	Finish: Gold Potential: Connected to pin #4 (GND) Case Isolation to Any Lead: 20×10 ⁹ Ω (min)

7.1 Metallization Mask Layout

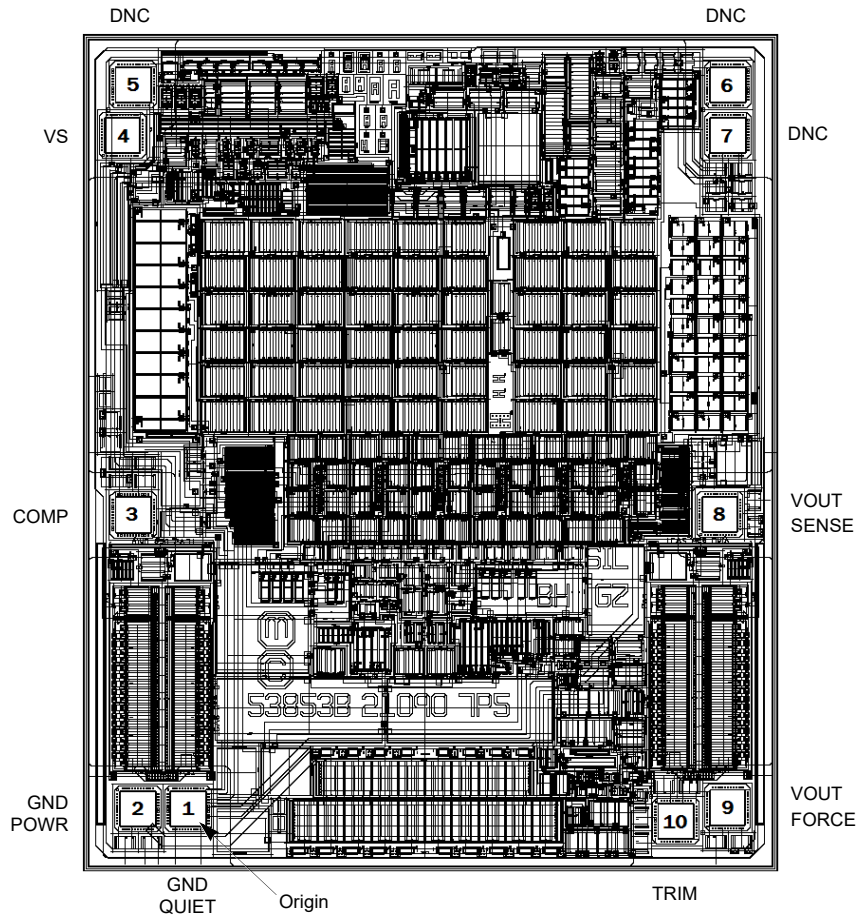


Table 4. Die Layout X-Y Coordinates

Pad Name	Pad Number	X (μm)	Y (μm)	Bond Wires Per Pad ^[1]
GND PWR	2	-104	0	1
GND QUIET ^[2]	1	0	0	1
COMP	3	-108	589	1
VS	4	-125	1350	1
DNC	5	-108	1452	1
DNC	6	1089	1452	1
DNC	7	1089	1350	1
VOUT SENSE	8	1072	598	1
VOUT FORCE	9	1088	1	1
TRIM	10	985	-25	1

1. Bond wire size is 1.0 mil.

2. Origin of coordinates is the centroid of GND QUIET.

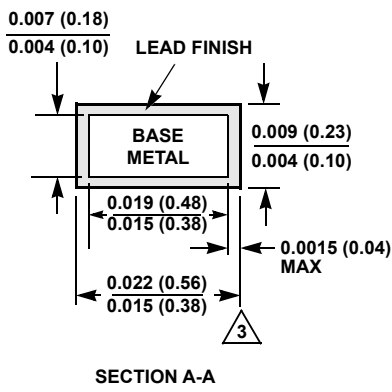
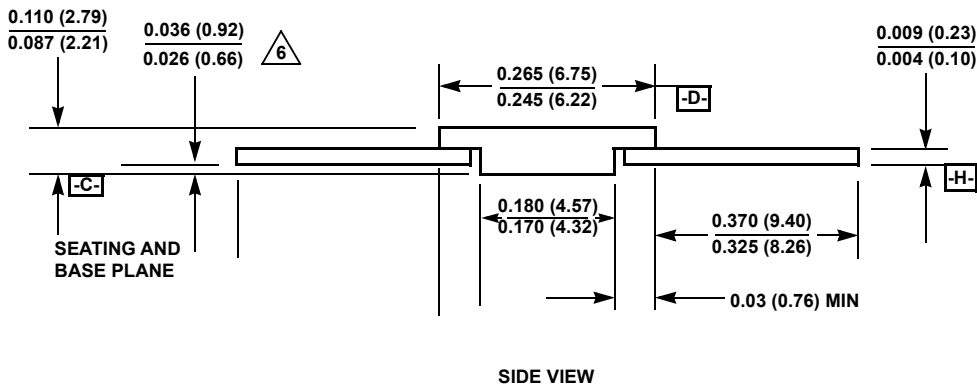
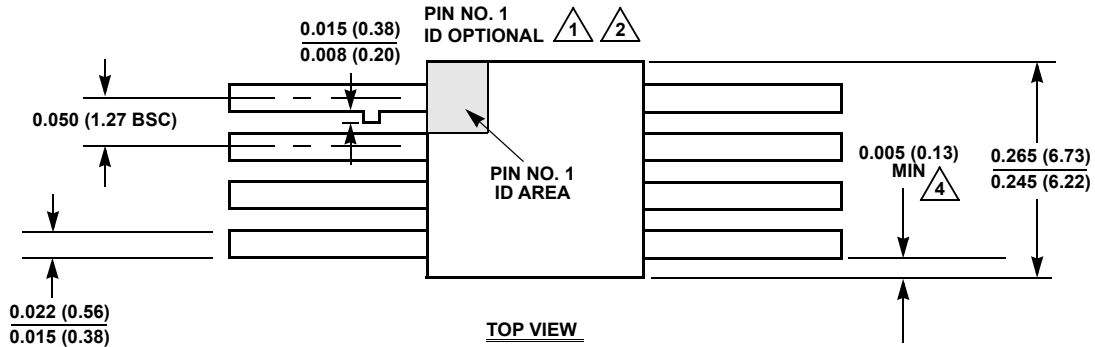
8. Package Outline Drawing

For the most recent package outline drawing, see [K8.A](#).

K8.A

8 Lead Ceramic Metal Seal Flatpack Package

Rev 4, 12/14



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to or instead of a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

9. Ordering Information

SMD Ordering Number ^[1]	Part Number ^[2]	V _{OUT} Option (V)	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	PKG. DWG. #	Carrier Type	Temp Range
5962R1321104VXC	ISL71090SEHVF75	7.5	HDR to 100krad(Si), LDR to 50krad(Si)	8 Ld Flatpack	K8.A	Tray	-55 to +125°C
N/A	ISL71090SEHF75/PROTO ^[3]		N/A				
5962R1321104V9A	ISL71090SEHVX75 ^[4]		HDR to 100krad(Si), LDR to 50krad(Si)	Die	-	-	
N/A	ISL71090SEHX75SAMPLE ^{[3][4]}		N/A				
N/A	ISL71090SEH75EV1Z ^[5]		Evaluation Board				

- Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed must be used when ordering.
- These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
- The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
- Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in [Electrical Specifications](#).
- Evaluation board uses the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Table 5. Key Differences Between Family of Parts

Part Number	V _{OUT} (V)	TEMPCO (ppm/°C)	Output Voltage Noise (μV _{P-P})	Load Regulation (ppm/mA)
ISL71090SEH12	1.25	10	1	35
ISL71090SEH25	2.5	10	2	2.5
ISL71090SEH50	5.0	10	1.1	10
ISL71090SEH75	7.5	10	1	10

10. Revision History

Revision	Date	Description
4.02	Sept 29, 2023	Applied new template formatting throughout. Updated Radiation Acceptance Tested feature bullets. Added Figure 4. Updated Note 1 in Abs Max section.
4.01	Jan 21, 2022	Updated Figure 9.
4.00	May 14, 2021	Updated the Radiation Features bullet. Updated Ordering Information table formatting and added Notes 3, 4, and 5. Added the Transistor Count to the Assembly Related Information. Removed Related Literature and About Intersil sections.

Revision	Date	Description
3.00	Mar 18, 2016	<ul style="list-style-type: none"> -Changed title from "Radiation Hardened Ultra Low Noise, Precision Voltage Reference" to "7.5V Radiation Hardened Ultra Low Noise, Precision Voltage Reference" -Updated Related Literature document titles to match titles on the actual documents. -Added Table 5. -Corrected the Evaluation board part number in the Ordering Information table. -On page 6: <ul style="list-style-type: none"> -Changed Electrical Specification for Flatpack note from: "Boldface limits apply over the operating temperature range, -55°C to +125°C and radiation." to: "Boldface limits apply after radiation at +25°C or across the operating temperature range, -55°C to +125°C without radiation, unless otherwise specified. -For parameter VOA (row 4) in Electrical Specifications for Flatpack table changed description from: "VOUT Accuracy, Post Rad", to: "VOUT Accuracy at TA = +25°C, Post radiation" and for parameters VOA (rows 2, 3, 4) added "Note 9" to Conditions column. -On page 7: <ul style="list-style-type: none"> -Changed Electrical Specification for Die note from: "Boldface limits apply over the operating temperature range, -55°C to +125°C and radiation." To: "Boldface limits apply after radiation at +25°C or across the operating temperature range, -55°C to +125°C without radiation, unless otherwise specified. -For parameter VOA (row 4) in Electrical Specifications for Die table changed description from: "VOUT Accuracy, Post Rad", to: "VOUT Accuracy at TA = +25°C, Post radiation" and for parameters VOA for Post radiation (row 4) added "Note 11" to Conditions column. -Updated POD K8.A to the latest revision changes are as follows: <ul style="list-style-type: none"> Modified Note 2 by adding the words "...in addition to or instead of..."
2.00	Dec 2, 2013	Electrical spec table (Flatpack) and (Die): V _{OUT} Accuracy Post Rad section, changed the value for Min from -0.25% to -0.3% and Max from +0.25% to +0.3%.
1.00	Oct 4, 2013	Initial Release.

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