RNA53A27F

System Organizer IC for Dedicate Microcomputer

Description

RNA53A27F is reset function and reference voltage output for microcontroller has been installed.

Provide support for Renesas MCU operation.

Features

- Reset detection voltage: 2.745 V ± 1%
- Standard voltage: 3.050 V ± 0.8%
- Delay time: 50,100 ms (fine regulation by resistance is possible)
- Corresponds to manual reset
- Sleep mode is installed

## Ordering Information

| Part Name	Package Type	Package Code	Package Abbreviation	Taping Abbreviation (Quantity)	Surface Treatment
RNA53A27FUSH1	SSOP-8	PVSP0008KA-A	US	H (3,000 pcs/reel)	1 (Sn/Bi)

Application

- Power supply voltage monitoring for microprocessors
- Computers and notebook computers
- Digital still camera, digital video camera, and PDA

Block Diagram
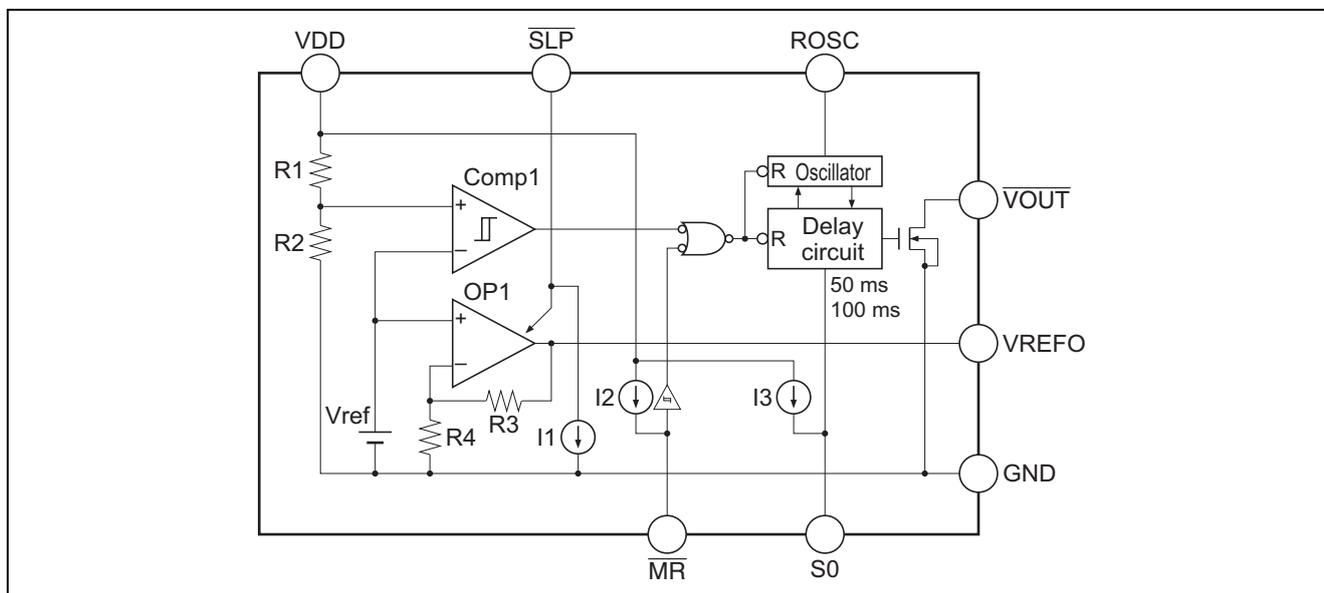
Timing Chart

Pin Arrangement

```
         ROSC ⊏  1        8  ⊐ S0
          SLP ⊏  2        7  ⊐ VDD
           MR ⊏  3        6  ⊐ VREFO
          GND ⊏  4        5  ⊐ VOUT
```

(Top view)
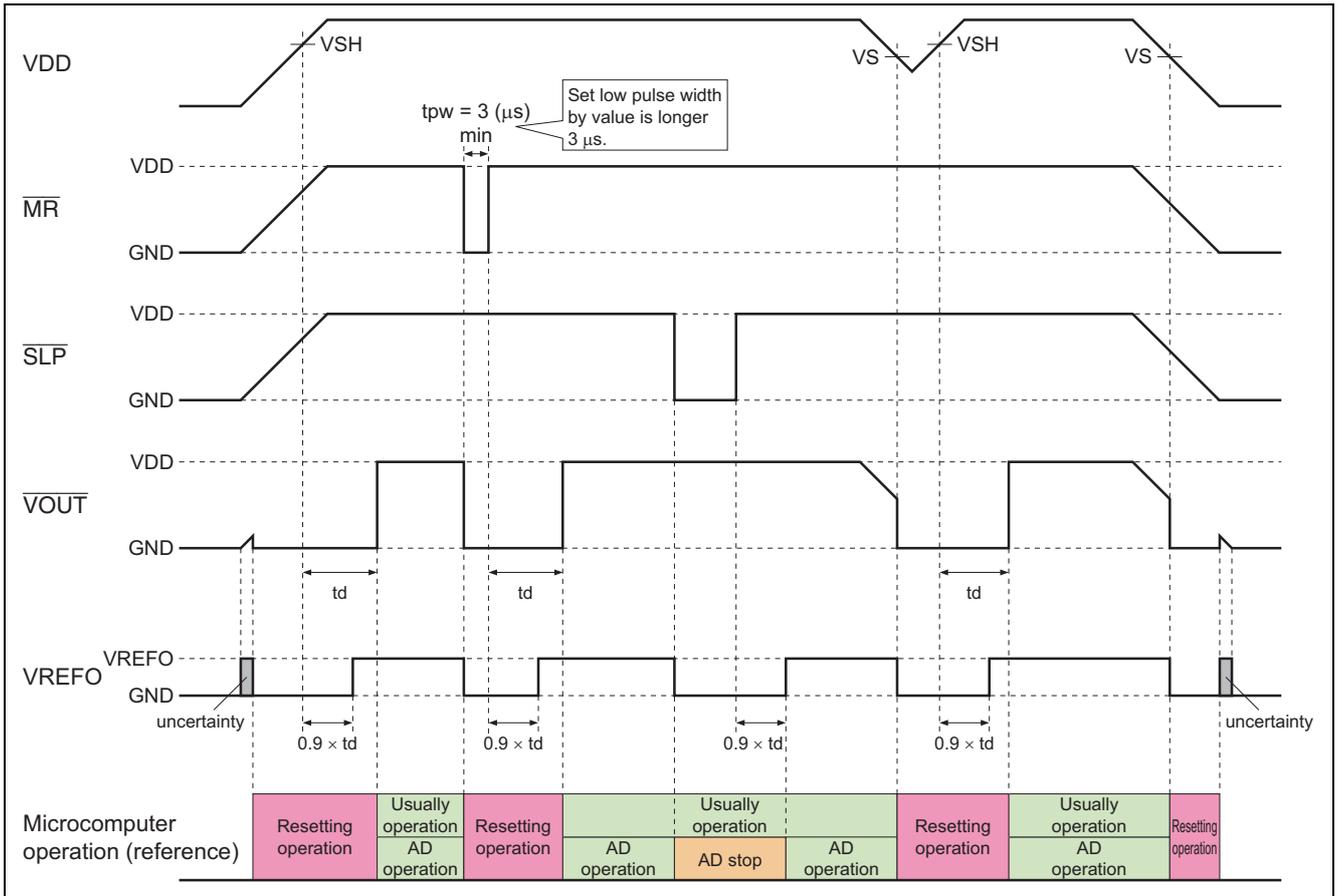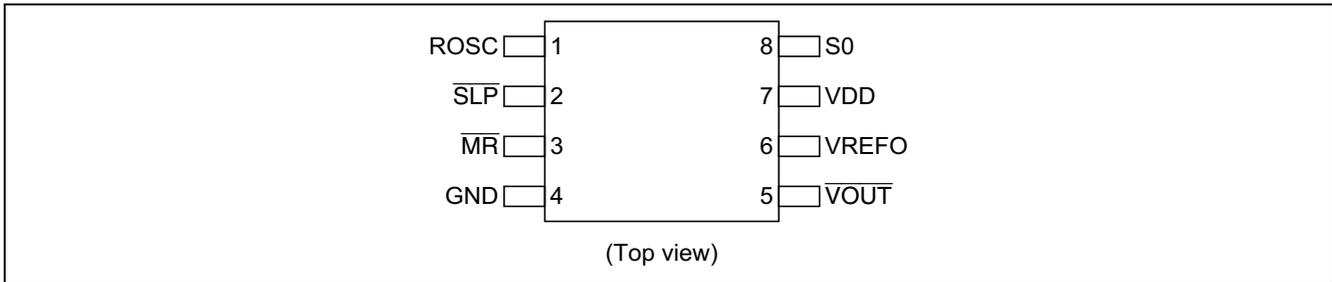
Mark Indication
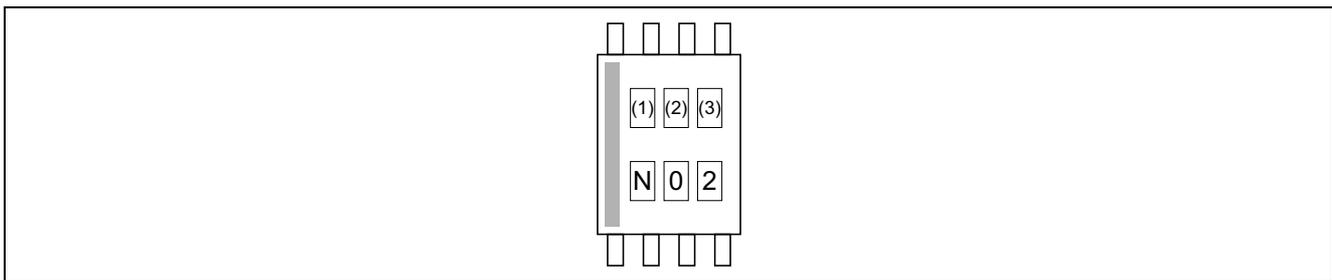
(1)	Year code	The last digit of year
(2)	Month code	Starting in January "A", "B", "C", "D", "E", "F", "G", "H", "J", "K", "L", "M"
(3)	Week code	View week of month, 1 week → "1"

Pin Description

Pin No.	Terminal Marking	Terminal Name	I/O	Function
1	ROSC	Oscillation control resistance installation terminal	—	• 1.1 MΩ is installed between GND usually. • Delay adjustment range of resistance: 650(kΩ) to 1.35(MΩ)
2	SLP	Sleep mode control	I	• L: Sleep mode (Power-supply current becomes several μA) • H: Usually mode • Terminal is open, Pull-down in GND
3	MR	Manual reset input	I	• Low is input, 5pin(VOUT) output the low level Set the low pulse width by value is longer 3 μs • Terminal open, pull-up in VDD
4	GND	GND	—	• Sorcing 0 V.
5	VOUT	Reset output	O	• Power-supply voltage reaches the value below the detection voltage, low is output • Low level is input to MR terminal, low is output • Open drain output • Range pull-up resistance: 10(kΩ) to 100(kΩ)
6	VREFO	Standard voltage output	O	• Standard voltage (3.05 V typ) for AD/DA is output • Outside puts capacity (0.1 μF) by pursuant for microcomputer
7	VDD	Power-supply terminal	—	• Sorcing power-supply voltage.
8	S0	Delay time switch	I	• Delay time is switched. Low: 50 (ms), High: 100 (ms) • Terminal is open, pull-up in Vdd

Absolute Maximum Ratings

| Item	Symbol	Ratings	Unit
Supply voltage	VDD	6.5	V
Output voltage (open-drain type)	Vout	−0.3 to +6.5	V
Input voltage	Vin	−0.3 to VDD	V
Output current	Iout	10	mA
Standard voltage terminal source current	IREF	5	mA
Continuous power dissipation	Pd	160 (Ta = 25°C)	mW
Operating temperature	Topr	−40 to +85	°C
Storage temperature	Tstg	−55 to +125	°C

Electrical Characteristics

(Vdd = 3.3 V, Ta = 25°C, unless otherwise noted)

| Item	Symbol	Min	Typ	Max	Unit	Test Conditions
Output fixation voltage	VOUL	—	—	0.9	V	$\overline{VOUT}$ terminal, RL = 10 (kΩ)
Operating limit voltage	VOPM	2.7	—	—	V	
Current consumption	Idd	—	100	200	μA	Vdd = 3.3 V, $\overline{SLP}$ = Hi (Vdd)
Standing circuit current	IddSLP	—	2.8	5.6	μA	$\overline{SLP}$ = Low (GND), $\overline{MR}$ = Hi (Vdd), $\overline{S0}$ = Hi (Vdd)
Detecting voltage	VS	2.718	2.745	2.772	V	
Detecting voltage temperature coefficient	Vs/ΔT	—	±100	—	ppm/°C	
Hysteresis voltage	VHYS	VS×0.03	VS×0.05	VS×0.08	V	
Standard voltage	VREF	3.026	3.050	3.074	V	Vdd ≥ 3.3 V, Isource = 0 to 3 mA, CL = 0.1 μF
Standard voltage temperature coefficient	VREF/ΔT	—	±100	—	ppm/°C	
Standard voltage return time	VRCV	—	—	0.9×td	ms	
Output low voltage	VOL	—	0.3	0.54	V	$\overline{VOUT}$, Isink = 4 mA, Vdd = 2.6 (V)
Output leakage current	ILK	—	—	100	nA	$\overline{VOUT}$, Vdd = 3.6 V
Minimum pulse width	tpw	3	—	—	μs	MR terminal input
Delay time	td	35	50	65	ms	S0 = Low
		70	100	130	ms	S0 = High
Reactive time	tPHL	—	6	—	μs	VDD drop to time until outputting $\overline{VOUT}$ $\overline{MR}$ input to time until outputting $\overline{VOUT}$
High input voltage	VIH	Vdd×0.8	—	Vdd	V	$\overline{MR}$ terminal, $\overline{SLP}$ terminal, S0 terminal, Vdd = 3.0 V to 3.6 V
Low input voltage	VIL	0	—	Vdd×0.2	V	$\overline{MR}$ terminal, $\overline{SLP}$ terminal, S0 terminal, Vdd = 3.0 V to 3.6 V
S0 terminal pull-up current	IPUS0	—	—	0.5	μA	S0 terminal
$\overline{MR}$ terminal pull-up current	IPUMR	1.5	3	6	μA	$\overline{MR}$ terminal
$\overline{SLP}$ terminal pull-down current	IPDSLP	—	—	0.5	μA	$\overline{SLP}$ terminal

Example of Application Circuit

[Application Example1]

Such t_{WL1} > t_{WL2}, (1) recommend set a longer pulse width.
Low pulse between two is recommended set to overlap.

[Application Example2]
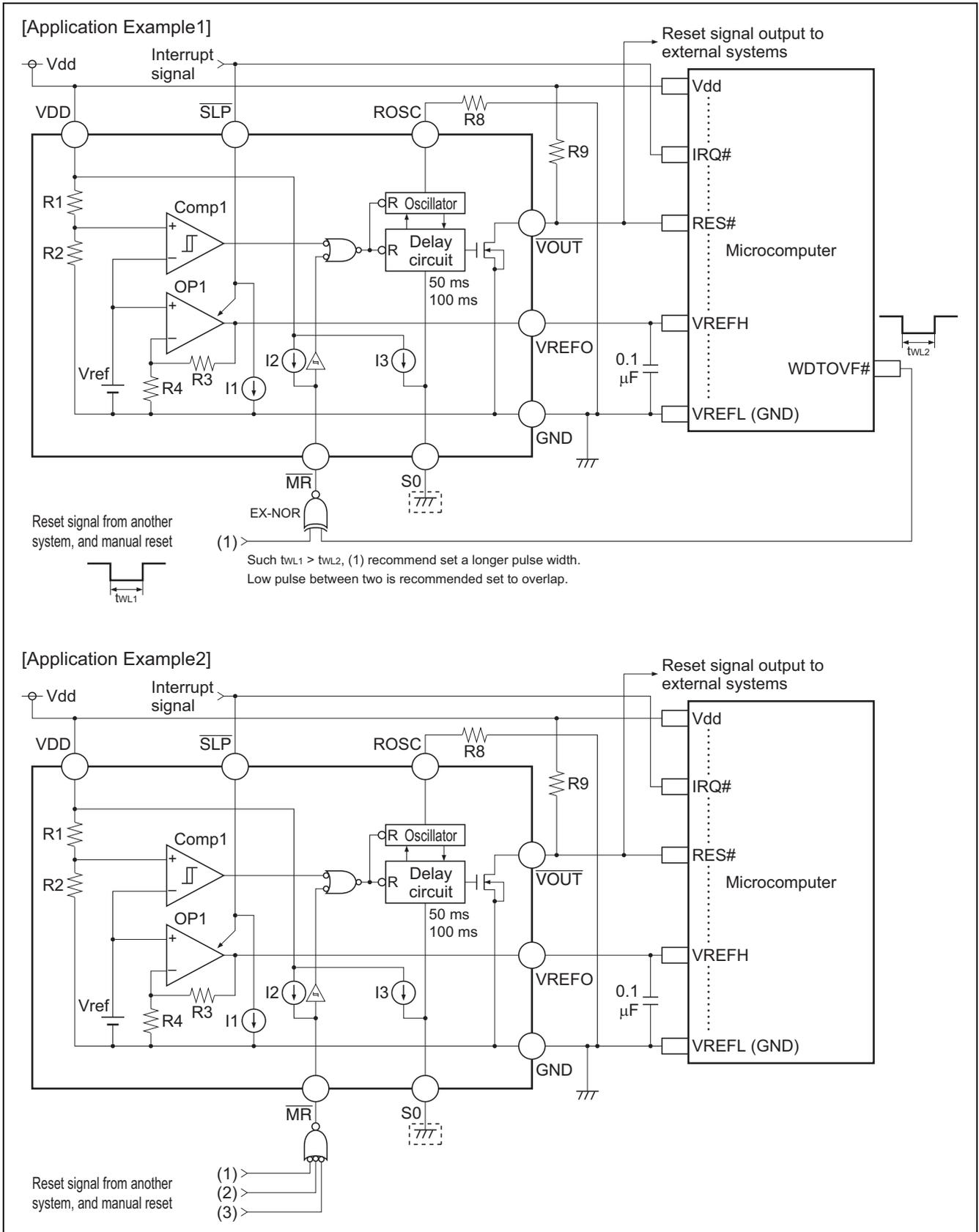
Package Dimensions

JEITA Package Code	RENESAS Code	Previous Code	MASS[Typ.]
P-VSSOP8-2.3x2-0.50	PVSP0008KA-A	TTP-8DB/TTP-8DBV	0.010g
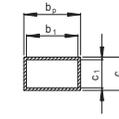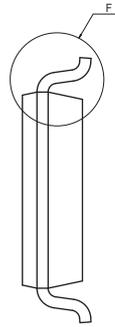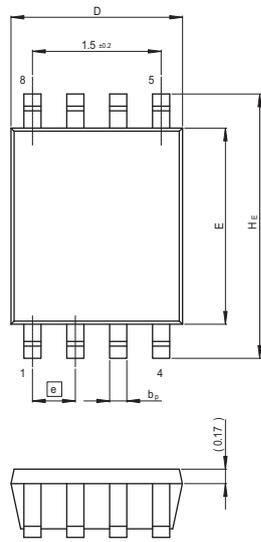
Terminal cross section
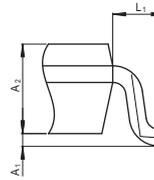
Detail F

Reference Symbol	Dimension in Millimeters		
	Min	Nom	Max
D	1.8	2.0	2.2
E	2.2	2.3	2.4
A_2	0.6	0.7	0.8
A_1	0	——	0.1
A	——	——	——
b_p	0.15	0.22	0.3
b_1	——	0.20	——
c	0.08	0.13	0.23
c_1	——	0.11	——
θ	——	——	——
H_E	2.8	3.1	3.4
e	——	(0.5)	——
x	——	——	——
y	——	——	——
Z	——	——	——
L	——	——	——
L_1	——	(0.4)	——

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