IS-139ASRH, IS-139ASEH

Single Event Radiation Hardened Quad Voltage Comparators

FN9000
Rev 4.00
April 6, 2012

The single event effects and total dose radiation hardened IS-139ASRH, IS-139ASEH consist of four independent single or dual supply voltage comparators on a single monolithic substrate. The common mode input voltage range includes ground, even when operated from a single supply, and the low supply current makes these comparators suitable for low power applications. These types were designed to directly interface with TTL and CMOS inputs.

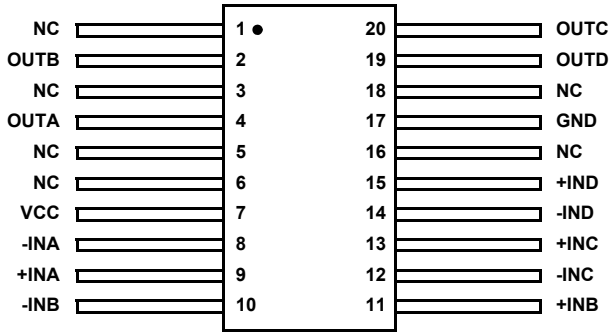
The IS-139ASRH, IS-139ASEH are fabricated on our dielectrically isolated Rad Hard Silicon Gate (RSG) process, which provides immunity to single event latch-up and the capability of highly reliable performance in any radiation environment.

Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed below must be used when ordering.

Detailed Electrical Specifications for the IS-139ASRH, IS-139ASEH are contained in SMD 5962-01510.

Pin Configuration

IS9-139ASRH, IS9-139ASEH
(FLATPACK CDFP4-F20)
TOP VIEW



Features

- Electrically Screened to SMD # 5962-01510
- QML Qualified per MIL-PRF-38535 Requirements
- Radiation Hardness
  - Total Dose . . . . . 300krad(Si) (Max)
  - Single Event Latch-up . . . . . >84MeV/mg/cm^2
  - Single Event Upset . . . . . >84MeV/mg/cm^2
- Operating Supply Voltage Range . . . . . 9V to 30V
- Input Offset Voltage (V_{IO}) . . . . . 5mV (Max)
- Quiescent Supply Current . . . . . 3mA (Max)
- Differential Input Voltage Range Equal to the Supply Voltage

Applications

- DC-DC Power Conversion
- Pulse Generators
- Timing Circuitry
- Level Shifting
- Analog to Digital Conversion

Ordering Information

ORDERING NUMBER	INTERNAL MKT. NUMBER	TEMP. RANGE (°C)	PACKAGE DRAWING NUMBER
5962F0151001VXC	IS9-139ASRH-Q	-55 to +125	K20.A
5962F0151001QXC	IS9-139ASRH-8	-55 to +125	K20.A
5962F0151002VXC	IS9-139ASEH-Q	-55 to +125	K20.A
IS9-139ASRH/PROTO	IS9-139ASRH/PROTO	-55 to +125	K20.A

Die Characteristics

DIE DIMENSIONS

3750µm x 4510µm (148 mils x 178 mils)
483µm ± 25.4µm (19 mils ± 1 mil)

INTERFACE MATERIALS

Glassivation

Type: Silox (SiO_2)
Thickness: 8.0kÅ ± 1.0kÅ

Top Metallization

Type: AlSiCu
Thickness: 16.0kÅ ± 2kÅ

Substrate

Radiation Hardened Silicon Gate, Dielectric Isolation

Backside Finish

Silicon

ASSEMBLY RELATED INFORMATION

Substrate Potential

Unbiased (DI)

ADDITIONAL INFORMATION

Worst Case Current Density

$<2.0 \times 10^5$ A/cm^2

Transistor Count

644

Metallization Mask Layout

IS-139ASRH, IS-139ASEH