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April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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SuperH™ Family E10A-USB Emulator

Additional Document for User's Manual Supplementary Information on Using the SH7338

Renesas Microcomputer Development
Environment System
SuperH™ Family

E10A-USB for SH7338 HS7338KCU01HE

Renesas Electronics
www.renesas.com

Rev.1.00   2005.07

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Section 1   Connecting the Emulator with the User System

1.1   Components of the Emulator

The E10A-USB emulator supports the SH7338. Table 1.1 lists the components of the emulator.

Table 1.1   Components of the Emulator

Classi-fication	Component	Appearance	Quan-tity	Remarks
Hard-ware	Emulator box		1	HS0005KCU01H: Depth: 65.0 mm, Width: 97.0 mm, Height: 20.0 mm, Mass: 72.9 g or HS0005KCU02H: Depth: 65.0 mm, Width: 97.0 mm, Height: 20.0 mm, Mass: 73.7 g
	User system interface cable		1	14-pin type: Length: 20 cm, Mass: 33.1 g
	User system interface cable		1	36-pin type: Length: 20 cm, Mass: 49.2 g (only for HS0005KCU02H)
	USB cable		1	Length: 150 cm, Mass: 50.6 g
Soft-ware	E10A-USB emulator setup program, SuperH™ Family E10A-USB Emulator User's Manual, Supplementary Information on Using the SH7338*, and Test program manual for HS0005KCU01H and HS0005KCU02H		1	HS0005KCU01SR, HS0005KCU01HJ, HS0005KCU01HE, HS7338KCU01HJ, HS7338KCU01HE, HS0005TM01HJ, and HS0005TM01HE (provided on a CD-R)
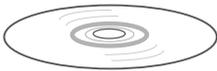
Note: Additional document for the MPUs supported by the emulator is included. Check the target MPU and refer to its additional document.

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1.2　Connecting the Emulator with the User System

To connect the E10A-USB emulator (hereinafter referred to as the emulator), the H-UDI port connector must be installed on the user system to connect the user system interface cable. When designing the user system, refer to the recommended circuit between the H-UDI port connector and the MPU. In addition, read the E10A-USB emulator user's manual and hardware manual for the related device.

Table 1.2 shows the type number of the emulator, the corresponding connector type, and the use of AUD function.

Table 1.2　Type Number, AUD Function, and Connector Type

Type Number	Connector	AUD Function
HS0005KCU02H	36-pin connector	Available
HS0005KCU01H, HS0005KCU02H	14-pin connector	Not available

The H-UDI port connector has the 36-pin and 14-pin types as described below. Use them according to the purpose of the usage.

1. 36-pin type (with AUD function)
   The AUD trace function is supported. A large amount of trace information can be acquired in realtime. The window trace function is also supported for acquiring memory access in the specified range (memory access address or memory access data) by tracing.
2. 14-pin type (without AUD function)
   The AUD trace function cannot be used because only the H-UDI function is supported. Since the 14-pin type connector is smaller than the 36-pin type (1/2.5), the area where the connector is installed on the user system can be reduced.

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1.3 Installing the H-UDI Port Connector on the User System

Table 1.3 shows the recommended H-UDI port connectors for the emulator.

Table 1.3   Recommended H-UDI Port Connectors

Connector	Type Number	Manufacturer	Specifications
36-pin connector	DX10M-36S	Hirose Electric Co., Ltd.	Screw type
	DX10M-36SE, DX10G1M-36SE		Lock-pin type
14-pin connector	2514-6002	Minnesota Mining & Manufacturing Ltd.	14-pin straight type

Note: When designing the 36-pin connector layout on the user board, do not connect any components under the H-UDI connector. When designing the 14-pin connector layout on the user board, do not place any components within 3 mm of the H-UDI port connector.

1.4 Pin Assignments of the H-UDI Port Connector

Figures 1.1 and 1.2 show the pin assignments of the 36-pin and 14-pin H-UDI port connectors, respectively.

Note: Note that the pin number assignments of the H-UDI port connector shown on the following pages differ from those of the connector manufacturer.

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Pin No.	Signal	Input/Output *1	SH7338 Pin No.	Note	Pin No.	Signal	Input/Output *1	SH7338 Pin No.	Note
1	AUDCK	Output	Y13		19	TMS	Input	W15	
2	GND	——			20	GND	——		
3	AUDATA0	Output	AA14		21	/TRST *2	Input	W14	
4	GND	——			22	(GND) *4	——		
5	AUDATA1	Output	V14		23	TDI	Input	V15	
6	GND	——			24	GND	——		
7	AUDATA2	Output	AB14		25	TDO	Output	Y14	
8	GND	——			26	GND	——		
9	AUDATA3	Output	W13		27	/ASEBRK /BRKACK *2	Input/output	AA13	
10	GND	——			28	GND	——		
11	/AUDSYNC *2	Output	V13		29	UVCC	Output		
12	GND	——			30	GND	——		
13	NC	——			31	/RESETP *2	Output	V16	User reset
14	GND	——			32	GND	——		
15	NC	——			33	GND *3	Output		
16	GND	——			34	GND	——		
17	TCK	Input	AB15		35	NC	——		
18	GND	——			36	GND	——		

Notes: 1. Input to or output from the user system.
2. The slash (/) means that the signal is active-low.
3. The emulator monitors the GND signal of the user system and detects whether or not the user system is connected.
4. When the user system interface cable is connected to this pin and the MPMD pin is set to 0, do not connect to GND but to the MPMD pin directly.
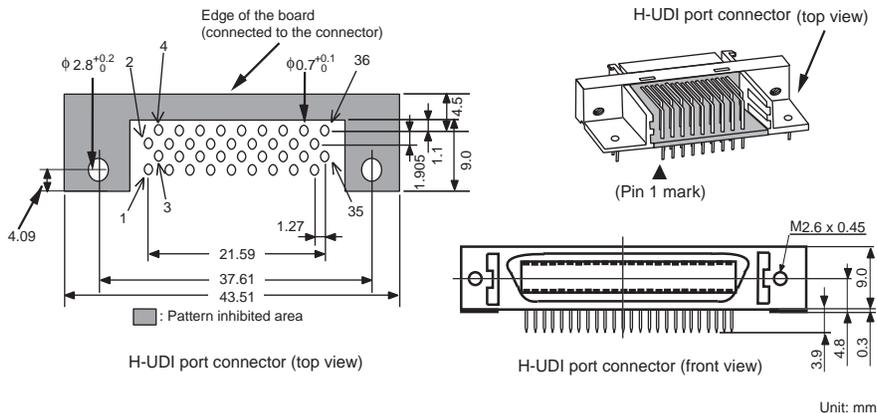
Figure 1.1 Pin Assignments of the H-UDI Port Connector (36 Pins)

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Pin No.	Signal	Input/Output*1	SH7338 Pin No.	Note
1	TCK	Input	AB15	
2	/TRST *2	Input	W14	
3	TDO	Output	Y14	
4	/ASEBRK /BRKACK *2	Input/output	AA13	
5	TMS	Input	W15	
6	TDI	Input	V15	
7	/RESETP *2	Output	V16	User reset
8	N.C.		——	
9	(GND) *4		——	
11	UVCC	Output		
10, 12, and 13	GND		——	
14	GND *3	Output		

Notes: 1. Input to or output from the user system.
2. The slash (/) means that the signal is active-low.
3. The emulator monitors the GND signal of the user system and detects whether or not the user system is connected.
4. When the user system interface cable is connected to this pin and the MPMD pin is set to 0, do not connect to GND but to the MPMD pin directly.
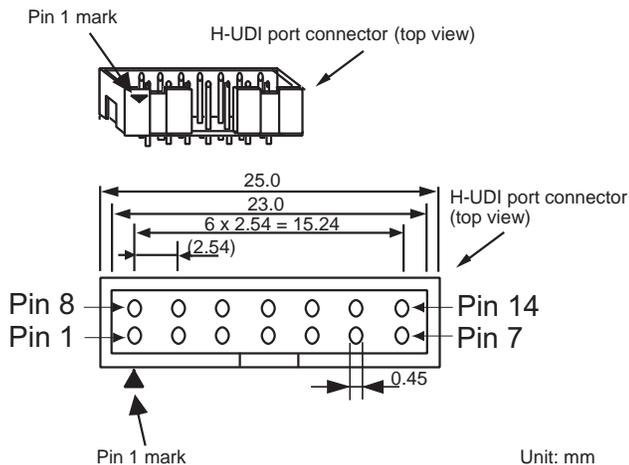
Figure 1.2   Pin Assignments of the H-UDI Port Connector (14 Pins)

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1.5 Recommended Circuit between the H-UDI Port Connector and the MPU

1.5.1 Recommended Circuit (36-Pin Type)

Figure 1.3 shows a recommended circuit for connection between the H-UDI and AUD port connectors (36 pins) and the MPU when the emulator is in use.

Notes: 1. Do not connect anything to the N.C. pins of the H-UDI port connector.

2. The MPMD pin must be 0 when the emulator is connected and 1 when the emulator is not connected, respectively.
   (1) When the emulator is used: MPMD = 0
   (2) When the emulator is not used: MPMD = 1
   Figures 1.3 shows an examples of circuits that allow the MPMD pin to be GND (0) whenever the emulator is connected by using the user system interface cable.

3. When a network resistance is used for pull-up, it may be affected by a noise. Separate TCK from other resistances.

4. The /TRST pin must be at the low level for a certain period when the power is supplied whether the H-UDI is used or not. Reduce the power supplied to the /TRST pin by pulling the pin down by a resistance of 1 kilo-ohm and setting PUL15 = 0 in the PULCR register after a reset.

5. The pattern between the H-UDI port connector and the MPU must be as short as possible. Do not connect the signal lines to other components on the board.

6. Since the H-UDI and the AUD of the MPU operate with the Vcc, supply only the Vcc to the UVCC pin. Make the emulator's switch settings so that the user power will be supplied (SW2 = 1 and SW3 = 1).

7. The resistance values shown in figure 1.3 are reference.

8. For the pin processing in cases where the emulator is not used, refer to the hardware manual of the related MPU.

9. For the AUDCK pin, guard the pattern between the H-UDI port connector and the MPU at GND level.

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When the circuit is connected as shown in figure 1.3, the switches of the emulator are set as SW2 = 1 and SW3 = 1. For details, refer to section 3.8, Setting the DIP Switches, in the SuperH™ Family E10A-USB Emulator User's Manual.
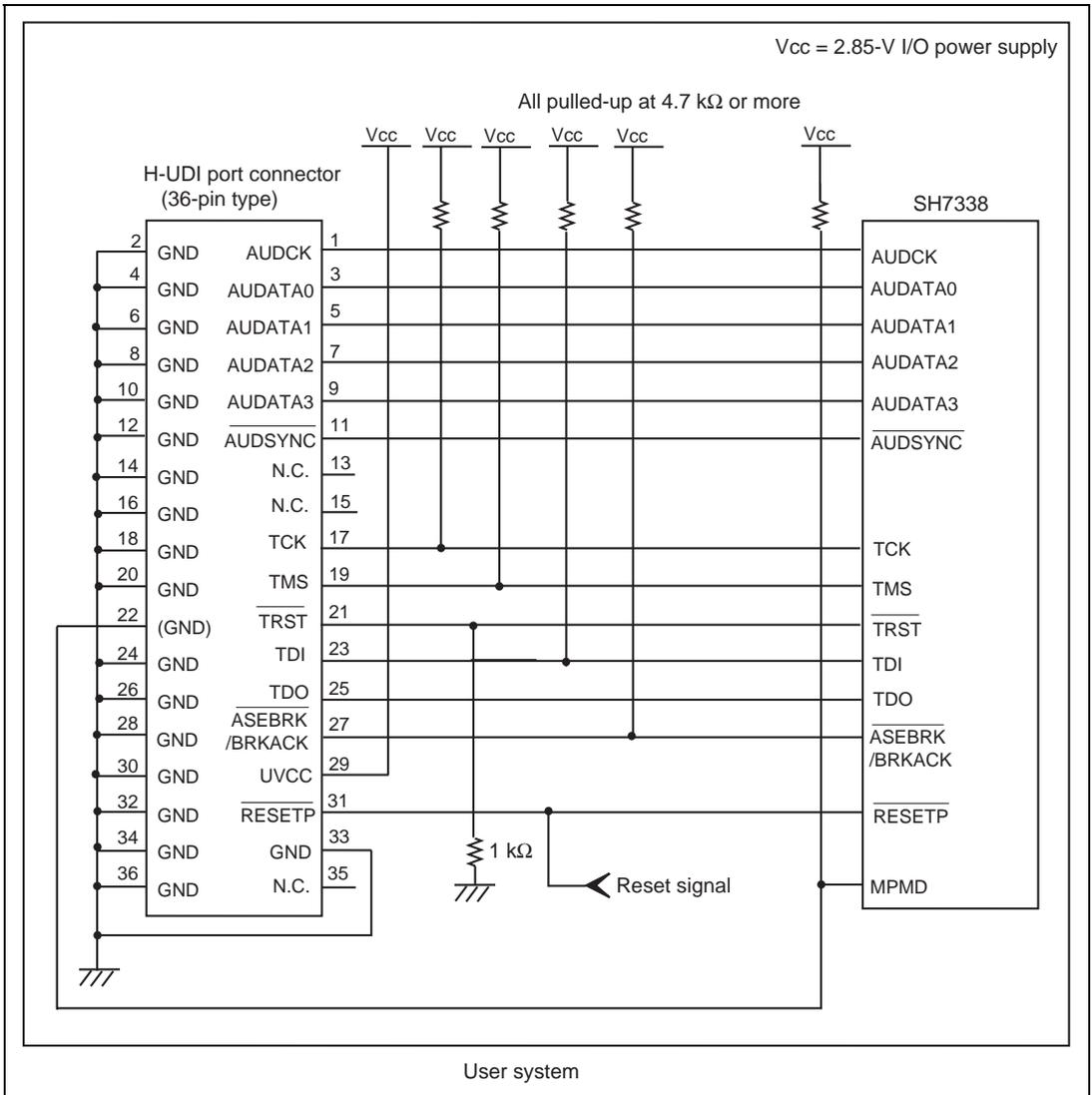
Figure 1.3   Recommended Circuit for Connection between the H-UDI Port Connector and MPU when the Emulator is in Use (36-Pin Type)

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1.5.2   Recommended Circuit (14-Pin Type)

Figure 1.4 shows a recommended circuit for connection between the H-UDI and AUD port connectors (14 pins) and the MPU when the emulator is in use.

Notes: 1. Do not connect anything to the N.C. pins of the H-UDI port connector.
2. The MPMD pin must be 0 when the emulator is connected and 1 when the emulator is not connected, respectively.
(1) When the emulator is used: MPMD = 0
(2) When the emulator is not used: MPMD = 1
Figures 1.3 shows an examples of circuits that allow the MPMD pin to be GND (0) whenever the emulator is connected by using the user system interface cable.
3. When a network resistance is used for pull-up, it may be affected by a noise. Separate TCK from other resistances.
4. The /TRST pin must be at the low level for a certain period when the power is supplied whether the H-UDI is used or not. Reduce the power supplied to the /TRST pin by pulling the pin down by a resistance of 1 kilo-ohm and setting PUL15 = 0 in the PULCR register after a reset.
5. The pattern between the H-UDI port connector and the MPU must be as short as possible. Do not connect the signal lines to other components on the board.
6. Since the H-UDI and the AUD of the MPU operate with the Vcc, supply only the Vcc to the UVCC pin. Make the emulator's switch settings so that the user power will be supplied (SW2 = 1 and SW3 = 1).
7. The resistance values shown in figure 1.4 are reference.
8. For the pin processing in cases where the emulator is not used, refer to the hardware manual of the related MPU.

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When the circuit is connected as shown in figure 1.4, the switches of the emulator are set as SW2 = 1 and SW3 = 1. For details, refer to section 3.8, Setting the DIP Switches, in the SuperH™ Family E10A-USB Emulator User's Manual.
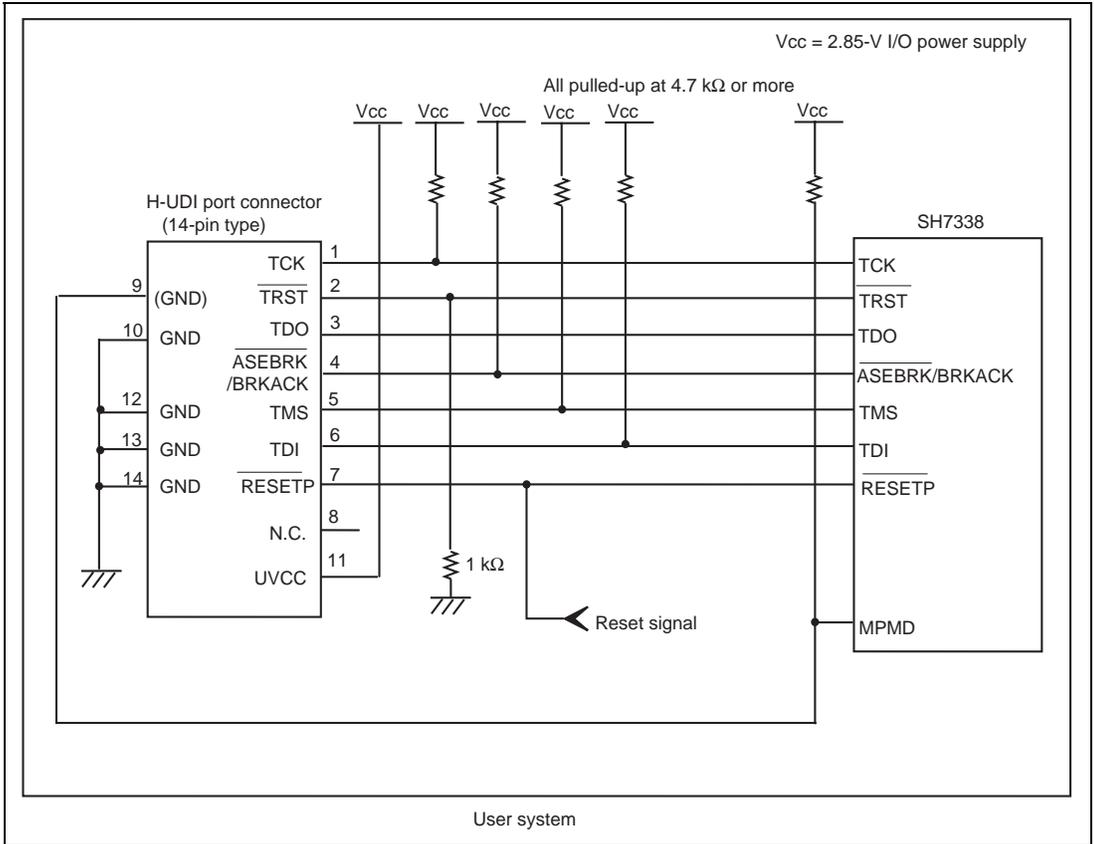

Figure 1.4   Recommended Circuit for Connection between the H-UDI Port Connector and MPU when the Emulator is in Use (14-Pin Type)

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Section 2 Software Specifications when Using the SH7338

2.1   Differences between the SH7338 and the Emulator

1. When the emulator system is initiated, it initializes the general registers and part of the control registers as shown in table 2.1. The initial values of the actual SH7338 registers are undefined. When the emulator is initiated from the workspace, a value to be entered is saved in a session.

Table 2.1   Register Initial Values at Emulator Link Up

Register	Emulator at Link Up
R0 to R14	H'00000000
R15 (SP)	H'A0000000
R0_BANK to R7_BANK	H'00000000
PC	H'A0000000
SR	H'700000F0
GBR	H'00000000
VBR	H'00000000
MACH	H'00000000
MACL	H'00000000
PR	H'00000000
SPC	H'00000000
SSR	H'000000F0
RS	H'00000000
RE	H'00000000
MOD	H'00000000
A0G, A1G	H'00000000
A0, A1	H'00000000
X0, X1	H'00000000
Y0, Y1	H'00000000
M0, M1	H'00000000
DSR	H'00000000

2. The emulator uses the H-UDI; do not access the H-UDI.

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3. Low-Power States (Sleep, Software Standby, Module Standby, U Standby, and R Standby)

For low-power consumption, the SH7338 has sleep, software standby, module standby, U standby, and R standby states.

The sleep, software standby, and module standby states are switched using the SLEEP instruction. When the emulator is used, the sleep and software standby states can be cleared with either the normal clearing function or with the [STOP] button, and a break will occur.

Note: The memory must not be accessed or modified in sleep state.

4. Reset Signals

The SH7338 reset signals are only valid during emulation started with clicking the GO or STEP-type button. If these signals are enabled on the user system in command input wait state, they are not sent to the SH7338.

Note: Do not break the user program when the /RESETP or /BREQ signal is being low and the wait control signal is being active. A TIMEOUT error will occur. If the wait control signal becomes active or the /BREQ signal is fixed to low during break, a TIMEOUT error will occur at memory access.

5. Direct Memory Access Controller (DMAC)

The DMAC operates even when the emulator is used. When a data transfer request is generated, the DMAC executes DMA transfer.

6. Memory Access during User Program Execution

When a memory is accessed from the memory window, etc. during user program execution, the user program is resumed after it has stopped in the E10A-USB emulator to access the memory. Therefore, realtime emulation cannot be performed.

The stopping time of the user program is as follows:

Environment:

Host computer: 800 MHz (Pentium® III)
JTAG clock: 10 MHz (TCK clock)

When a one-byte memory is read from the command-line window, the stopping time will be about 42 ms.

7. Memory Access during User Program Break

The emulator can download the program for the flash memory area (for details, refer to section 6.22, Download Function to the Flash Memory Area, in the SuperH™ Family E10A-USB Emulator User's Manual). Other memory write operations are enabled for the RAM area. Therefore, an operation such as memory write or BREAKPOINT should be set only for the RAM area.

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8. Cache Operation during User Program Break

    When cache is enabled, the emulator accesses the memory by the following methods:

    - At memory write: Writes through the cache, then issues a single write to outside. The LRU is not updated.

    - At memory read: Reads memory from the cache. The LRU is not updated.

    Therefore, when memory read or write is performed during user program break, the cache state does not change.

    - At breakpoint set: Disables the instruction cache.

9. Port G

    The AUD pin is multiplexed as shown in table 2.2.

Table 2.2 Multiplexed Functions

Port	Function 1	Function 2
G	PTG4 input/output (port)*	/AUDSYNC (AUD)
G	PTG3 input/output (port)*	AUDATA3 (AUD)
G	PTG2 input/output (port)*	AUDATA2 (AUD)
G	PTG1 input/output (port)*	AUDATA1 (AUD)
G	PTG0 input/output (port)*	AUDATA0 (AUD)

Note: Function 1 can be used when the AUD pins of the device are not connected to the emulator. When the AUD trace is enabled, the emulator changes settings so that function 2 is forcibly used.

10. UBC

    When [User] is specified in the [UBC mode] list box in the [Configuration] dialog box, the UBC can be used in the user program.
    Do not use the UBC in the user program as it is used by the emulator when [EML] is specified in the [UBC mode] list box in the [Configuration] dialog box.

11. MFI

    When the MFI boot mode is used, be sure to activate the emulator by setting the MFIINT signal as a trigger for the MFI transfer from the base-band side.
    In the active-through mode, the emulator does not operate during break.

12. Using RWDT

    At power-on reset, the operation of RWDT is enabled. When RWDT is not used, be sure to disable the operation of RWDT at the top of the user-reset program.
    The RWTCSR.TME bit is masked as 0 during break. Therefore, 0 is always displayed in the [IO] and [Memory] windows.

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13. Memory Access during Break

In the enabled MMU, when a memory is accessed and a TLB error occurs during break, it can be selected whether the TLB exception is controlled or the program jumps to the user exception handler in [TLB Mode] in the [Configuration] dialog box. When [TLB miss exception is enable] is selected, a "Communication Timeout error" will occur if the TLB exception handler does not operate correctly. When [TLB miss exception is disable] is selected, the program does not jump to the TLB exception handler even if a TLB exception occurs. Therefore, if the TLB exception handler does not operate correctly, a "Communication Timeout error" will not occur but the memory contents may not be correctly displayed.

14. Loading Sessions

Information in [JTAG clock] of the [Configuration] dialog box cannot be recovered by loading sessions. Thus the TCK value will be as follows:

- When HS0005KCU01H or HS0005KCU02H is used: TCK = 1.25 MHz

15. [IO] window

- Display and modification

  Do not change values of the User Break Controller because it is used by the emulator.

  For each RCLK watchdog timer register, there are two registers to be separately used for write and read operations.

Table 2.3   RCLK Watchdog Timer Register

Register Name	Usage	Register
RWTCSR(W)	Write	RCLK watchdog timer control/status register
RWTCNT(W)	Write	RCLK watchdog timer counter
RWTCSR(R)	Read	RCLK watchdog timer control/status register
RWTCNT(R)	Read	RCLK watchdog timer counter

- The RCLK watchdog timer operates only when the user program is executed. Do not change the value of the frequency change register in the [IO] window or [Memory] window.

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- The internal I/O registers can be accessed from the [IO] window. However, note the following when accessing the SDMR register of the bus-state controller. Before accessing the SDMR register, specify addresses to be accessed in the I/O-register definition file (SH7338.IO) and then activate the HEW. After the I/O-register definition file is created, the MPU's specifications may be changed. If each I/O register in the I/O-register definition file differs from addresses described in the hardware manual, change the I/O-register definition file according to the description in the hardware manual. The I/O-register definition file can be customized depending on its format. Note that, however, the E10A emulator does not support the bit-field function.

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- Verify

    In the [IO] window, the verify function of the input value is disabled.

16. Illegal Instructions

    If illegal instructions are executed by STEP-type commands, the emulator cannot go to the next program counter.

17. [Reset CPU] and [Reset Go] in the [Debug] Menu

    When a reset is issued from [Reset CPU] or [Reset Go] in the [Debug] menu, the clock pulse generator or watchdog timer is not initialized.

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2.2 Specific Functions for the Emulator when Using the SH7338

2.2.1 Event Condition Functions

The emulator is used to set 12 event conditions (Ch1 to Ch12) and the software trace. Table 2.4 lists the conditions of Event Condition.

Table 2.4 Types of Event Conditions

Event Condition Type	Description
Address bus condition (Address)	Breaks when the SH7338 address bus value or the program counter value matches the specified value.
Data bus condition (Data)	Breaks when the SH7338 data bus value matches the specified value. Byte, word, or longword can be specified as the access data size.
Bus state condition (Bus State)	There are two bus state condition settings:
	Bus state condition: Breaks or acquires a trace when the data bus or the X-Bus or Y-Bus address bus of the SH7338 is matched.
	Read/Write condition: Breaks or acquires a trace when the specified read/write condition is matched.
Window address condition	Breaks or acquires a trace when the data in the specified memory range is accessed.
System bus	Breaks or acquires a trace when the address or data on the system bus is matched.
LDTLB instruction event condition	Breaks when the SH7338 executes the LDTLB instruction.
Count	Breaks when the conditions set are satisfied the specified number of times.
Branch trace condition (Branch trace)	Breaks or acquires a trace when a branch occurs with the condition specified by the SH7338. (By default, trace acquisition is enabled).
Software trace	Selects whether or not the software trace is acquired.
Action	Selects the operation when a condition, such as setting a break, trace, or performance start or end, is matched.

Table 2.5 lists the combinations of conditions that can be set under Ch1 to Ch12 and the software trace.

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Table 2.5   Dialog Boxes for Setting Event Conditions

Dialog Box	Address Bus Condition (Address)	Data Bus Condition (Data)	ASID Condition (ASID)	Bus State Condition (Bus Status)	Window Address Condition (Window address)	System Bus	LDTLB Instruction Break	Count Condition (Count)	Branch Condition (Branch Trace)	Software Trace	Action
[Event Condition 1] dialog box	O	X	O	O	X	X	X	X	X	X	O (B and P)
[Event Condition 2] dialog box	O	O	O	O	X	X	X	O	X	X	O (B and P)
[Event Condition 3] dialog box	O	X	O	X	X	X	X	X	X	X	O (B and P)
[Event Condition 4] dialog box	O	X	O	X	X	X	X	X	X	X	O (B and P)
[Event Condition 5] dialog box	X	X	O	O	O	X	X	X	X	X	O (B, T, and P)
[Event Condition 6] dialog box	X	X	O	O	O	X	X	X	X	X	O (B, T, and P)
[Event Condition 7] dialog box	X	X	X	X	X	X	O	X	X	X	Break fixed
[Event Condition 8] dialog box	O	X	X	X	X	O	X	X	X	X	O (B, T, and P)

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Table 2.5   Dialog Boxes for Setting Event Conditions (cont)

	Function										
Dialog Box	Address Bus Condition (Address)	Data Bus Condition (Data)	ASID Condition (ASID)	Bus State Condition (Bus Status)	Window Address Condition (Window address)	System Bus	LDTLB Instruction Break	Count Condition (Count)	Branch Condition (Branch Trace)	Software Trace	Action
[Event Condition 9] dialog box	O	X	X	X	X	O	X	X	X	X	O (B, T, and P)
[Event Condition 10] dialog box	O	X	O	O	X	X	X	X	X	X	O (B and P)
[Event Condition 11] dialog box	O	O	O	O	X	X	X	O	X	X	O (B and P)
[Event Condition 12] dialog box	X	X	X	X	X	X	X	X	O	X	O (B, T, and P)
[Software trace] dialog box	X	X	X	X	X	X	X	X	X	O	Trace fixed

Notes: 1. O: Can be set in the dialog box.
X: Cannot be set in the dialog box.

2. For the Action item,
B: Setting a break is enabled.
T: Setting a trace is enabled.
P: Setting a performance start or end condition is enabled.

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Sequential Setting: In the emulator, sequential setting of an Event Condition is enabled.

Table 2.6   Sequential Event Conditions

	Type	Event Condition	Description
[CPU Sequential Event] Page	2 Channel Sequential	Ch2 -> 1	Halts a program when a condition is satisfied in the order of Event Condition 2, 1. An event condition must be set for Ch2 and Ch1.
		Ch4 -> 3	Halts a program when a condition is satisfied in the order of Event Condition 4, 3. An event condition must be set for Ch4 and Ch3.
		Ch6 -> 5	Halts a program when a condition is satisfied in the order of Event Condition 6, 5. An event condition must be set for Ch6 and Ch5.
		Ch11 -> 10	Halts a program when a condition is satisfied in the order of Event Condition 11, 10. An event condition must be set for Ch11 and Ch10.
	Many Channel Sequential	Ch3 -> 2 -> 1	Halts a program when a condition is satisfied in the order of Event Condition 3, 2, 1. An event condition must be set for Ch3, Ch2, and Ch1.
		Ch4 -> 3-> 2 -> 1	Halts a program when a condition is satisfied in the order of Event Condition 4, 3, 2, 1. An event condition must be set for Ch4, Ch3, Ch2, and Ch1.
		Ch5 -> 4 -> 3-> 2 -> 1	Halts a program when a condition is satisfied in the order of Event Condition 5, 4, 3, 2, 1. An event condition must be set for Ch5, Ch4, Ch3, Ch2, and Ch1.
		Ch6 -> 5 -> 4 -> 3-> 2 -> 1	Halts a program when a condition is satisfied in the order of Event Condition 6, 5, 4, 3, 2, 1. An event condition must be set for Ch6, Ch5, Ch4, Ch3, Ch2, and Ch1.
		Ch10 -> 6 -> 5 -> 4 -> 3-> 2 -> 1	Halts a program when a condition is satisfied in the order of Event Condition 10, 6, 5, 4, 3, 2, 1. An event condition must be set for Ch10, Ch6, Ch5, Ch4, Ch3, Ch2, and Ch1.
		Ch11 -> 10 -> 6 -> 5 -> 4 -> 3-> 2 -> 1	Halts a program when a condition is satisfied in the order of Event Condition 11, 10, 6, 5, 4, 3, 2, 1. An event condition must be set for Ch11, Ch10, Ch6, Ch5, Ch4, Ch3, Ch2, and Ch1.

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Table 2.6   Sequential Event Conditions (cont)

	Type	Event Condition	Description
[CPU Sequential Event] Page (cont)	CPU Extend		Expands the [CPU Sequential Extend] page. The sequential setting is enabled with any combination. For details, refer to section 2.2.1, Sequential Break Extension Setting, in this manual.
[SystemBus Sequential Event] Page	SystemBus Sequential Event	Ch9 -> 8	Halts a program when a condition is satisfied for Event Condition 9, 8. An event condition must be set for Ch9 and Ch8.
		Ch8 -> 9	Halts a program when a condition is satisfied for Event Condition 8, 9. An event condition must be set for Ch8 and Ch9.
	SystemBus Extend		Expands the [SystemBus Sequential Extend] page. The sequential setting is enabled with any combination. For details, refer to section 2.2.1, Sequential Break Extension Setting, in this manual.

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Sequential Break Extension Setting:
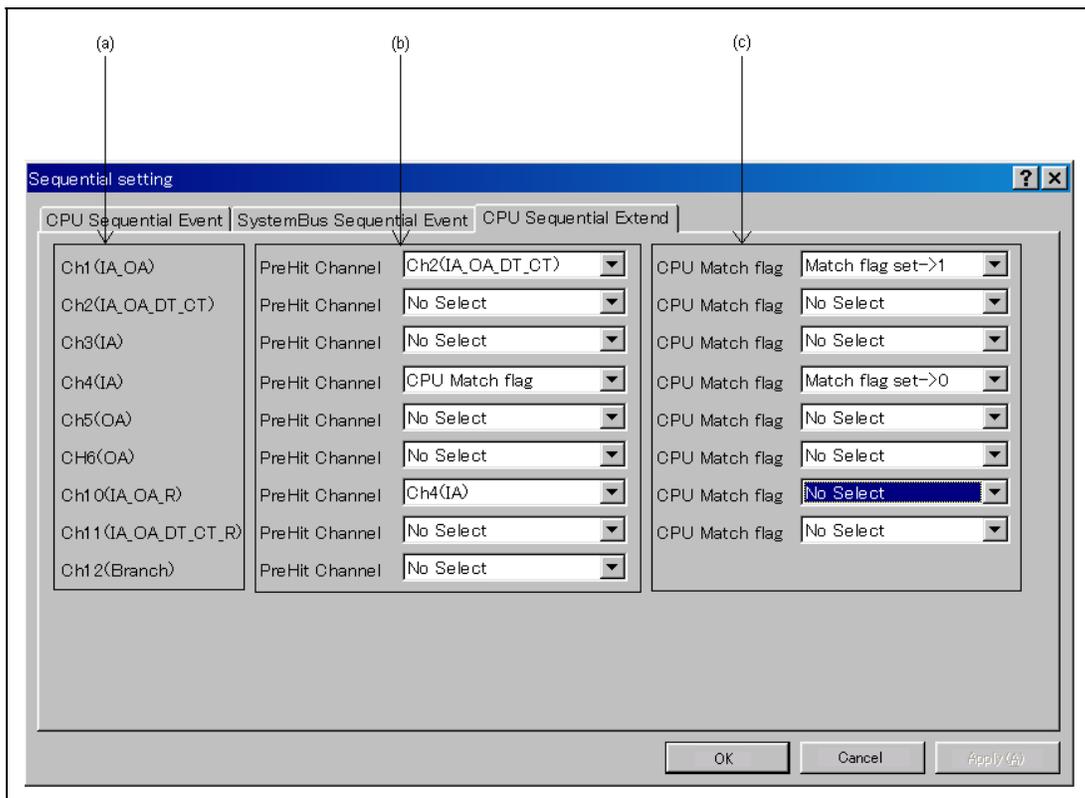
Figure 2.1   [CPU Sequential Extend] Page

(a) Indicates the channel name for setting conditions.

(b) Selects a condition that is satisfied before the channel which sets up conditions.
When a channel name is selected, it is required that the condition of the channel selected here must have already been satisfied.
When [CPU Match flag] is selected, the CPU match flag must be set.
When a condition is selected by the channel selected here, no break will occur.

(c) When a condition is satisfied, the CPU match flag is set or cleared.
When a program breaks, the CPU match flag is initialized.

Set the event condition for each channel in the [Event Condition] dialog box; this also applies to the [SystemBus Sequential Extend] page.

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Usage Example of Sequential Break Extension Setting: A tutorial program provided for the product is used as an example. For the tutorial program, refer to section 6, Tutorial, in the SuperH™ Family E10A-USB Emulator User's Manual.

The conditions of Event Condition are set as follows:

1. Ch1

   Breaks address H'00001068 when the condition [Prefetch address break after executing] is satisfied.

2. Ch2

   Breaks address H'00001058 when the condition [Prefetch address break after executing] is satisfied.

3. Ch4

   Breaks address H'0000107a when the condition [Prefetch address break after executing] is satisfied.

4. Ch10

   Breaks address H'00001086 when the condition [Prefetch address break after executing] is satisfied.
   Note: Do not set other channels.

5. Set the [CPU Sequential Extend] page as shown in figure 2.1.

Then, set the program counter and stack pointer (PC = H'00000800, R15 = H'00010000) in the [Registers] window and click the [Go] button. If this does not execute normally, issue a reset and execute the above procedures.

The program is executed up to the condition of Ch10 and halted. Here, the condition is satisfied in the order of Ch2 -> 1 -> 4 -> 10.

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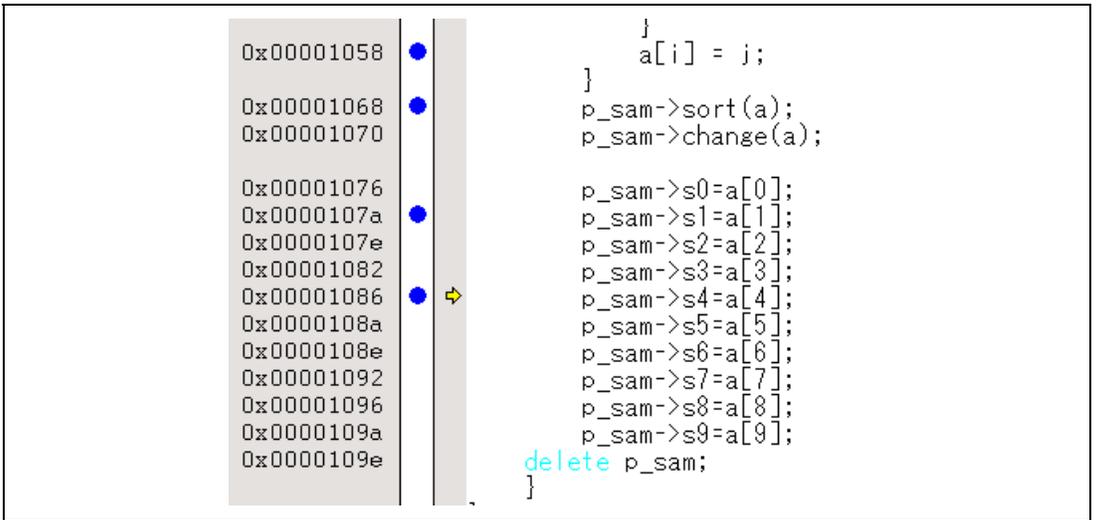
Figure 2.2 [Source] Window at Execution Halted (Sequential Break)

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2.2.2 Trace Functions

The emulator supports the trace functions listed in table 2.7.

Table 2.7 Trace Functions

Function	Internal Trace	AUD Trace	Memory Output Trace
Branch trace	Supported (eight branches)	Supported	Supported
Range memory access trace	Supported (eight events)	Supported	Supported
Software trace	Supported (eight events)	Supported	Supported

Table 2.8 shows the type numbers that the AUD function can be used.

Table 2.8 Type Number and AUD Function

Type Number	AUD Function
HS0005KCU01H	Not supported
HS0005KCU02H	Supported

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Branch Trace Functions: The branch source and destination addresses, their source lines, branch types, and types of accessed bus masters are displayed.

[Setting Method]
Select the check box in the [Branch] group box in the [Branch trace] page of the [Branch trace] dialog box that opens by double-clicking on the Ch12 (Branch) column of the [Eventpoint] window. The branch condition to be acquired can be set.
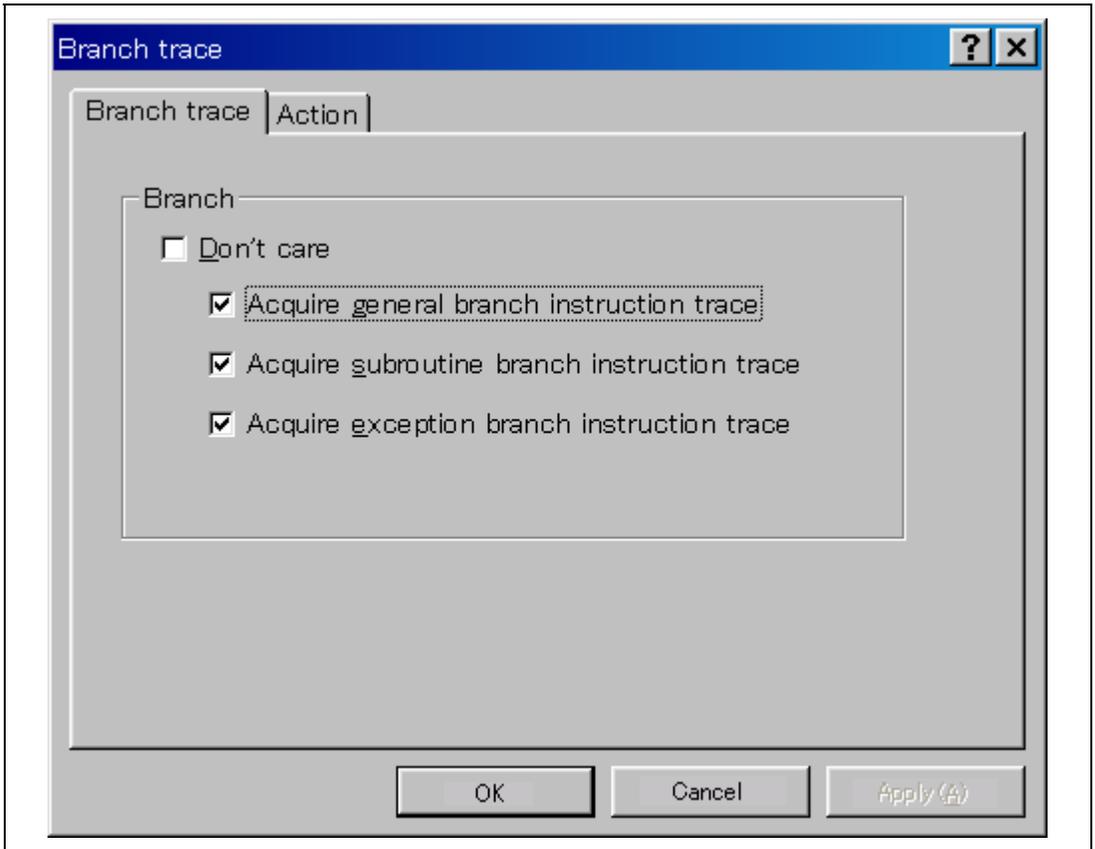
Figure 2.3   [Branch trace] Dialog Box

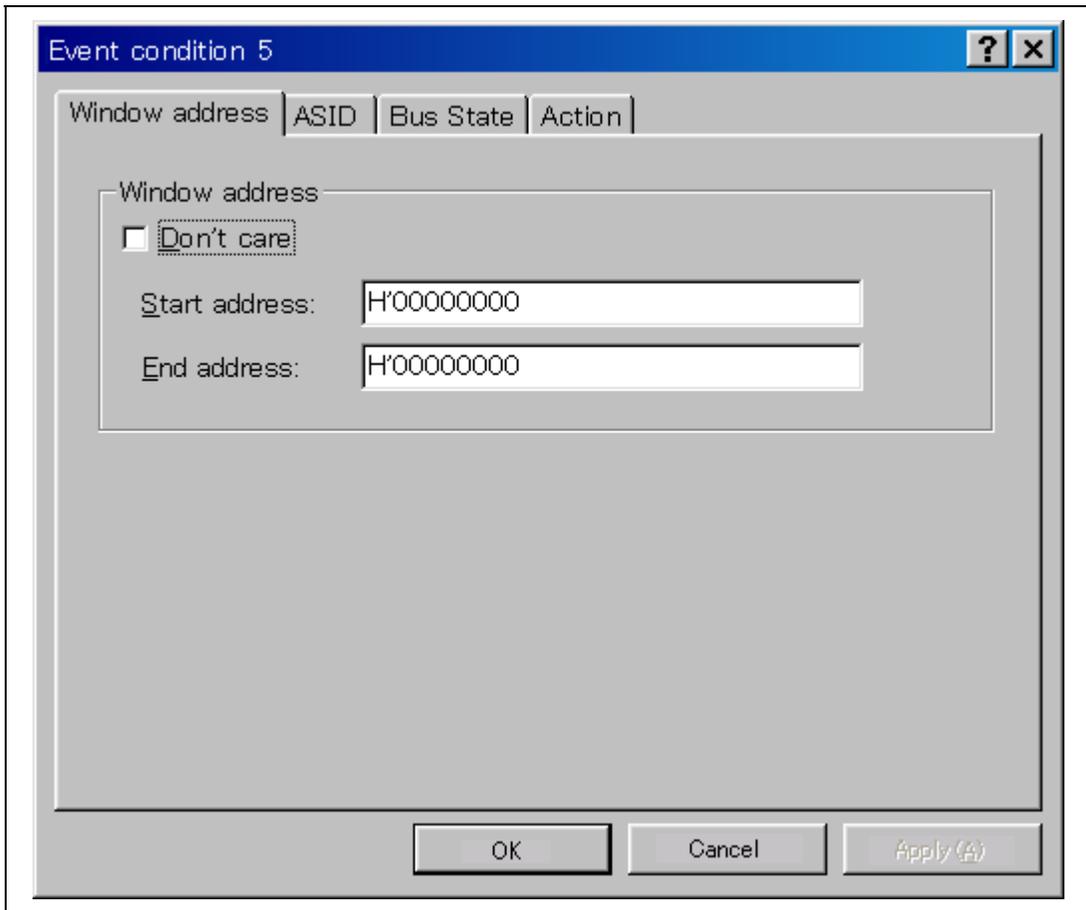A branch trace can be acquired by selecting the [Acquire trace] check box of the [Action] page.

Note: To cancel settings, select [Delete] from the popup menu that is opened by clicking on the Ch12 (Branch) column with the right-mouse button.

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Range Memory Access Trace Functions: The memory access within the specified range is acquired by a trace. The read cycle, write cycle, or read/write cycle can be selected as the bus type, ASID value, or bus cycle for trace acquisition.

[Setting Method]
To open the [Event condition 5] or [Event condition 6] dialog box, double-click on the Ch5 (OA) or Ch6 (OA) column of the [Eventpoint] window.
Remove the check mark of the [Don't care] check box in the [Window address] page and enter the memory range to be set.

Figure 2.4 [Window address] Page

(i)   Open the [ASID] page, remove the check mark of the [Don't care] check box, and enter the ASID value to be set.

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When the ASID value is not set as a condition, do not remove the check mark of the [Don't care] check box.

(ii)   Open the [Bus state] page and specify the bus type and bus cycle that are to be set.
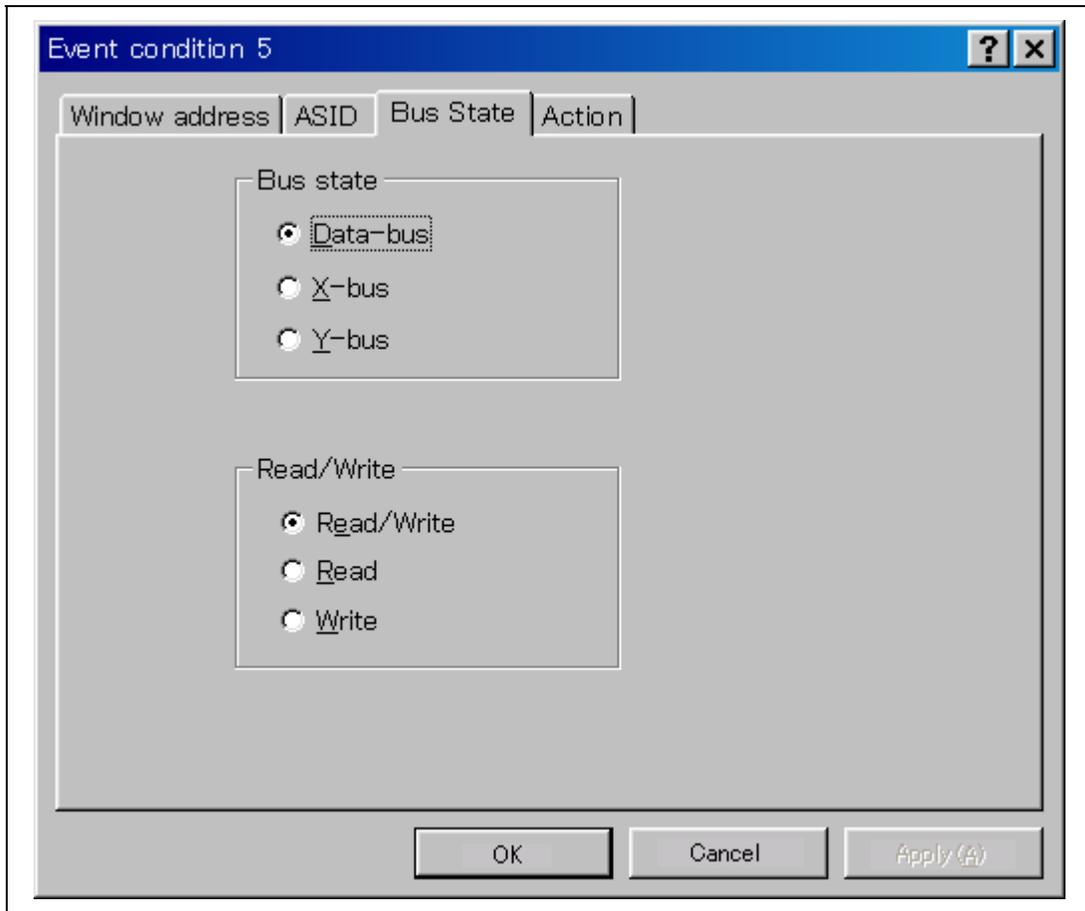
Figure 2.5   [Bus State] Page

(iii)   Selecting the [Acquire trace] check box in the [Action] page enables acquiring memory access within the range.

Note: To cancel settings, select the popup menu that is opened by clicking on the Ch5 (OA) or Ch6 (OA) column with the right-mouse button.

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Software Trace Function:

Note: This function can be supported with SHC/C++ compiler (manufactured by Renesas Technology Corp.; including OEM and bundle products) V6.0 or later.
However, SHC/C++ compiler (including OEM and bundle products) V8.0 or later is needed when instructions other than those compatible with SH4 are output.

When a specific instruction is executed, the PC value at execution and the contents of one general register are acquired by trace. Describe the Trace(x) function (x is a variable name) to be compiled and linked beforehand. For details, refer to the SuperH™ RISC engine C/C++ Compiler, Assembler, Optimizing Linkage Editor User's Manual.

When the load module is downloaded on the emulator and is executed while a software trace function is valid, the PC value that has executed the Trace(x) function, the general register value for x, and the source lines are displayed.

To activate the software trace function, select the [Acquire Software trace] radio button in the [Software trace] dialog box that is opened by double-clicking on the software Trace column of the [Eventpoint] window.

Note: To cancel settings, select the [Don't care] radio button in the [Software trace] dialog box or select [Delete] from the popup menu that is opened by clicking on the software Trace column with the right-mouse button.

Internal Trace Function: This function is activated by selecting the [Internal trace] radio button in the [Trace type] group box of the [Trace mode] page. Set the trace condition to be used.

Notes: 1. If an interrupt is generated at the program execution start or end, including a step operation, the emulator address may be acquired. In such a case, the following message will be displayed. Ignore this address because it is not a user program address.
*** EML ***
2. If a completion-type exception occurs during exception branch acquisition, the next address to the address in which an exception occurs is acquired.
3. Trace information cannot be acquired for the following branch instructions:
   - The BF and BT instructions whose displacement value is 0
   - Branch to H'A0000000 by reset

AUD Trace Functions: This function is operational when the AUD pin of the device is connected to the emulator. It is activated by selecting the [AUD trace] radio button in the [Trace type] group box of the [Trace mode] page. Set the trace condition to be used.

Table 2.9 shows the AUD trace acquisition mode that can be set in each trace function.

Table 2.9   AUD Trace Acquisition Mode

Type	Mode	Description
Continuous trace occurs	Realtime trace	When the next branch occurs while the trace information is being output, all the information may not be output. The user program can be executed in realtime, but some trace information will be lost.
	Non realtime trace	When the next branch occurs while the trace information is being output, the CPU stops operations until the information is output. The user program is not executed in realtime.
Trace buffer full	Trace continue	This function overwrites the oldest trace information to store the latest trace information.
	Trace stop	After the trace buffer becomes full, the trace information is no longer acquired. The user program is continuously executed.

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To set the AUD trace acquisition mode, click the [Trace] window with the right mouse button and select [Setting] from the pop-up menu to display the [Acquisition] dialog box. The AUD trace acquisition mode can be set in the [Trace mode1] or [Trace mode2] group box in the [Trace mode] page of the [Acquisition] dialog box.
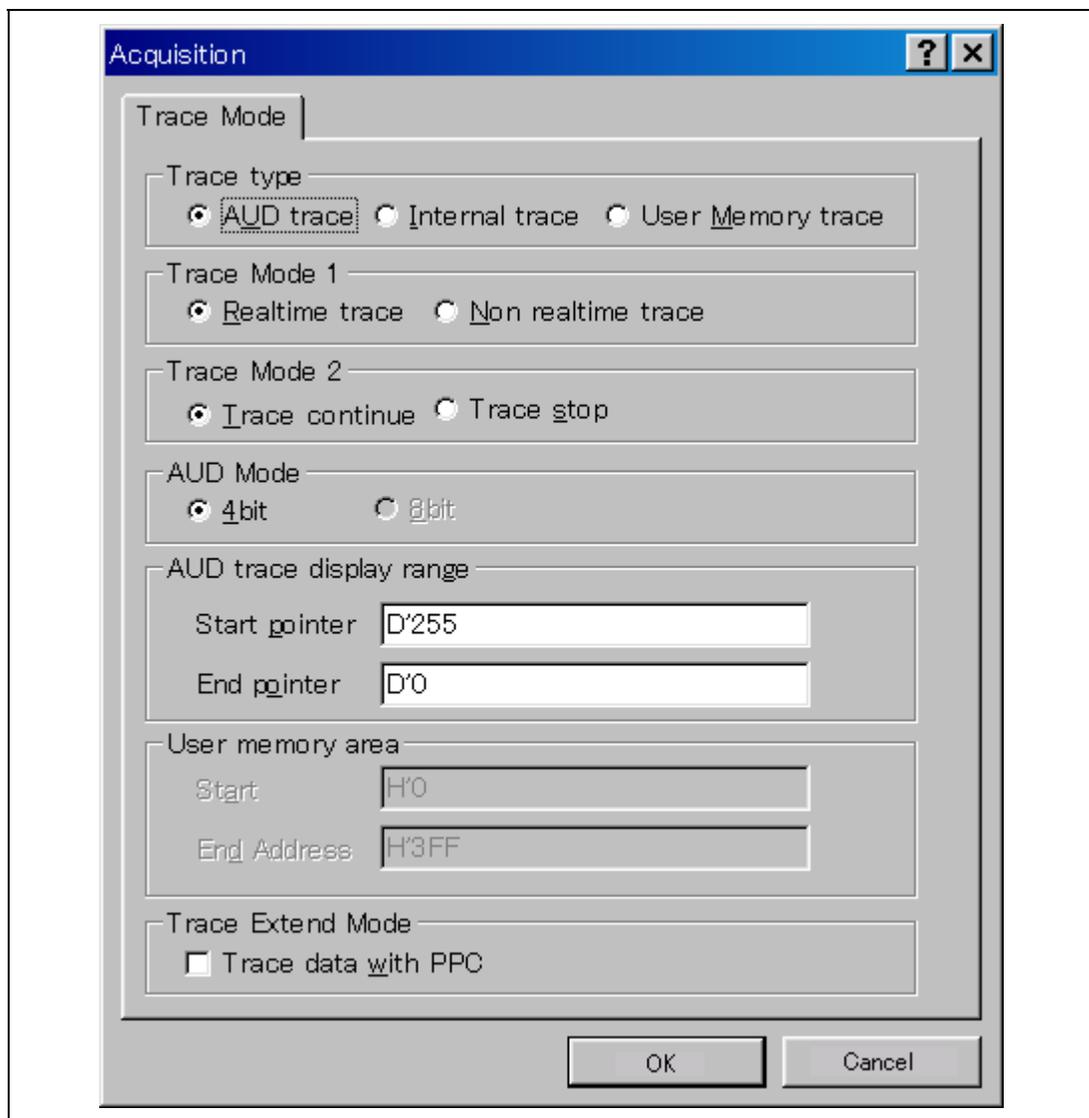

Figure 2.6   [Trace Mode] Page

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When the AUD trace function is used, select the [AUD function] radio button in the [Trace type] group box of the [Trace mode] page.

Notes on AUD Trace:

1. When the trace display is performed during user program execution, the mnemonics, operands, or source is not displayed.
2. The AUD branch trace function outputs the differences between newly output branch source addresses and previously output branch source addresses. The window trace function outputs the differences between newly output addresses and previously output addresses. If the previously output address is the same as the upper 16 bits, the lower 16 bits are output. If it matches the upper 24 bits, the lower 8 bits are output. If it matches the upper 28 bits, the lower 4 bits are output.
   The emulator regenerates the 32-bit address from these differences and displays it in the [Trace] window. If the emulator cannot display the 32-bit address, it displays the difference from the previously displayed 32-bit address.
3. If the 32-bit address cannot be displayed, the source line is not displayed.
4. In the emulator, when multiple loops are performed to reduce the number of AUD trace displays, only the IP counts up.
5. In the emulator, the maximum number of trace displays is 65534 lines (32767 branches). However, the maximum number of trace displays differs according to the AUD trace information to be output. Therefore, the above pointers cannot be always acquired.
6. The AUD trace acquisition is not available when [User] is selected in the [UBC mode] list box of the [Configuration] dialog box. In this case, close the [Trace] window.
7. Do not use the AUD full-trace mode for the VIO function.
8. If a completion-type exception occurs during exception branch acquisition, the next address to the address in which an exception occurs is acquired.

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Memory Output Trace Functions: This function is activated by selecting the [Use Memory trace] radio button in the [Trace type] group box of the [Trace mode] page.
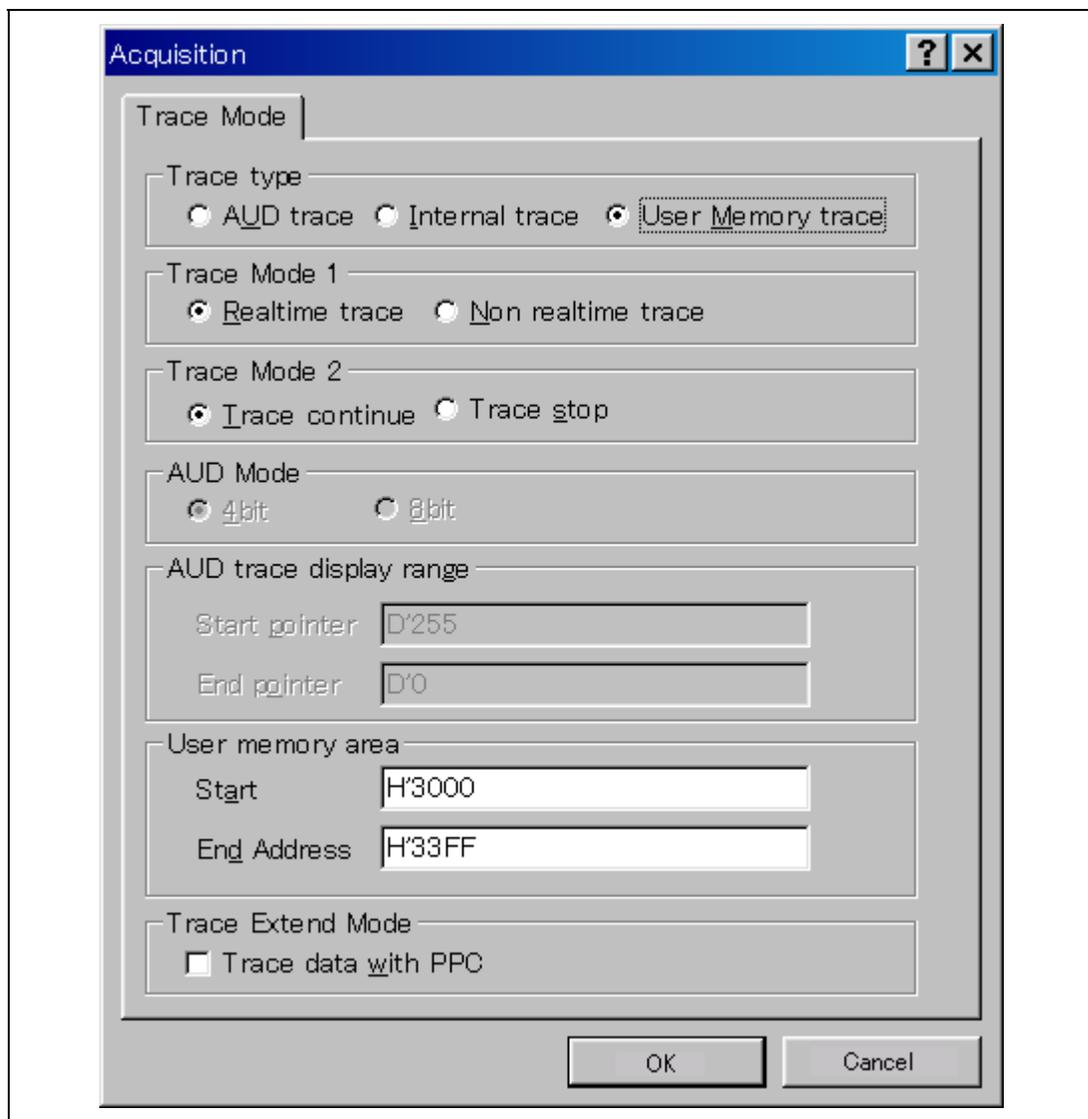In this function, write the trace data in the specified user memory range.
Specify the start address to output a trace for the [Start] edit box in the [User memory area] group box, and the end address for the [End Address] edit box. Set the trace condition to be used.

Table 2.10 shows the memory-output trace acquisition mode that can be set in each trace function.

Table 2.10   Memory-Output Trace Acquisition Mode

Type	Mode	Description
Continuous trace occurs	Realtime trace	When the next branch occurs while the trace information is being output, all the information may not be output. The user program can be executed in realtime, but some trace information will be lost.
	Non realtime trace	When the next branch occurs while the trace information is being output, the CPU stops operations until the information is output. The user program is not executed in realtime.
Trace buffer full	Trace continue	This function overwrites the oldest trace information to store the latest trace information.
	Trace stop	After the trace buffer becomes full, the trace information is no longer acquired. The user program is continuously executed.

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To set the memory-output trace acquisition mode, click the [Trace] window with the right mouse button and select [Setting] from the pop-up menu to display the [Acquisition] dialog box. The AUD trace acquisition mode can be set in the [Trace mode1] or [Trace mode2] group box in the [Trace mode] page of the [Acquisition] dialog box.

Figure 2.7   [Trace Mode] Page

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Notes: 1. Use only the following addresses in the memory range for which trace is output:
                <External memory area>
                CS0, CS2, CS4, CS5A, CS5B, CS6A, and CS6B
                <Internal memory area>
                URAM: H'055E0000 to H'0561FFFF
                XRAM: H'05007000 to H'05008FFF
                YRAM: H'05017000 to H'05018FFF
                Note that this address is on the system bus and not supported for the MMU or cache.

    2. In the memory range for output, do not specify the ranges that the user program has been downloaded or the user program accesses.

    3. The range for trace output must be 1 MB or less.

2.2.3 Notes on Using the JTAG (H-UDI) Clock (TCK) and AUD Clock (AUDCK)

1. Set the JTAG clock (TCK) frequency to lower than the frequency of the SH7338 peripheral module clock (CKP).
2. Set the AUD clock (AUDCK) frequency to 50 MHz or lower. If the frequency is higher than 50 MHz, the emulator will not operate normally.
3. The set value of the JTAG clock (TCK) is initialized by executing [Reset CPU] or [Reset Go].

2.2.4 Notes on Setting the [Breakpoint] Dialog Box

1. When an odd address is set, the next lowest even address is used.
2. A BREAKPOINT is accomplished by replacing instructions of the specified address. Accordingly, it can be set only to the RAM areas in CS0 to CS6 and the internal RAM areas. However, a BREAKPOINT cannot be set to the following addresses:
    - ROM areas in CS0 to CS6
    - Areas other than the internal RAM
    - Areas other than CS0 to CS6
    - A slot instruction of a delayed branch instruction
    - An area that can be only read by MMU
3. During step operation, BREAKPOINTs are disabled.
4. When execution resumes from the address where a BREAKPOINT is specified, single-step operation is performed at the address and execution is continued from the next PC value. Therefore, realtime operation cannot be performed.
5. When a BREAKPOINT is set to the slot instruction of a delayed branch instruction, the PC value becomes an illegal value. Accordingly, do not set a BREAKPOINT to the slot instruction of a delayed branch instruction.

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6. Note on DSP repeat loop:
   A BREAKPOINT is equal to a branch instruction. In some DSP repeat loops, branch instructions cannot be set. For these cases, do not set BREAKPOINTs. Refer to the hardware manual for details.

7. When the [Normal] option is selected in the [Memory area] group box in the [General] page of the [Configuration] dialog box, a BREAKPOINT is set to a physical address or a virtual address according to the SH7338 MMU status during command input when the VPMAP_SET command setting is disabled. The ASID value of the SH7338 PTEH register during command input is used. When VPMAP_SET command setting is enabled, a BREAKPOINT is set to a physical address into which address translation is made according to the VP_MAP table. However, for addresses out of the range of the VP_MAP table, the address to which a BREAKPOINT is set depends on the SH7338 MMU status during command input. Even when the VP_MAP table is modified after BREAKPOINT setting, the address translated when the BREAKPOINT is set valid.

8. When the [Physical] option is selected in the [Memory area] group box in the [General] page of the [Configuration] dialog box, a BREAKPOINT is set to a physical address. A BREAKPOINT is set after disabling the SH7338 MMU upon program execution. After setting, the MMU is returned to the original state. When a break occurs at the corresponding virtual address, the cause of termination displayed in the status bar and the [Output] window is ILLEGAL INSTRUCTION, not BREAKPOINT.

9. When the [Virtual] option is selected in the [Memory area] group box in the [General] page of the [Configuration] dialog box, a BREAKPOINT is set to a virtual address. A BREAKPOINT is set after enabling the SH7338 MMU upon program execution. After setting, the MMU is returned to the original state. When an ASID value is specified, the BREAKPOINT is set to the virtual address corresponding to the ASID value. The emulator sets the BREAKPOINT after rewriting the ASID value to the specified value, and returns the ASID value to its original value after setting. When no ASID value is specified, the BREAKPOINT is set to a virtual address corresponding to the ASID value at command input.

10. An address (physical address) to which a BREAKPOINT is set is determined when the BREAKPOINT is set. Accordingly, even if the VP_MAP table is modified after BREAKPOINT setting, the BREAKPOINT address remains unchanged. When a BREAKPOINT is satisfied with the modified address in the VP_MAP table, the cause of termination displayed in the status bar and the [Output] window is ILLEGAL INSTRUCTION, not BREAKPOINT.

11. If an address of a BREAKPOINT cannot be correctly set in the ROM or flash memory area, a mark ● will be displayed in the [BP] area of the address on the [Source] or [Disassembly] window by refreshing the [Memory] window, etc. after Go execution. However, no break will occur at this address. When the program halts with the event condition, the mark ● disappears.

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2.2.5   Notes on Setting the [Event Condition] Dialog Box and the BREAKCONDITION_ SET Command

1. When [Go to cursor], [Step In], [Step Over], or [Step Out] is selected, the settings of Event Condition 3 are disabled.
2. When an Event Condition is satisfied, emulation may stop after two or more instructions have been executed.
3. If a PC break address condition is set to the slot instruction after a delayed branch instruction, user program execution cannot be terminated before the slot instruction execution; execution stops before the branch destination instruction.

2.2.6   Note on Setting the UBC_MODE Command

In the [Configuration] dialog box, if [User] is set while the [UBC mode] list box has been set, Ch10 (IA_OA_R) and Ch11 (OA_OA_CT_R) of Event Condition cannot be used.

2.2.7   Note on Setting the PPC_MODE Command

In the [Configuration] dialog box, if [User] is set while the [PPC mode] list box has been set, Ch1 and Ch2 of the performance analysis function and options 1 and 2 of the profile function cannot be used.

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2.2.8　　Performance Measurement Function

The emulator supports the performance measurement function.

1. Setting the performance measurement conditions

   To set the performance measurement conditions, use the [Performance Analysis] dialog box and the PERFORMANCE_SET command. When a channel line on the [Performance Analysis] window is clicked with the right mouse button, the popup menu is displayed and the [Performance Analysis] dialog box is displayed by selecting [Setting].
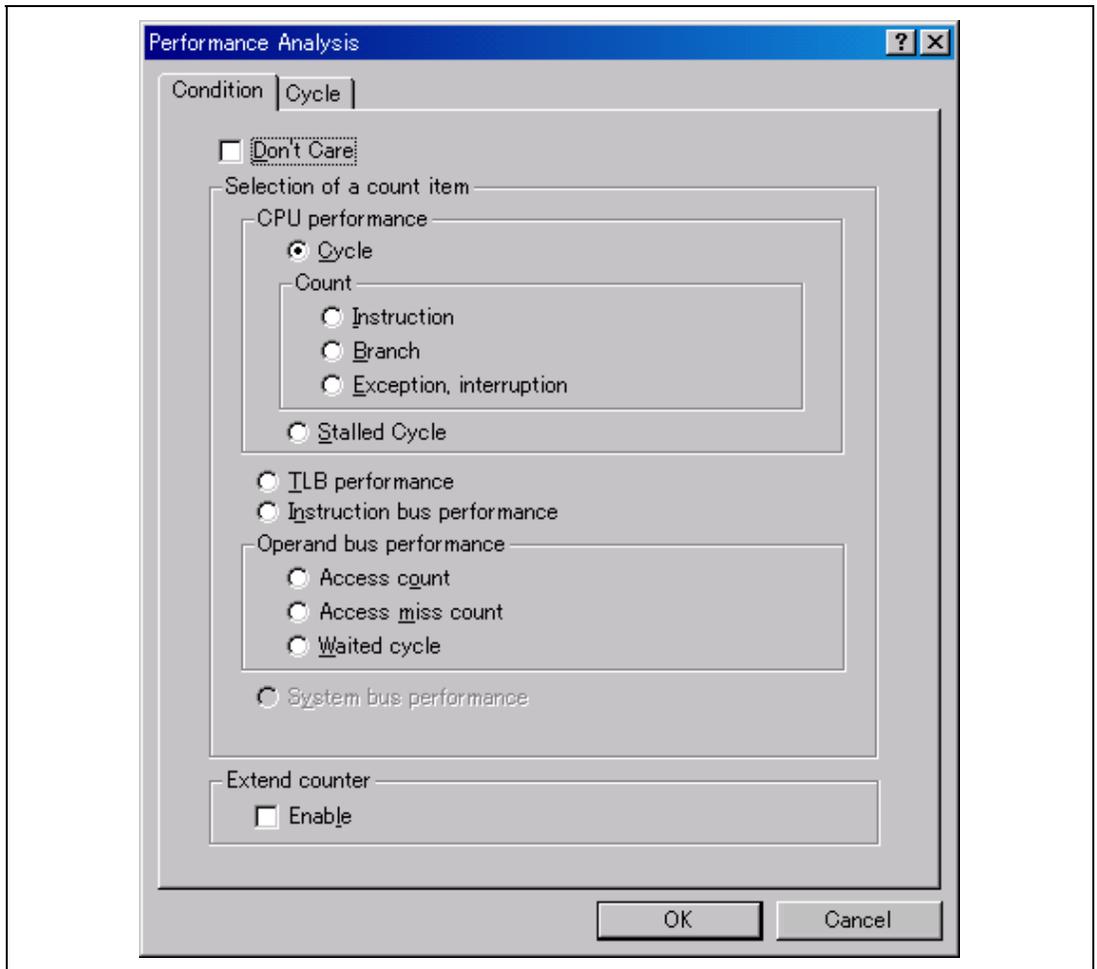

Figure 2.8　[Performance Analysis] Dialog Box

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Note: For the command line syntax, refer to the online help.

(a) Specifying the measurement start/end conditions

Set the performance measurement conditions in the [Action] page after conditions have been set in the [Event Condition] dialog box that is opened by double-clicking Ch1 to Ch6 and Ch8 to Ch12 on the [Event Condition] sheet of the [Eventpoint] window.

Notes: 1. When no measurement start/end conditions are specified, measurement is started by executing a program and ended when an event condition is satisfied.
2. When only the measurement start or end condition is specified, performance cannot be measured. Be sure to specify both of the measurement start and end conditions.
3. When the measurement start/end conditions are specified, step operation cannot be performed.

Table 2.11 Conditions Specified in the [Action] Page

Item		Description
PA1	pa1_start_point	Specifies the conditions of Event Condition that has been set as the measurement start condition of performance channel 1.
	pa1_end_point	Specifies the conditions of Event Condition that has been set as the measurement end condition of performance channel 1.
PA2	pa2_start_point	Specifies the conditions of Event Condition that has been set as the measurement start condition of performance channel 2.
	pa2_end_point	Specifies the conditions of Event Condition that has been set as the measurement end condition of performance channel 2.
PA3	pa3_start_point	Specifies the conditions of Event Condition that has been set as the measurement start condition of performance channel 3.
	pa3_end_point	Specifies the conditions of Event Condition that has been set as the measurement end condition of performance channel 3.
PA4	pa4_start_point	Specifies the conditions of Event Condition that has been set as the measurement start condition of performance channel 4.
	pa4_end_point	Specifies the conditions of Event Condition that has been set as the measurement end condition of performance channel 4.

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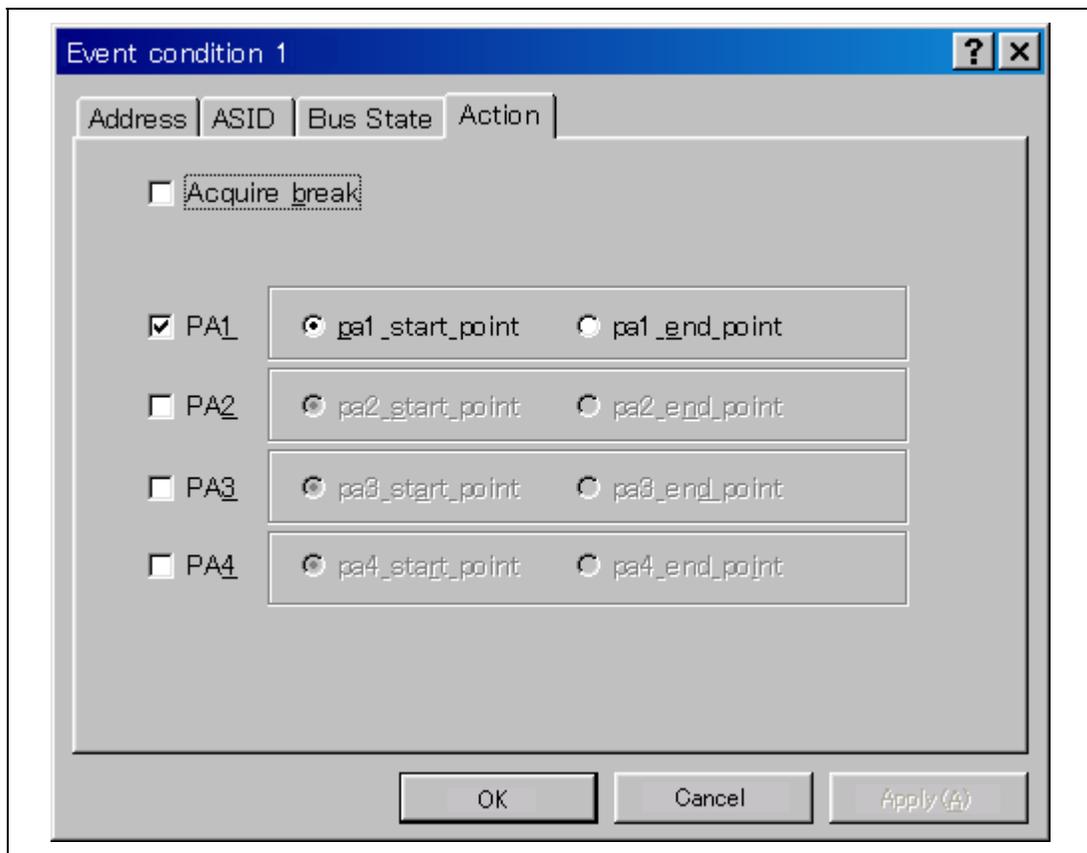
Figure 2.9   [Action] Page

Note: PA1 or PA2 cannot be set for Ch8 and Ch9.

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(b) Measurement tolerance

- The measured value includes tolerance.
- Tolerance will be generated before or after a break.

For details, see table 2.14.

(c) Measurement items

Items are measured in the [Performance Analysis] dialog box for each channel from Ch1 to Ch4. A maximum of four conditions can be specified at the same time. Table 2.12 shows the measurement items. (Options in table 2.12 are parameters for <mode> of the PERFORMANCE_SET command. They are displayed in CONDITION of the [Performance Analysis] window.)

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Table 2.12   Measurement Items

Classification	Type	Measurement Item	Option	Note
Disabled			None	Not measured.
CPU performance	Cycle	Elapsed cycles	AC	Except for power-on period; counted by the CPU clock.
		Cycles executed in privileged mode	PM	The number of privileged-mode cycles among the number of elapsed cycles.
		Cycles for asserting the SR.BL bit	BL	The number of cycles when the SR.BL bit = 1 among the number of elapsed cycles.
	Instruction	Number of effective instructions issued	I	The number of execution instructions = number of valid instructions issued + number of cases of simultaneous execution of two instructions.
				The number of valid instructions means the number of completed instructions.
		Number of 2 instruction executed simultaneously	2I	The number of times that two instructions are executed simultaneously among the valid instructions issued.
	Branch	Number of unconditional branch	BT	The number of unconditional branches other than branches occurring after an exception. However, RTE is counted.
	Exception, interruption	Number of exceptions accepted	EA	Interrupts are included.
		Number of interrupts accepted	INT	NMI is included.
		Number of UBC channel hit	UBC	Performs OR to count the number of channel-hits in the CPU.

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Table 2.12   Measurement Items (cont)

Classification	Type	Measurement Item	Option	Note
CPU performance (cont)	Stalled cycle	Cycles stalled in full-trace mode (with multi-counts)	SFM	All items are counted independently.
		Cycles stalled in full-trace mode (without multi-counts)	SF	This item is not counted if the stall cycle is generated simultaneously with a stall cycle that has occurred due to instruction execution.
TLB performance	TLB	Number of UTLB miss for instruction fetch	UMI	The number of TLB-miss exceptions generated by an instruction fetch (number of EXPEVT sets).
		Number of UTLB miss for operand fetch	UMO	The number of TLB-miss exceptions generated by an operand access (number of EXPEVT sets).
		Number of ITLB miss	IM	The number of ITLB misses for valid accesses (does not include UTLB hits or misses).
Instruction bus performance	Instruction	Number of memory accesses for instruction fetch	MIF	The number of memory accesses by an instruction fetch. Accesses canceled by an instruction-fetch bus are not counted. Instruction fetches, which have been fetched in anticipation of a branch but not actually executed, are counted. Accesses by the PREFI instruction are included.
		Number of instruction cache access	IC	The number of accesses for an instruction cache during memory access of the opcode.

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Table 2.12   Measurement Items (cont)

Classification	Type	Measurement Item	Option	Note
Instruction bus performance (cont)	Instruction (cont)	Number of instruction cache miss	ICM	The number of cache misses by an instruction cache access (the number of accesses to the outside of the CPU core due to a cache miss).
		Number of internal-RAM access for instruction fetch (XY-RAM or L memory)	XL	The number of accesses for the XY memory in the SH7338 during memory accesses of the opcode.
Operand bus performance	Access count	Number of memory access for operand fetch (READ)	MR	The number of memory accesses by an operand read (equal to loading on the operand bus). Accesses by the PREF instruction or canceled accesses are not included.
		Number of memory access for operand fetch (WRITE)	MW	The number of memory accesses by an operand write (equal to storing memory on the operand bus). Canceled accesses are not included.
		Number of operand cache access (READ)	CR	The number of operand-cache reads during memory access (read) of an operand.
		Number of operand cache access (WRITE)	CW	The number of operand-cache reads during memory access (write) of an operand.
		Number of internal-RAM access for operand fetch (READ) (XY-RAM or L memory)	XLR	The number of accesses to XY memory in the SH7338 during memory access (read) of an operand. (Accesses via the XY bus and the operand bus are included. When MOVX and MOVY are executed simultaneously, it increments one count regardless of the read or write.)

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Table 2.12   Measurement Items (cont)

Classification	Type	Measurement Item	Option	Note
Operand bus performance (cont)	Access count (cont)	Number of internal-RAM access for operand fetch (WRITE) (XY-RAM or L memory)	XLW	The number of accesses to XY memory in the SH7338 during memory access (write) of an operand. (Accesses via the XY bus and the operand bus are included. When MOVX and MOVY are executed simultaneously, it increments one count regardless of the read or write.)
		Number of U-RAM access (READ)	UR	The number of U-memory accesses during memory access (read) of an operand. (Accesses via the cache are not included.)
		Number of U-RAM access (WRITE)	UW	The number of U-memory accesses during memory access (write) of an operand. (Accesses via the cache are not included.)
	Access miss count	Number of operand cache miss (READ)	CMR	The number of cache misses by an operand cache access (read) (number of accesses to the outside of the CPU core due to a cache miss). Cache misses are not counted by the PREF instruction.
		Number of operand cache miss (WRITE)	CMW	The number of cache misses by an operand cache access (write) (number of accesses to the outside of the CPU core due to a cache miss). Write-through accesses are not counted. Cache misses are not counted by the PREF instruction.
		Number of U-RAM read-buffer miss	UBM	

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Table 2.12   Measurement Items (cont)

Classification	Type	Measurement Item	Option	Note
Operand bus performance (cont)	Waited cycle	Waited cycles for operand fetch (READ)	WOR	The number of wait cycles by a memory access (read) of an operand.
		Waited cycles for operand fetch (WRITE)	WOW	The number of wait cycles by a memory access (write) of an operand.
		Waited cycles for operand cache miss (READ)	WCMR	The number of wait cycles by an operand cache miss (read) (however, the number of wait cycles of cache FIII is included due to contention).
		Waited cycles for operand cache miss (WRITE)	WCMW	The number of wait cycles by an operand cache miss (write).
System bus performance (only available for Ch3 and Ch4)	System bus	Number of requests	RQ	The number of valid bus cycles (cells) is counted by the system bus clock.
		Number of responses	RS	The number of valid bus cycles (cells) is counted by the system bus clock.
		Waited cycles for request	WRQ	The cycles for an issued request (req), that no acceptance signal (gnt) is issued to, are counted by the system bus clock.
				Even if the waits are issued simultaneously for multiple requests, they are counted as 1.
		Waited cycles for response	WRS	The cycles for an issued response (r_req), that no acceptance signal (r_gnt) is issued to, are counted by the system bus clock.
				Even if the waits are issued simultaneously for multiple requests, they are counted as 1.

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Table 2.13 shows the measurement items and methods that are mainly used.

Table 2.13   Main Measurement Items

Main Measurement Item	Measurement Method
Elapsed time	Number of elapsed cycles x CPU clock cycles
Number of execution instructions	Number of valid instructions issued + number of cases of simultaneous execution of two instructions
Number of interrupts accepted	Number of exceptions accepted
Number of instruction fetches (for both cache and non-cache)	Number of memory accesses in an opcode
Instruction-cache hit ratio	(Number of instruction-cache accesses– instruction-cache miss counts)/instruction-cache access counts
Number of operand accesses (for both cache and non-cache)	Number of memory accesses in an operand (read) + number of memory accesses in an operand (write)
Operand-cache hit ratio (read)	(Number of operand-cache accesses (read) – number of operand-cache misses (read))/number of operand-cache accesses (read)
Operand-cache hit ratio (write)	(Number of operand-cache accesses (write) – number of operand-cache misses (write))/ number of operand-cache accesses (write)
Operand-cache hit ratio	(Number of operand-cache accesses (read) + number of operand-cache accesses (write) – number of operand-cache misses (read) – number of operand-cache misses (write))/(number of operand-cache accesses (read) + number of operand-cache accesses (write))
System bus: occupied rate of request bus	(The equivalent CPU clock value of the number of requests)/number of elapsed cycles
System bus: occupied rate of response bus	(The equivalent CPU clock value of the number of responses)/number of elapsed cycles

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Each measurement condition is also counted when conditions in table 2.14 are generated.

Table 2.14   Performance Measurement Conditions to be Counted

Measurement Condition	Notes
No caching due to the settings of TLB cacheable bit	Counted for accessing the cacheable area.
Cache-on counting	Accessing the non-cacheable area is counted less than the actual number of cycles and counts. Accessing the cacheable, X/Y-RAM, and U-RAM areas is counted more than the actual number of cycles and counts.
Branch count	The counter value is incremented by 2. This means that two cycles are valid for one branch.

Notes: 1. In the non-realtime trace mode of the AUD trace and memory output trace, normal counting cannot be performed because the generation state of the stall or the execution cycle is changed.
2. Since the clock source of the counter is the CPU clock, counting also stops when the clock halts in the sleep mode.

(d) Extension setting of the performance-result storing counter

The 32-bit counter stores the result of performance, and two counters can be used as a 64-bit counter.

To set a 64-bit counter, check the [Enable] check box in the [Extend counter] group box of the [Performance Analysis] dialog box for Ch1 and Ch3.

2. Displaying the result of performance

The result of performance is displayed in the [Performance Analysis] window or the PERFORMANCE_ANALYSIS command in hexadecimal (32 bits).

However, when the extension counter is enabled, it is displayed in hexadecimal (64 bits).

Note: If a performance counter overflows as a result of measurement, "********" will be displayed.

3. Initializing the measured result

To initialize the measured result, select [Initialize] from the popup menu in the [Performance Analysis] window or specify INIT with the PERFORMANCE_ANALYSIS command.

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