

# ISL6334EVAL1Z User Guide

## Board Specifications

1. Intel VR11.1 compliant.
2. 4-Phase, 130W, 400kHz, Load Line = 0.8mΩ.
3. Socket: LGA1366, die sensing, can be configured for motherboard sensing.
4. 6 Layer Board: Top/Bottom - 0.5oz plated, 1.5oz finished; Internal Layer – 1oz.
5. Dual footprint for Intersil 12V (ISL6612A, ISL6622) and 5V drivers (ISL6596/ISL6620) for cost or efficiency optimization. With minor re-work, the board can also operate 12V drive for high-side MOSFET and 5V drive for low-side MOSFET.
6. Dual footprint for PowerPak and DPAK MOSFET for cost or efficiency optimization.

## ISL6334EVAL1Z Board Brief Description

### Control Power Supply

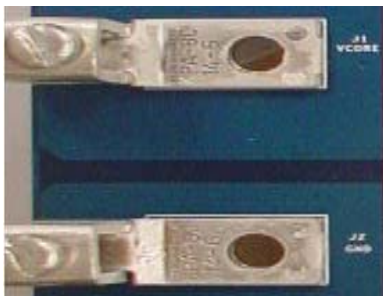
There are two ways to provide 5VDC to this evaluation board: through ATX power connectors (J21) or Banana connectors (J5 and J0). SW1 is used to control the ATX silver box power supply.



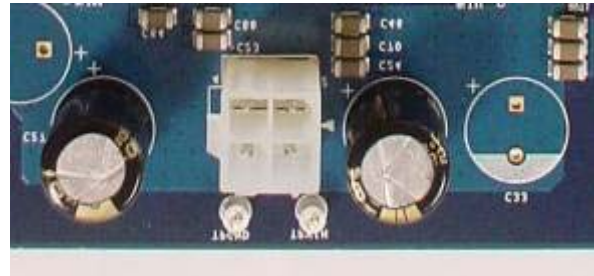
**FIGURE 1.**

### Input Power Supply and External Load Connector

12VDC input power supply can be connected to the board through the 4-pin ATX connector J4. Two test points, TPVIN and TPGND, are provided for input voltage measurement. Two connectors (J1 and J2) are provided for external load.



**FIGURE 2.**



**FIGURE 3.**

### VR Enable Switch

One switch (SW2) is provided for EN\_VTT signal control. In "OFF" position, EN\_VTT signal is shorted to ground and ISL6334 is disabled. Place SW2 in the "ON" position to enable operation.



**FIGURE 4.**

### PGOOD Indicator and Test Points

CR2 is used to indicate the status of VR\_RDY (PGOOD) signal. When VR\_RDY is high, the LED in CR2 will be OFF (no light); otherwise the red LED in CR2 will be on once 5V is applied.

Test points are provided for VR\_RDY, IMON, VR\_HOT and VR\_FAN signals.



**FIGURE 5.**

## VID (Figure 7)

VID code can be generated from Demo board (JP9 = DEMO) or VTT tool (JP9 = VTT).

## PSI

Dynamic PSI signal can be generated from LGA1366 VTT or external function generator. Static, fixed PSI operation can be set through SW5. Placing the 0 switch in the "N" position, leads to the circuit operating in PSI mode.

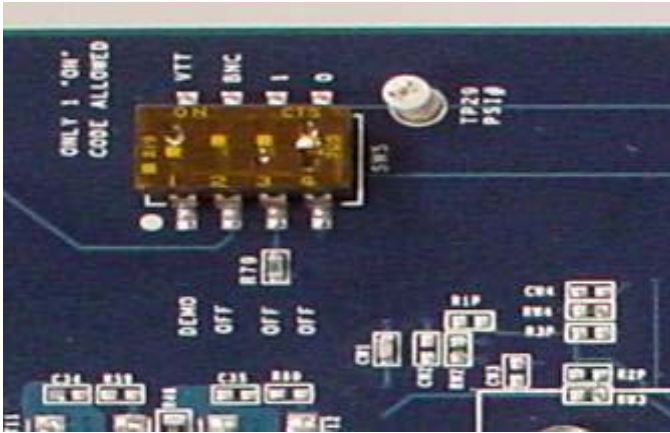


FIGURE 6.

## Phase Count Control

R1P, R2P, R3P, RW2, RW3, and RW4 are used to set the phase count, as shown in Table 1. If phase count is different than 4, R1 and R5 must be adjusted accordingly for stability and correct load line.

TABLE 1.

	R3P	R2P	R1P	RW4	RW3	RW2
4-Phase	DNP	DNP	DNP	0Ω	0Ω	0Ω
3-Phase	0Ω	DNP	DNP	DNP	0Ω	0Ω
2-Phase	X	0Ω	DNP	DNP	DNP	0Ω
1-Phase	X	X	0Ω	DNP	DNP	DNP

NOTE: X = Don't care.

## Available Design Assist Tools

1	Layout Check list.
2	VR Design Worksheet.
3	V <sub>CORE</sub> and IMON TOB Calculator.
4	Schematic is available in OrCAD format.
5	Layout is available in Allegro format.

Contact Intersil's local office or field support for the latest available information.

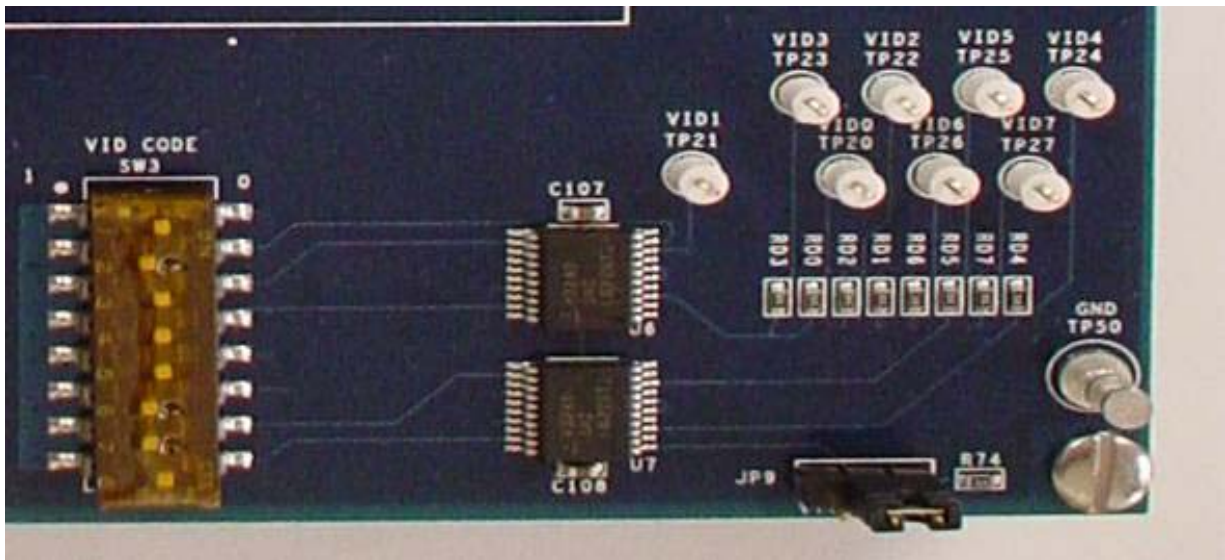
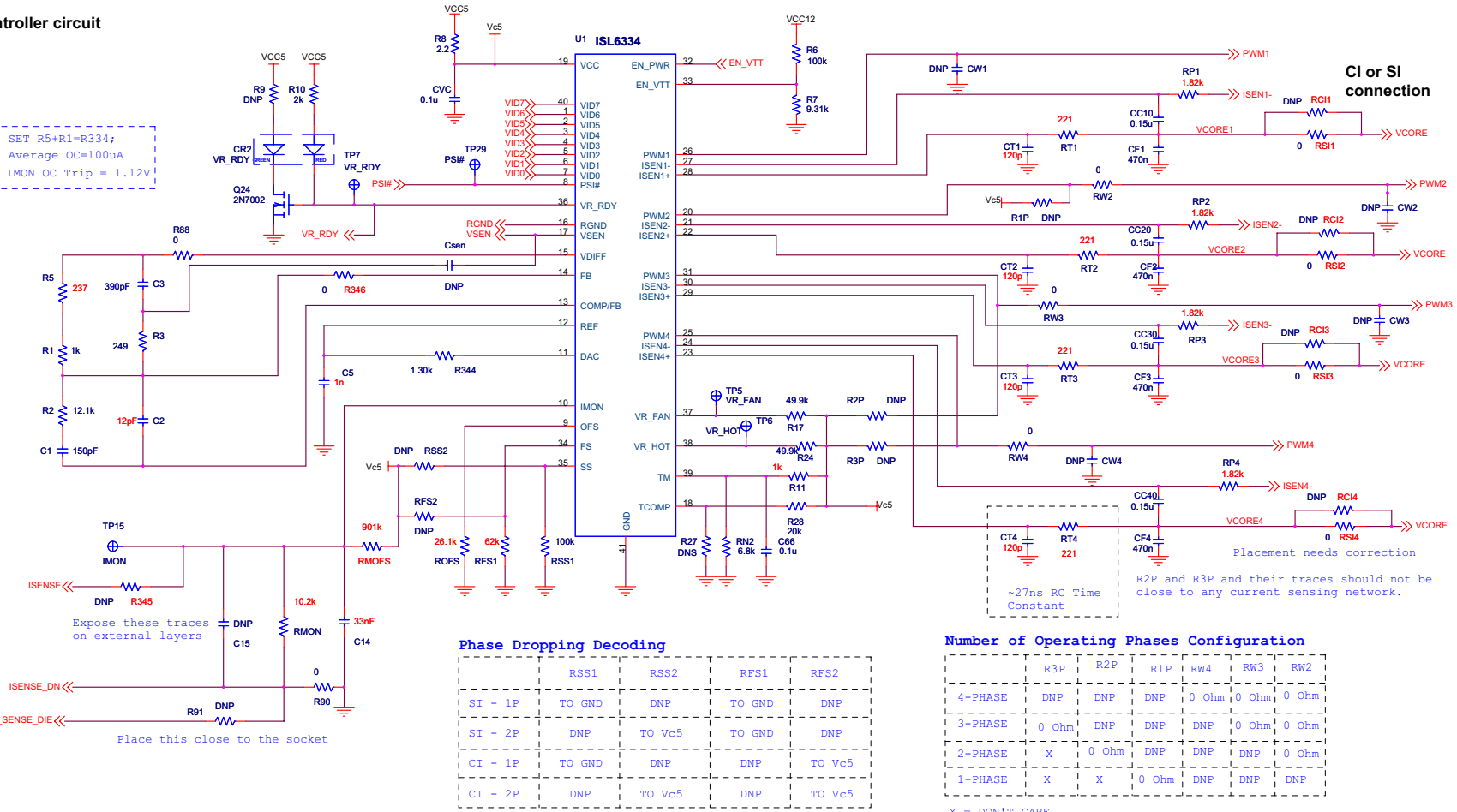


FIGURE 7.

# ISL6334EVAL1Z Schematics

## Controller circuit

SET R5+R1=R334;  
Average OC=100uA  
IMON OC Trip = 1.12V



Expose these traces on external layers

Place this close to the socket

Placement needs correction

R2P and R3P and their traces should not be close to any current sensing network.

~27ns RC Time Constant

### Phase Drooping Decoding

	RSS1	RSS2	RFS1	RFS2
SI - 1P	TO GND	DNP	TO GND	DNP
SI - 2P	DNP	TO Vc5	TO GND	DNP
CI - 1P	TO GND	DNP	DNP	TO Vc5
CI - 2P	DNP	TO Vc5	DNP	TO Vc5

RN2 = Vishay, NTHS0805N02N6B01  
SI = Un-coupled Inductor  
CI = Coupled Inductor

### Number of Operating Phases Configuration

	R3P	R2P	R1P	RW4	RW3	RW2
4-PHASE	DNP	DNP	DNP	0 Ohm	0 Ohm	0 Ohm
3-PHASE	0 Ohm	DNP	DNP	DNP	0 Ohm	0 Ohm
2-PHASE	X	0 Ohm	DNP	DNP	DNP	0 Ohm
1-PHASE	X	X	0 Ohm	DNP	DNP	DNP

X = DON'T CARE  
Drop (R1+R5) and compensation network must be adjusted accordingly.

FIGURE 8. ISL6334 BURNSIDE - 130W REV C BOARD, CONTROLLER CIRCUIT

# ISL6334EVAL1Z Schematics (Continued)

## Power Stage

Follow Intel Burside ATX Layout Guideline for Power Stage and LGA1366 Socket as well as Input Bus Line (1080 pre-preg stackup, 6 layers)  
 Dual footprint for SI and CI - Expose Output Inductor Copper  
 Dual footprint - LPAK/DPAK for High-side (T/B) and Low-Side (B/T)  
 CI: Phase1 (Thermistor) + Phase3 ; Phase2 + Phase4  
 Default - 12VUG, LDO=LG. Hardware Options: 12VUG5VLG; LDO=UGLG; 5V DRIVER

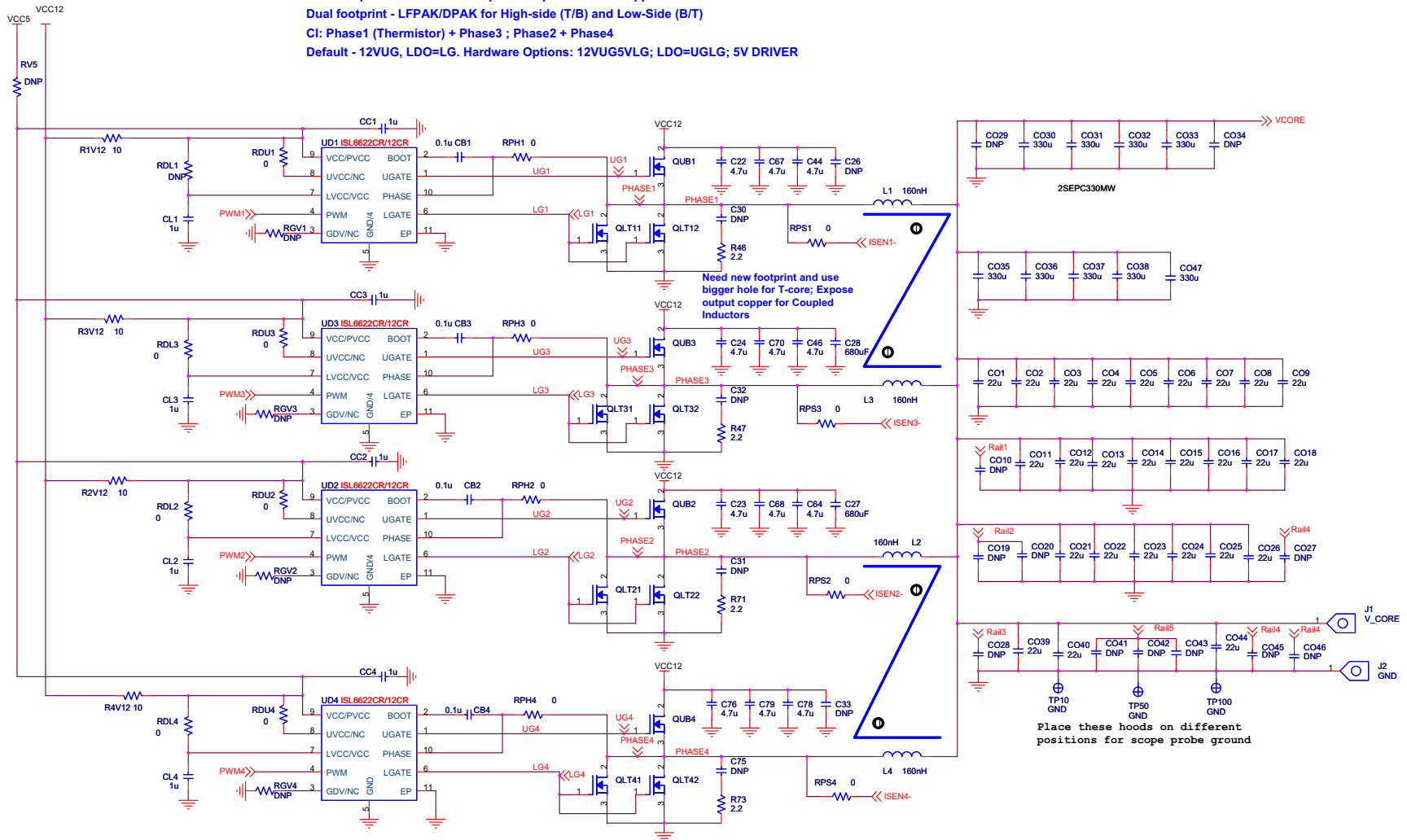
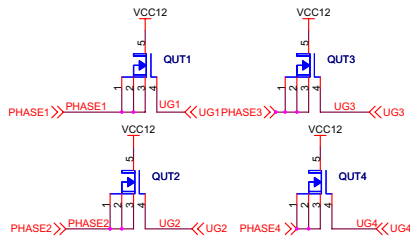


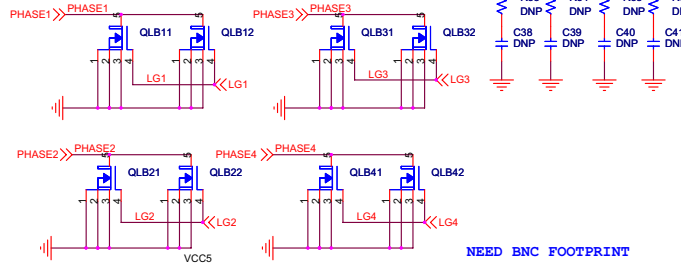
FIGURE 9. ISL6334 BURNSIDE - 130W REV C BOARD, POWER STAGE

# ISL6334EVAL1Z Schematics (Continued)

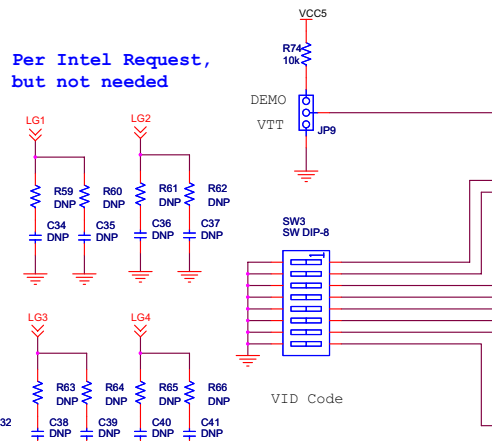
Place These FETs on Top Side for Intel Burnside CRB Design



Place These FETs on Bottom Side for Intel Burnside CRB Design (Depending on the Layout, we might drop this)

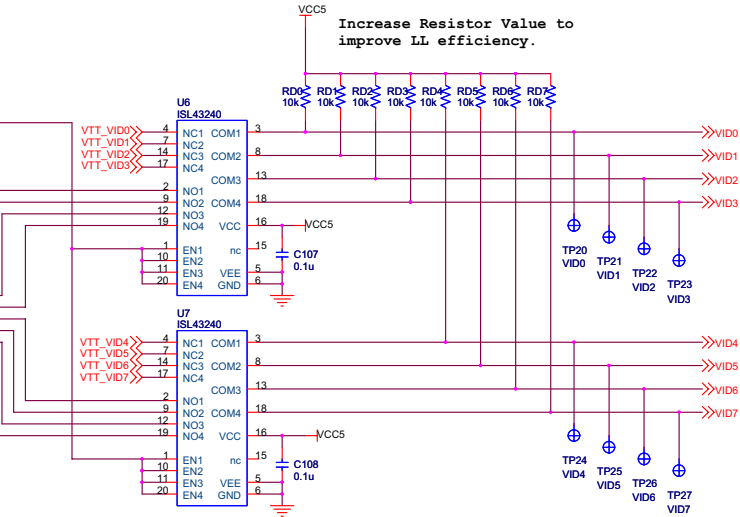


VID generator, LGA1366 socket and input connectors

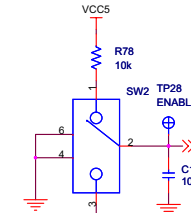


Per Intel Request, but not needed

Increase Resistor Value to improve LL efficiency.



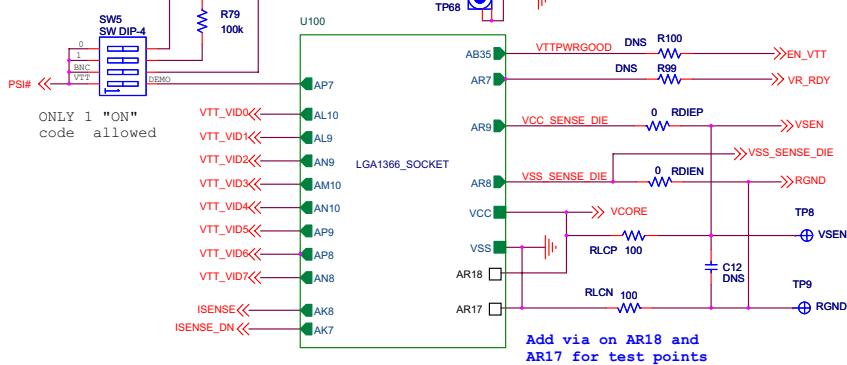
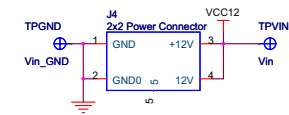
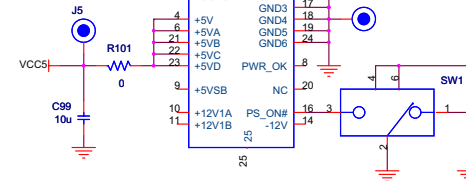
VID Code



NEED BNC FOOTPRINT



Use Intersil/VTT Interposer for DCLL Measurement



Add via on AR18 and AR17 for test points

FIGURE 10. ISL6334 BURNSIDE - 130W REV C BOARD

# ISL6334EVAL1Z Schematics (Continued)

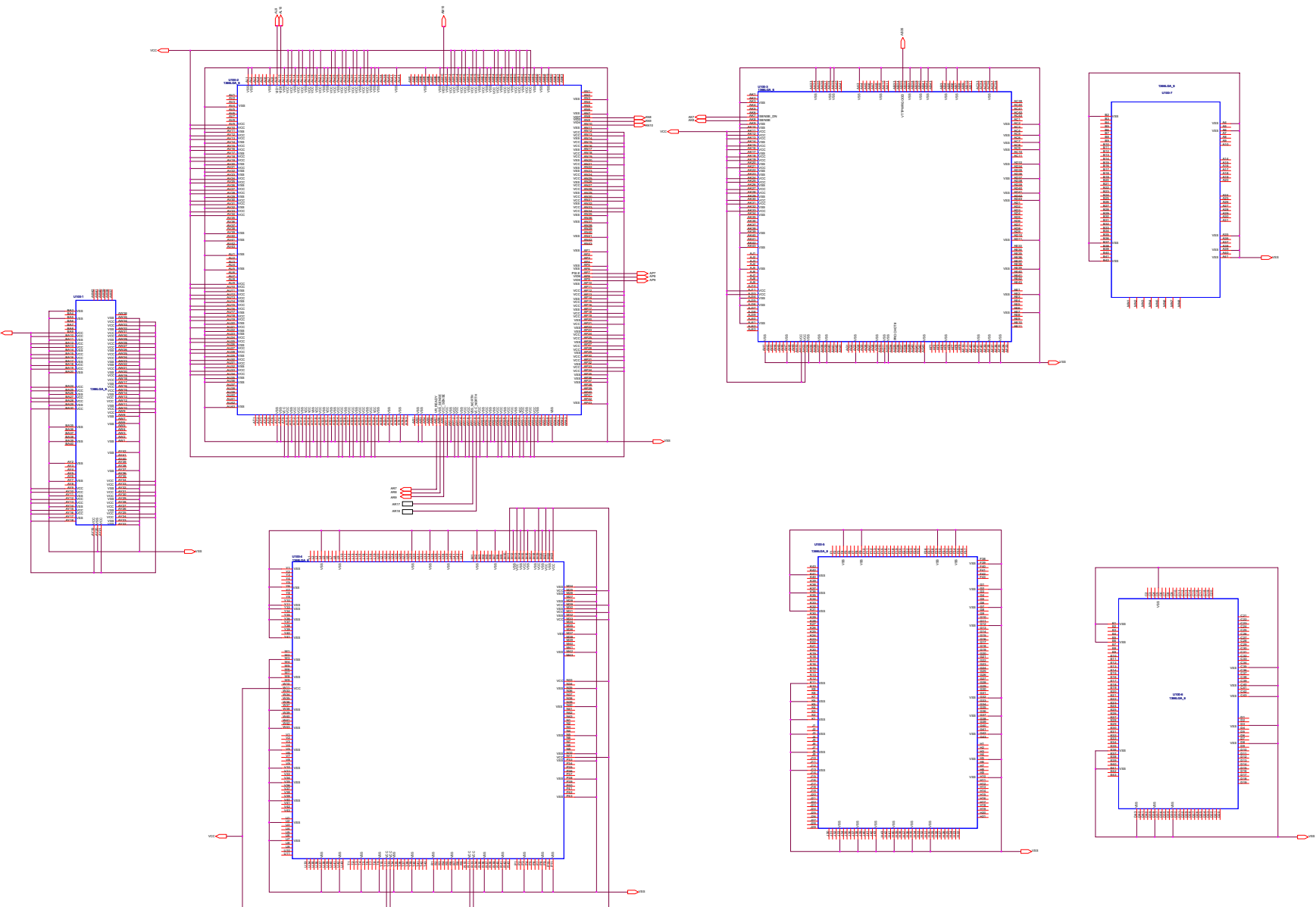


FIGURE 11. LGA1366 SOCKET PINOUT

ISL6334EVAL1Z Board Layout

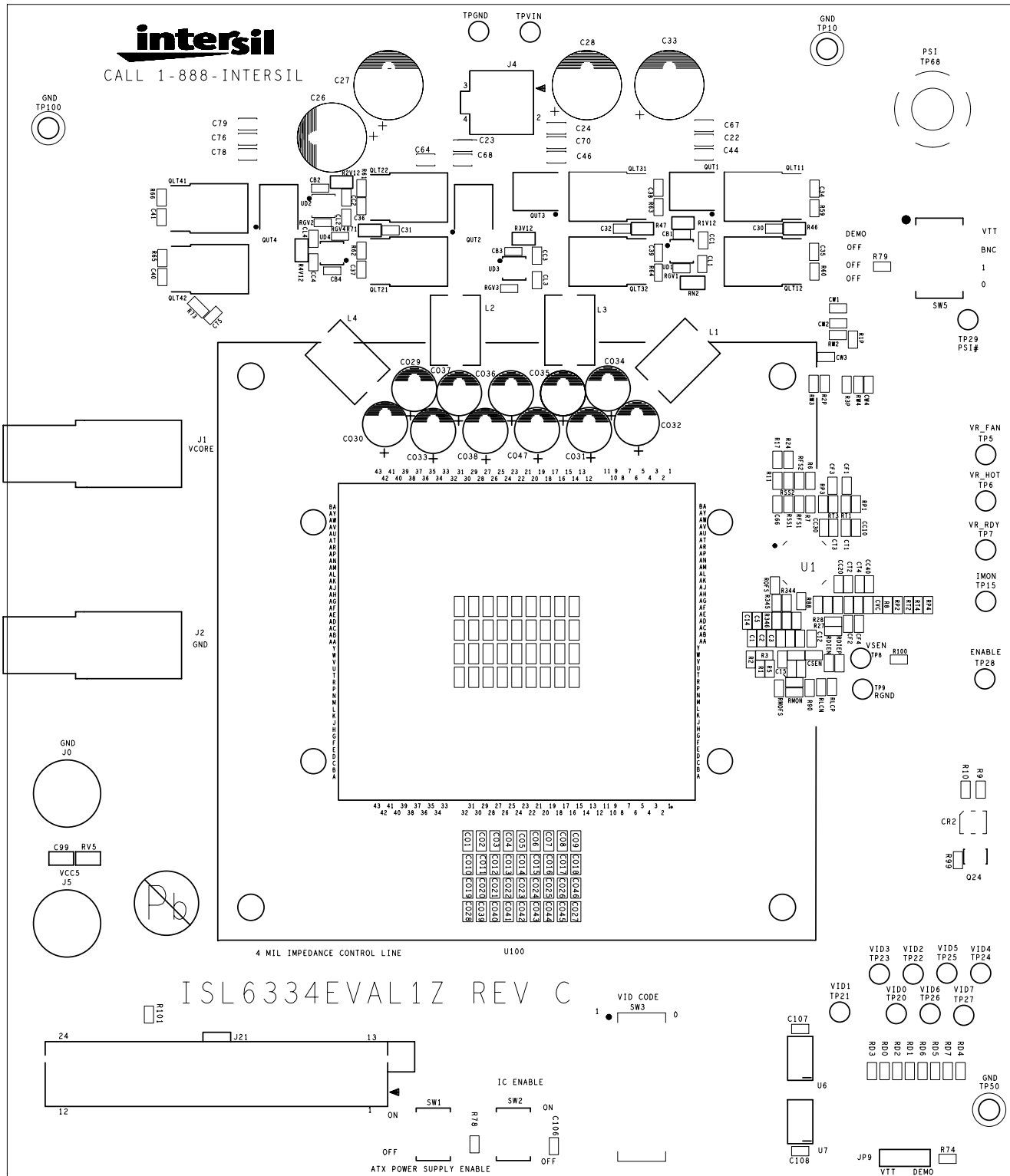


FIGURE 12. TOP SILKSCREEN

ISL6334EVAL1Z Board Layout (Continued)

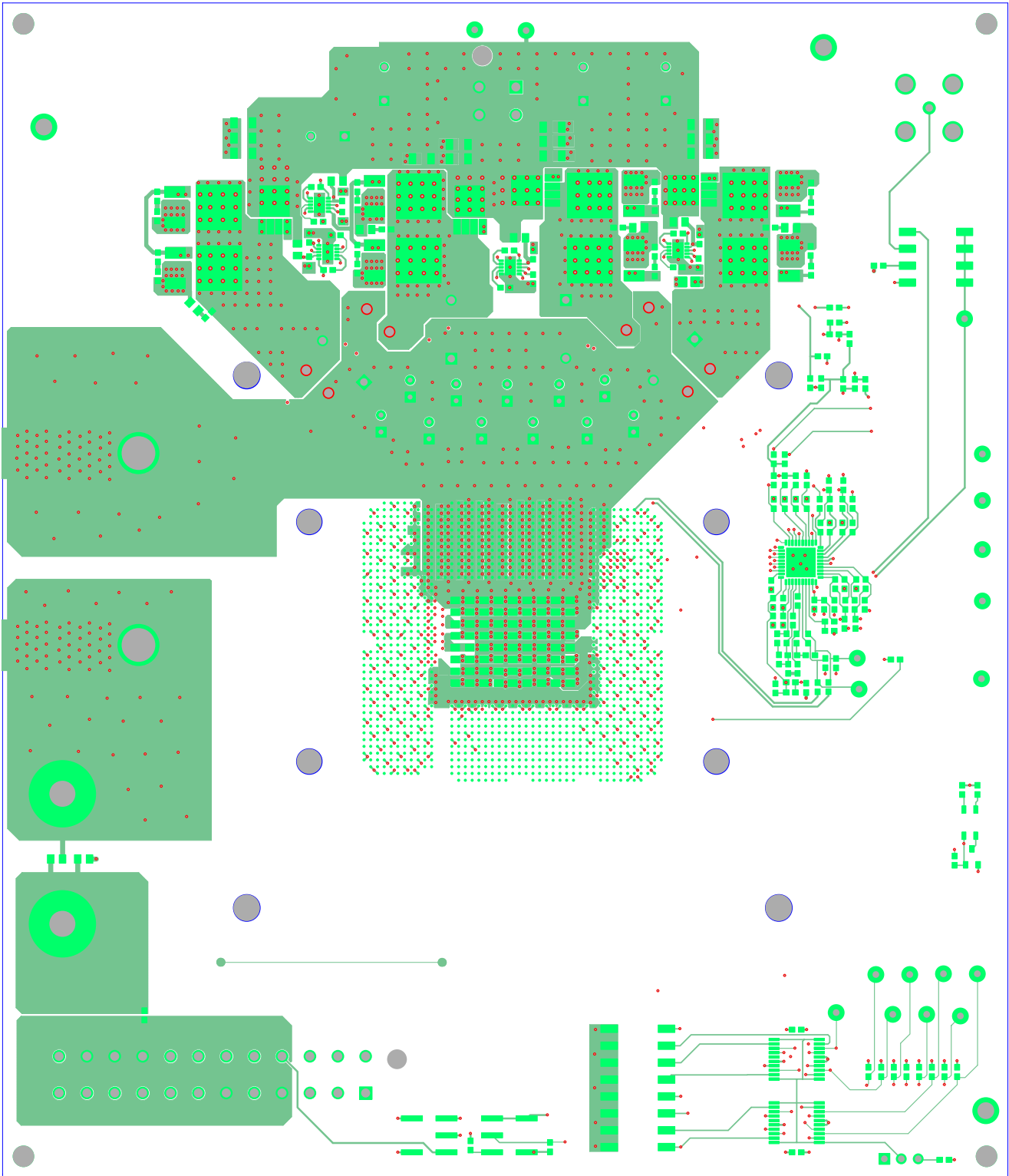


FIGURE 13. TOP COMPONENT SIDE



ISL6334EVAL1Z Board Layout (Continued)

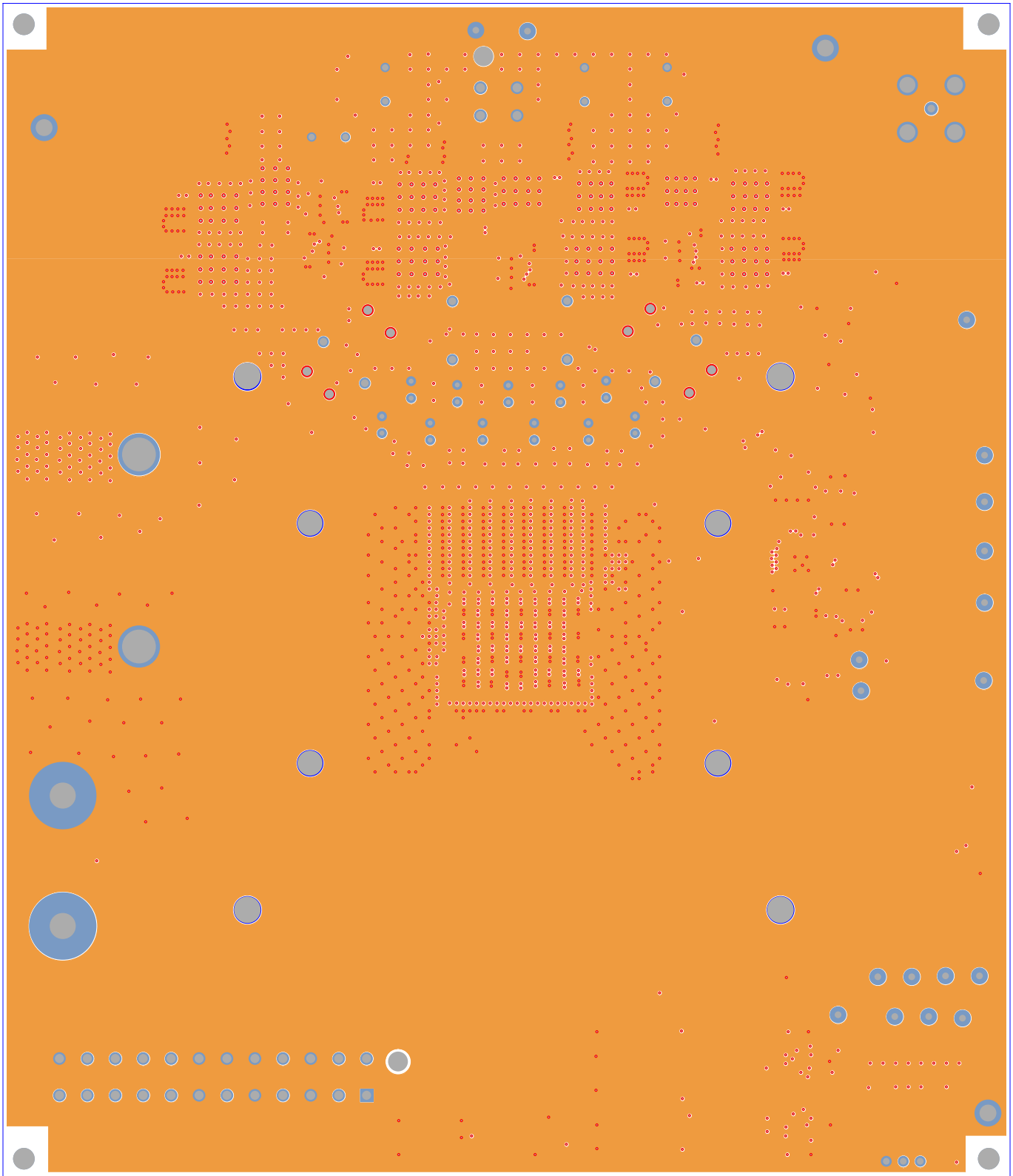


FIGURE 14. INTERNAL PLANE L2

ISL6334EVAL1Z Board Layout (Continued)

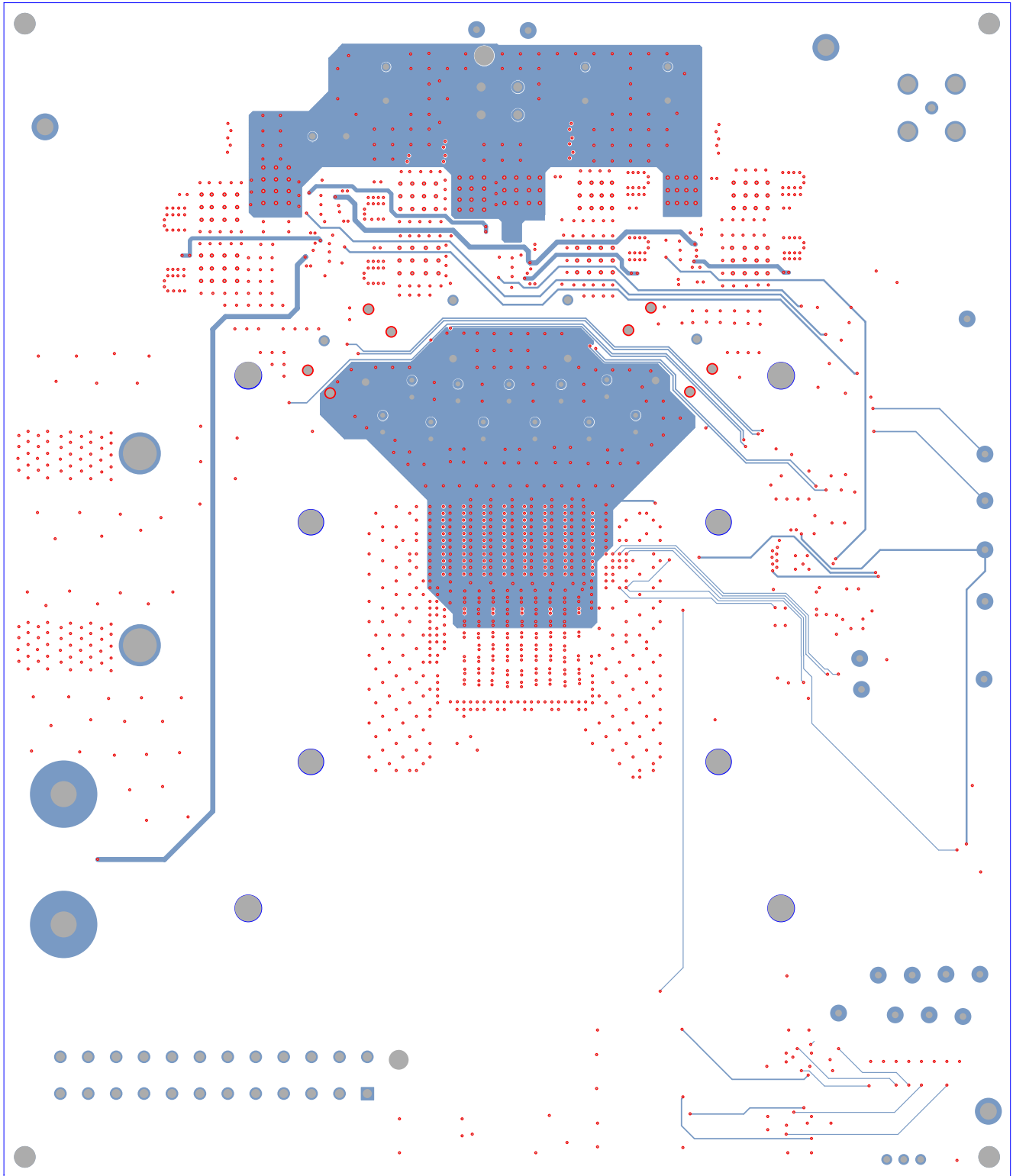


FIGURE 15. INTERNAL ETCH L3

ISL6334EVAL1Z Board Layout (Continued)

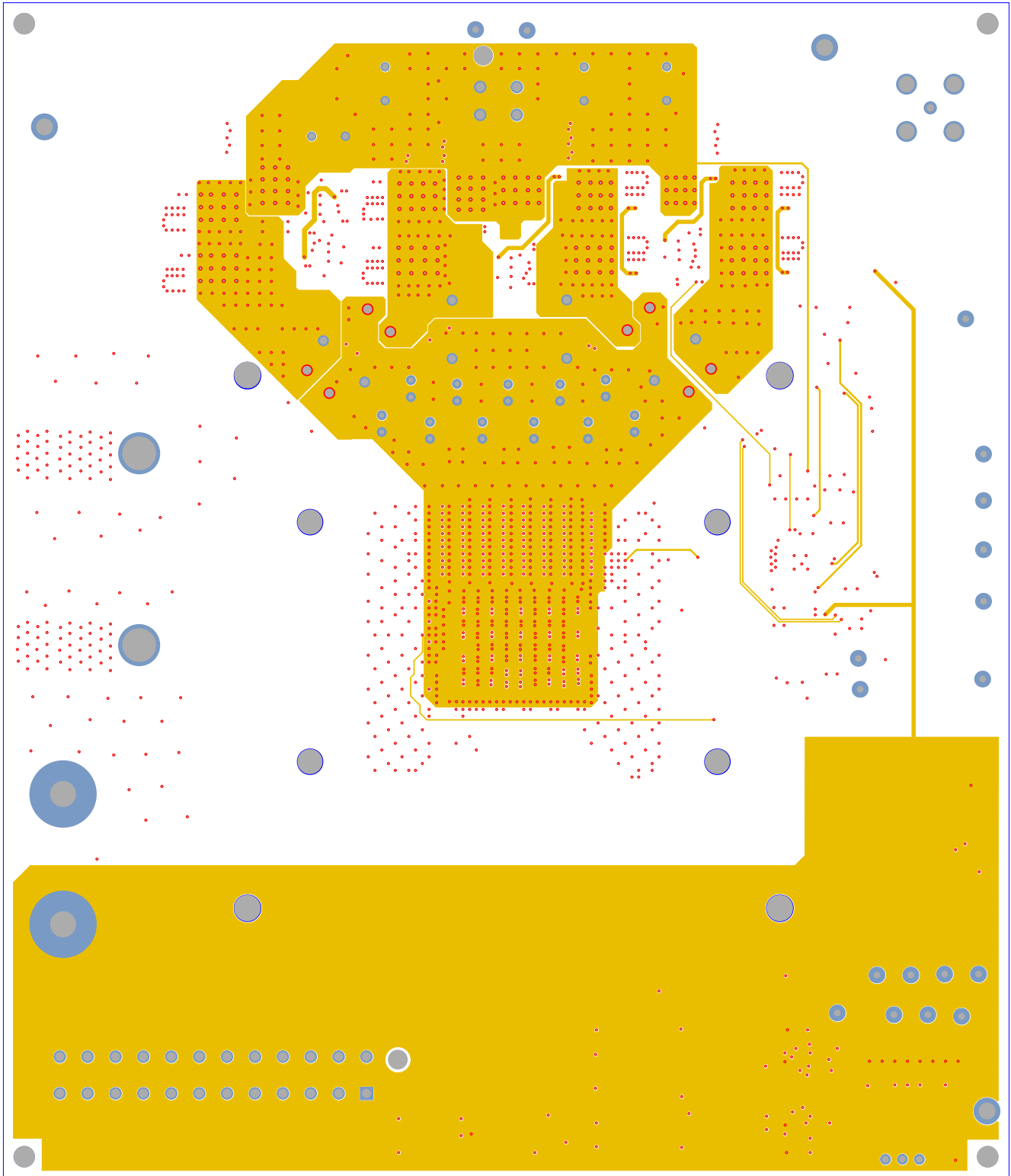


FIGURE 16. INTERNAL ETCH L4

ISL6334EVAL1Z Board Layout (Continued)

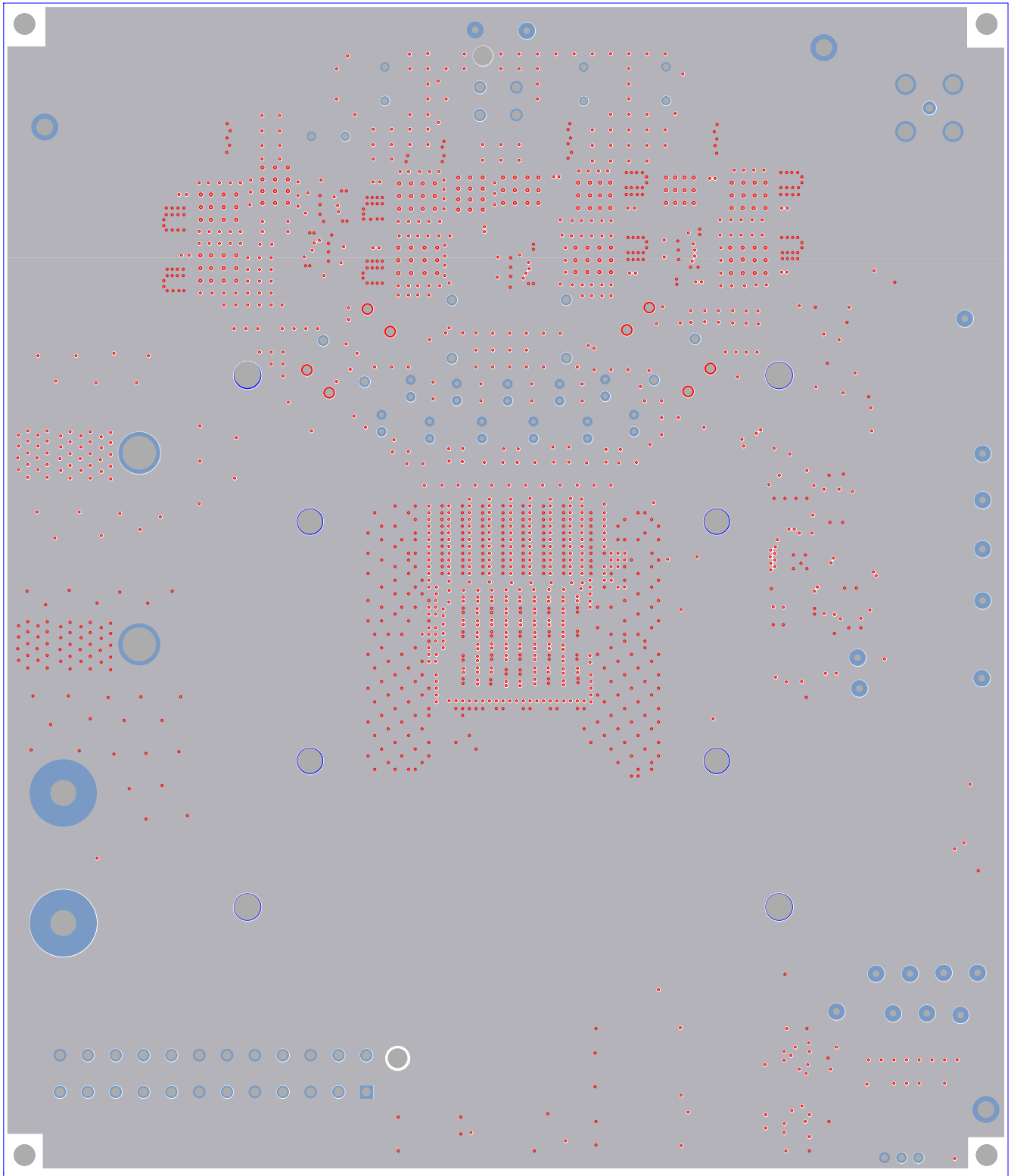


FIGURE 17. INTERNAL PLANE L5

ISL6334EVAL1Z Board Layout (Continued)

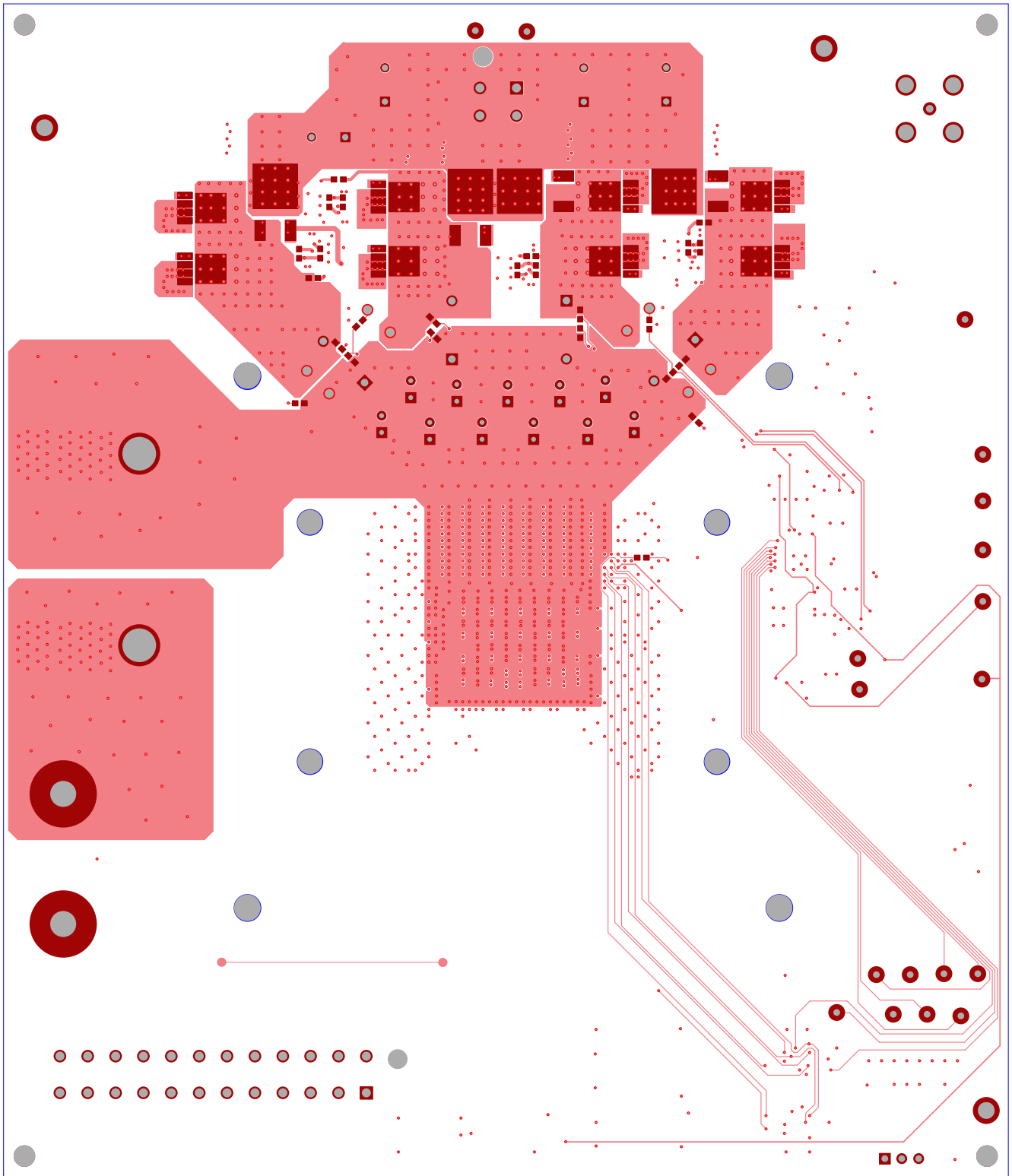


FIGURE 18. SOLDER SIDE BOTTOM

ISL6334EVAL1Z Board Layout (Continued)

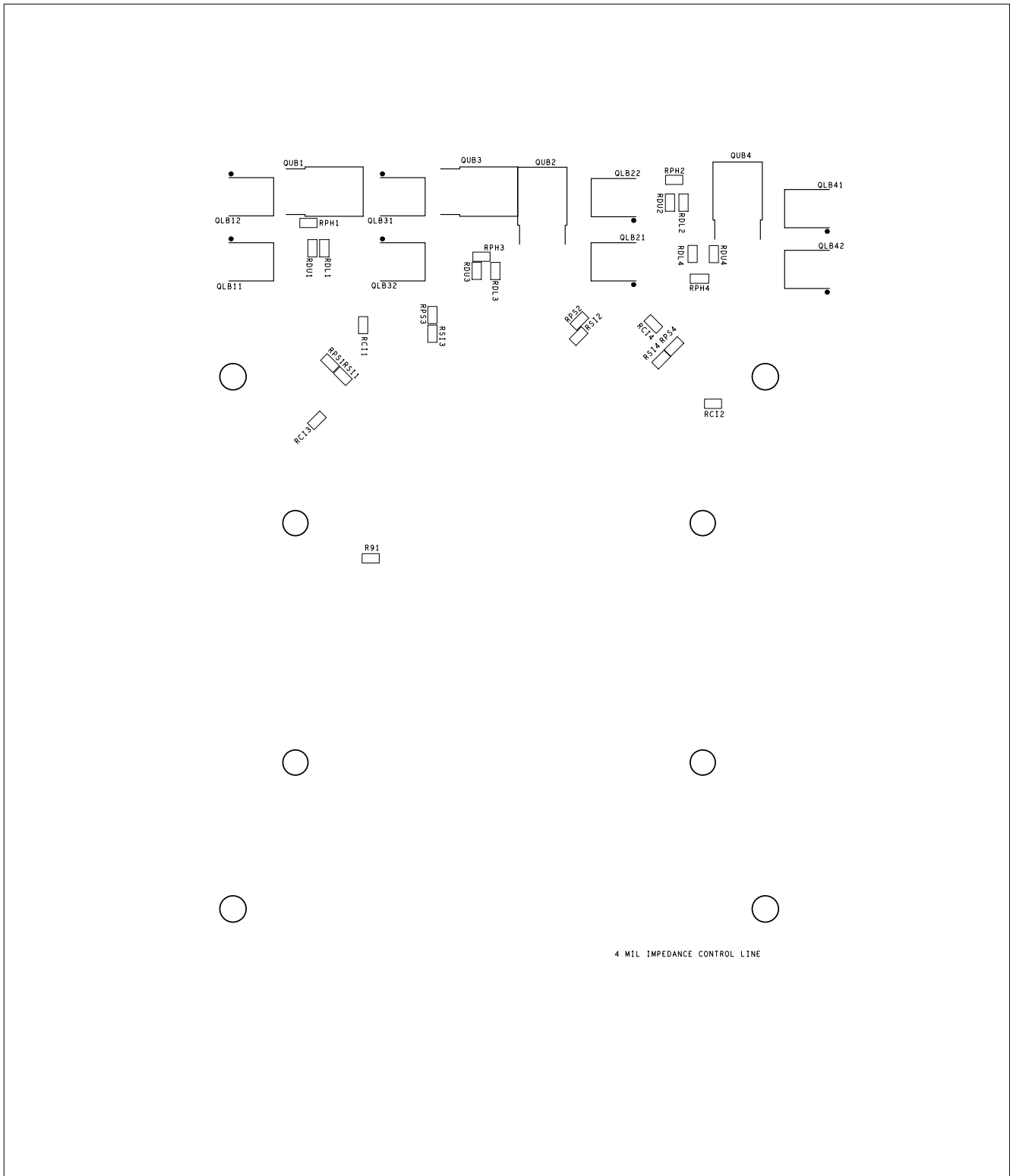


FIGURE 19. SILKSCREEN BOTTOM

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