Intersil Legacy Nomenclature Guide

Contents

ISL Types

ISL X XXXX X I XX X XXX Z -T

PREFIX

FAMILY DESIGNATOR
1: DSL, RTC, Clocks, ATE, Energy LED Lighting
2: Reference, DCPs, Buffers, Sensors, Precision Op Amp, Precision ADC & DAC
3: Interface, Data Communication
4: Analog Component Solutions
5: High Speed Amps, Switch/MUX, ADCs, DACs, Optical, Video, Telecom VoIP, DSP Function Specific
6: Desktop Power
7: Space, Auto
8: Analog Switches, General Purpose Power
9: Notebook, Handheld
A: High Speed ADCs

PART NUMBER
3 to 5 Digits

OPTION
E: 15kV ESD Protected DCP Resistance Options
W: 10k
U: 50k
T: 100k

TEMPERATURE RANGE
C: 0°C to +70°C (Commercial)
D: 0°C to +85°C
H: -10°C to +100°C (Hi-Temp Comm.)
E: -20°C to +85°C (Extended Comm.)
I: -40°C to +85°C (Industrial)
A: -40°C to +105°C (Automotive)
F: -40°C to +125°C (Full-range Industrial)
P: -40°C to +130°C (Power Supply)
M: -55°C to +125°C (Military)
RHV: QML Class V (Radiation Hardened)
RHQ: QML Class Q (Radiation Hardened)
RHT: QML Class T (Radiation Hardened)
EHV: QML Class V (Radiation Hardened)
EHQ: QML Class Q (Radiation Hardened)
EHT: QML Class T (Radiation Hardened)

PACKAGE DESIGNATOR
A: Shrink Small Outline Plastic (SSOP/QSOP)
AR: Quad Flat No-Lead (Punch QFN with Wettable Flank)
B: Small Outline Plastic (SOIC)
BE: Exposed Pad SOIC (EPSOIC)
C: Available
D: Ceramic Dual-In-Line Metal Seal (SBDIP)
E: Small Outline Transistor Plastic (SC-70)
F: Ceramic Flatpack
FE: Ceramic Flatpack w/Heatsink
G: Single In-line Plastic (SIP) TO-220
GS: Single In-line Plastic, Surface Mount (SIP) TO-263
H: Small Outline Transistor Plastic (SOT-23)
HT: Thin Small Outline Transistor Plastic (TSOT)
I: Chip Scale Package (CSP)
J: Ceramic Dual-In-Line Frit Seal (CERDIP)
K: Ball Grid Array (FBGA/PBGA/LGA)
KE: Heat Sink Ball Grid Array (HBGA)
KV: Very Thin Fine Pitch BGA (VFBGA)
L: Ceramic Leadless Chip Carrier (CLCC, SMD 0.5)
M: Plastic Leaded Chip Carrier (PLCC)
N: Thin Plastic Quad Flatpack (TQFP/LQFP)
NE: Thin Plastic Quad Flatpack (TQFP/LQFP w/Exposed Pad)
O: Do Not Use
P: Dual-In-Line Plastic (PDIP)
Q: Metric Plastic Quad Flatpack (MQFP/PQFP)
R: Quad/Dual Flat No Lead (QFN/DFN)/HDA (High Density Array)
RA: Array Flat No Lead (AFN)
RO: Optical Quad/Dual Flat No Lead (OQFN/ODFN)
ROM: Optical Quad/Dual Flat No Lead Module
RT: Thin Quad/Dual Flat No Lead (TQFN/TDFN)
RU: Ultra Thin Quad/Dual Flat No Lead (UTQFN/UTDFN/ePad UTQFN)
RS: Top Exposed Pad QFN (TEPQFN)
RX: Extreme Thin Flat No Lead (X2DFN/X2QFN)
S: Header (TO-257)
T: Metal Can (TO-39)
U: Mini Small Outline Package (MSOP)
UE: Thermally Enhanced Mini Small Outline Package (HMSOP)
UO: Optical Mini Small Outline Package (OSOP)
V: THIN Shrink Small Outline Plastic (TSSOP)
VE: Thermally Enhanced Thin Shrink Small Outline Plastic (HTSSOP/EPTSSOP)
W: Wafer Sale
WMB: Wafer Sale With Solderable Metal Backing Layer
XM: Die Sale, Military Visual (Condition B)
XC: Die Sale, Commercial Visual
XB: Die Sale, Bumped Die (FCP)
Y: Available
Z: Do Not Use

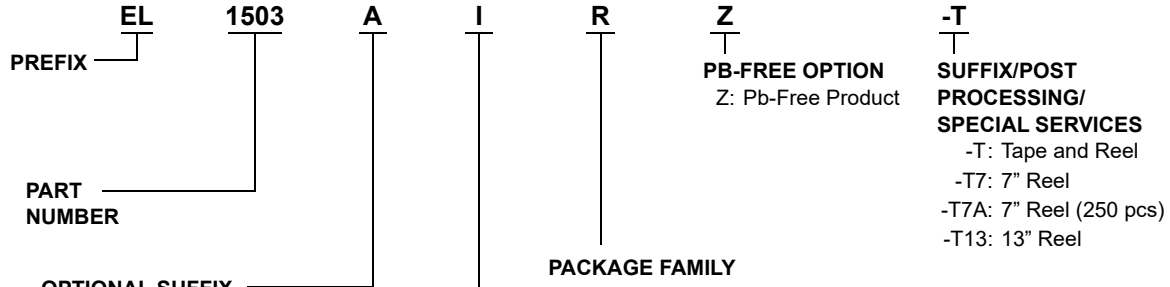
OPTIONAL ELECTRICAL GRADE
To Denote Speed or Precision Grading as Defined in Datasheet

SPECIAL SELECTIONS
Optional Characters to Denote Operating Conditions or Package Options:
18: 1.8V
33: 3.3V
EP: Enhanced Product (DLA Vendor Item Drawing)
EPZ: Enhanced Product w/100% Matte Tin Lead Finish
A, B etc.: Firmware revision. This will not appear on part marking

PB-FREE OPTION
Z: ROHS and IEC61249-2-21 Halogen Free

SUFFIX/ POST PROCESSING/ SPECIAL SERVICES
-T: Tape and Reel
-T1: Tape and Reel
-T2: Tape and Reel w/Vacuum Pack
-T7: 7” Reel
-TS: 7” Reel, 100pc.
-T7A: 7” Reel, 250pc.
-T13: 13” Reel
-T5: 500pc Tape and Reel
-TK: 1,000pc Tape and Reel
-T5K: 5,000pc Tape and Reel
-EV: Evaluation Board
-EVZ: Evaluation Board ROHS Compliant
-DM: Demo Board
-DMZ: Demo Board ROHS Compliant
-RF: Ref Design Eval Board
-RFZ: Ref Design Eval Board ROHS Compliant
-EC: Enhanced Commercial (Enhanced EOL, MIL-PRF-38535 Change Notice, Traceable to Wafer Lot)

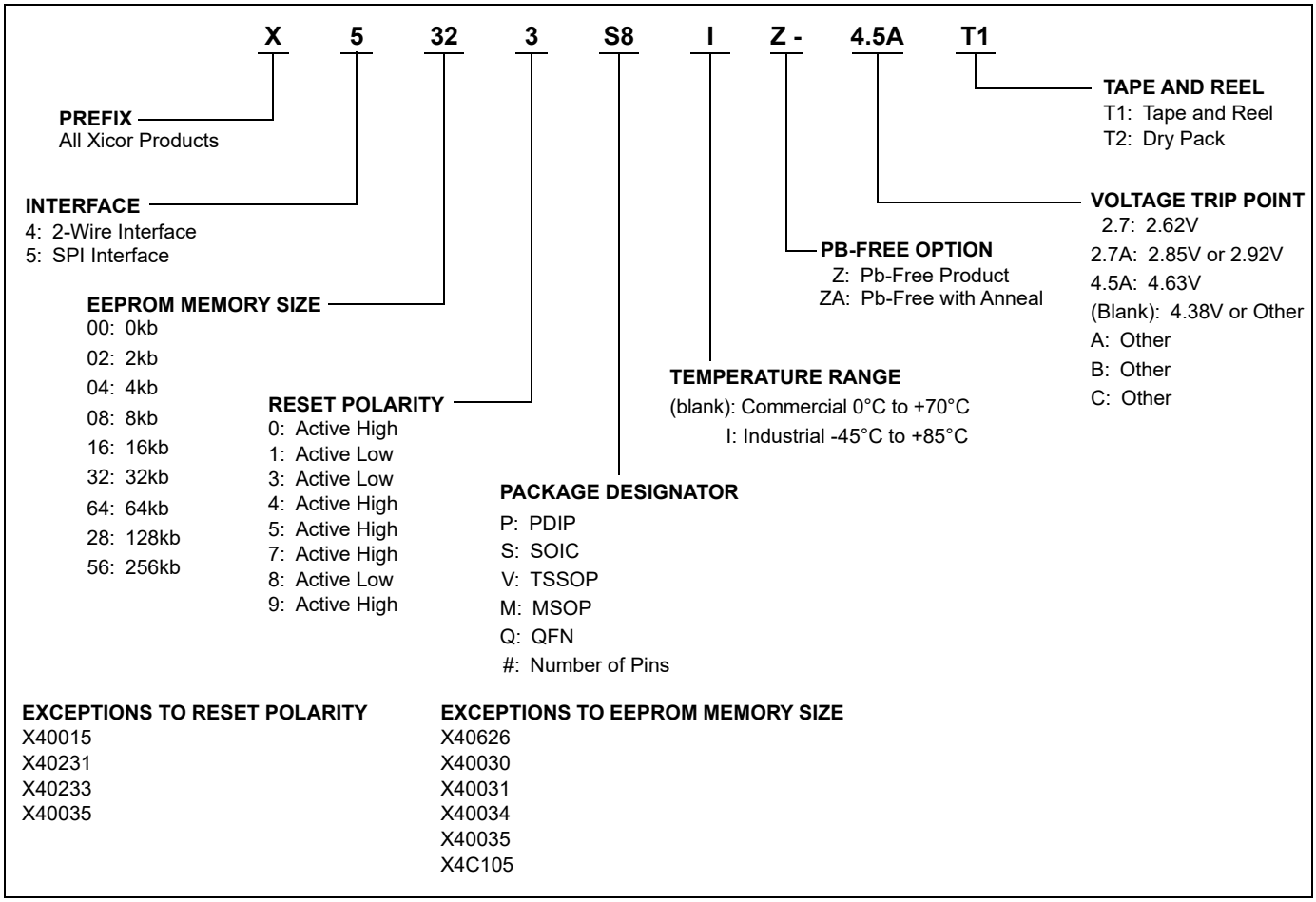
EL Types



PACKAGE TYPE	PACKAGE DESIGNATOR
Bare Die	D
CerDip	J
QFN/DFN (Saw Singulate)	L
SO (0.300”) and HSOP	M
PDIP	N
TSSOP (4.4 mm)	R
HTSSOP (4.4 mm)	RE
SO (0.150”)	S
TO-220	T
QSOP	U
SOT-23	W
MSOP	Y
HMSOP	YE
TSOT	WT
SC-70	C

X Types

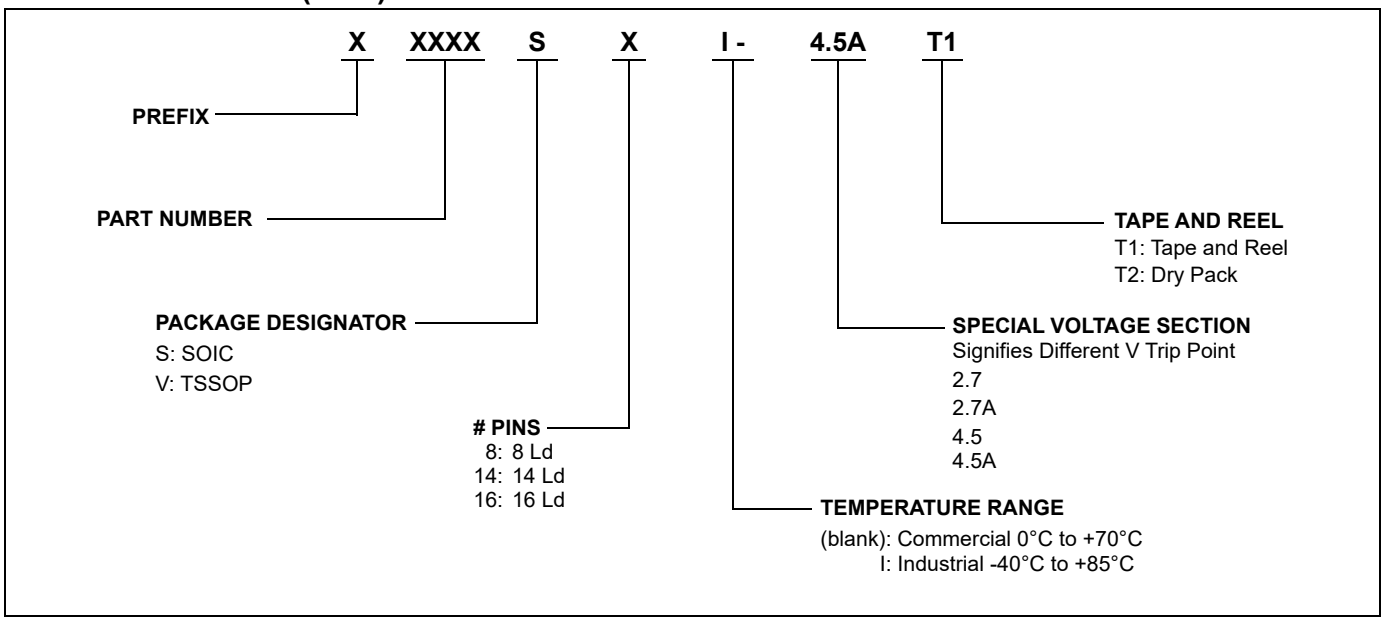
System Management Products (SMP)



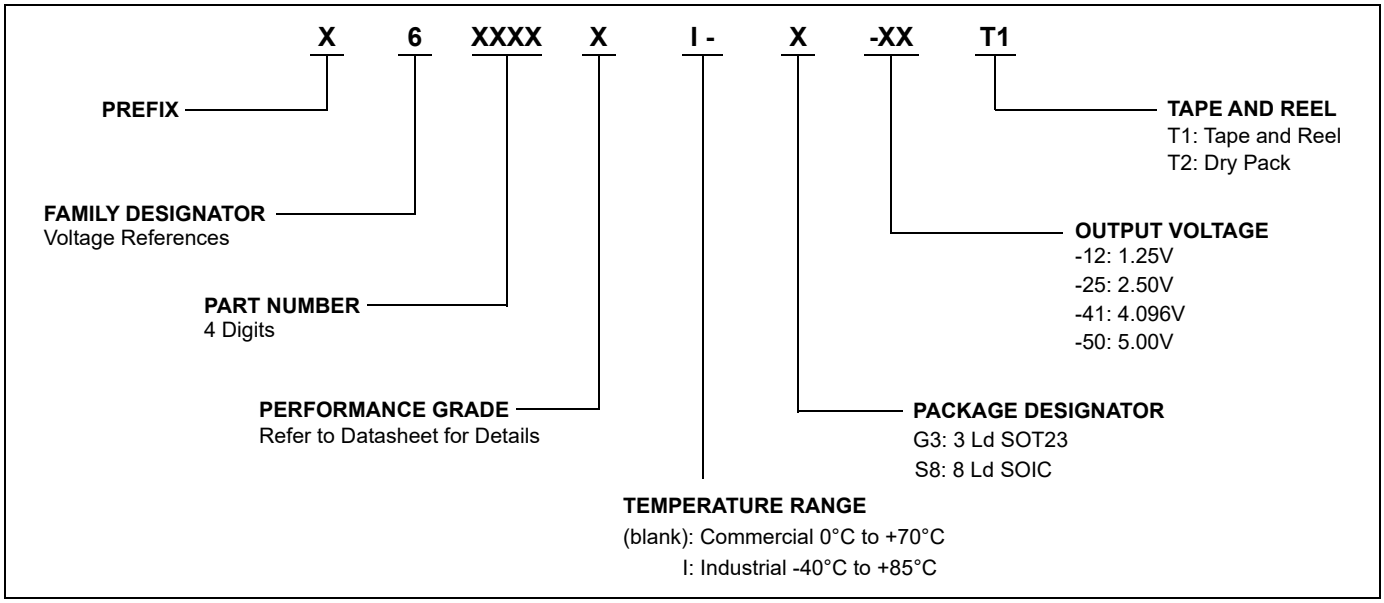
EXCEPTIONS TO RESET POLARITY
X40015
X40231
X40233
X40035

EXCEPTIONS TO EEPROM MEMORY SIZE
X40626
X40030
X40031
X40034
X40035
X4C105

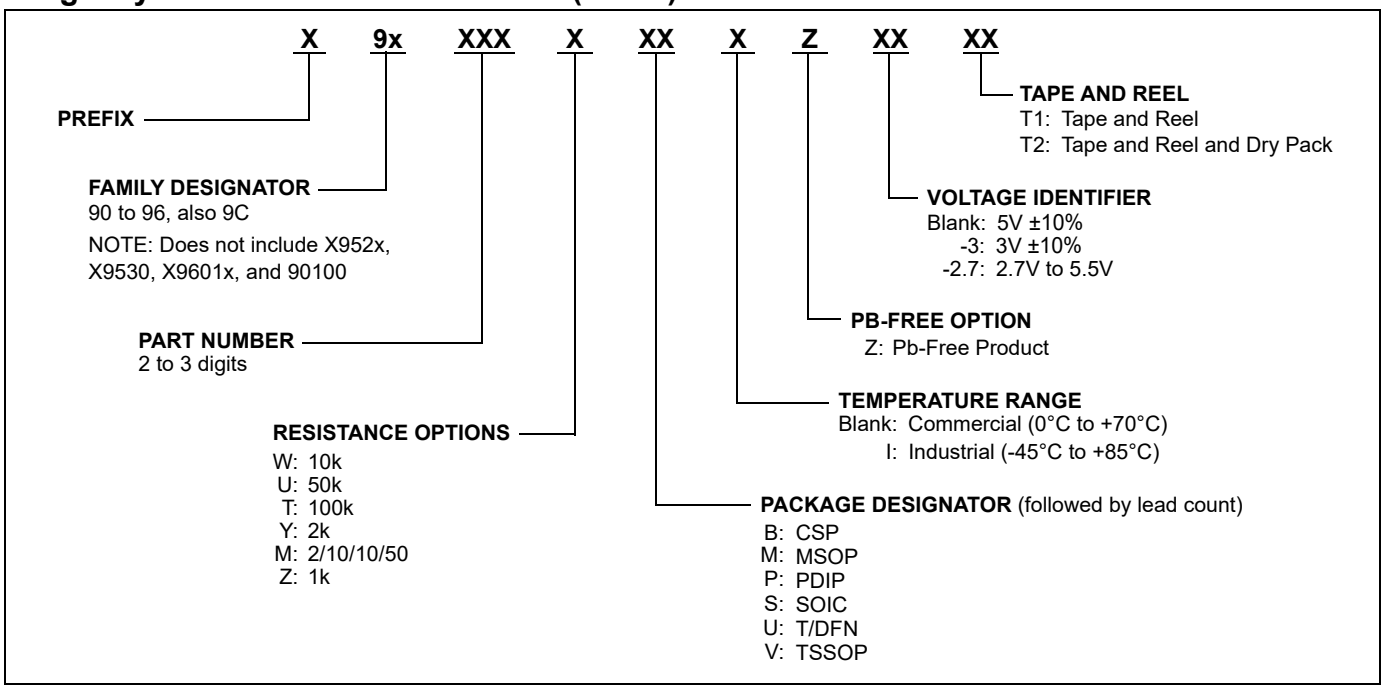
Real Time Clocks (RTC)



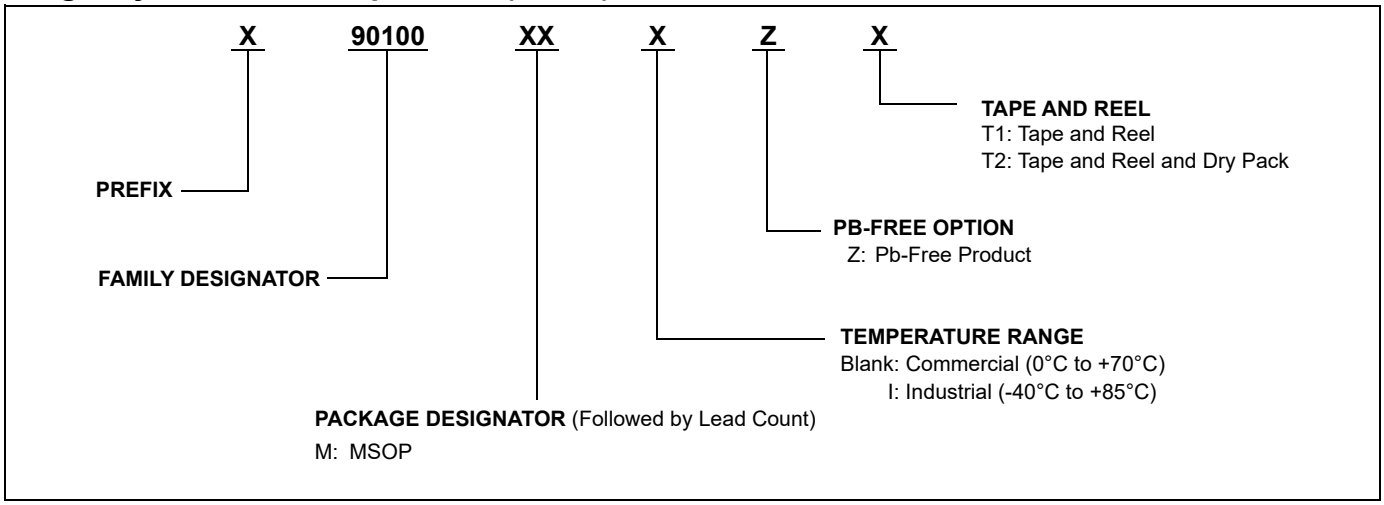
Voltage References (VREFs)



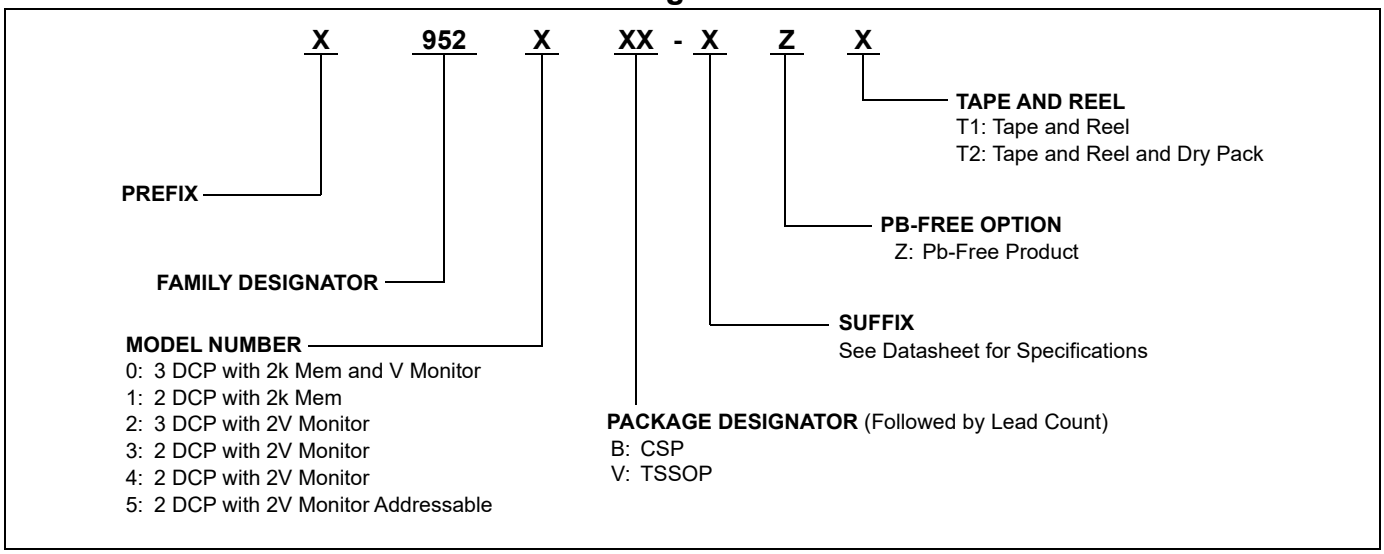
Digitally Controlled Potentiometers (DCPs)



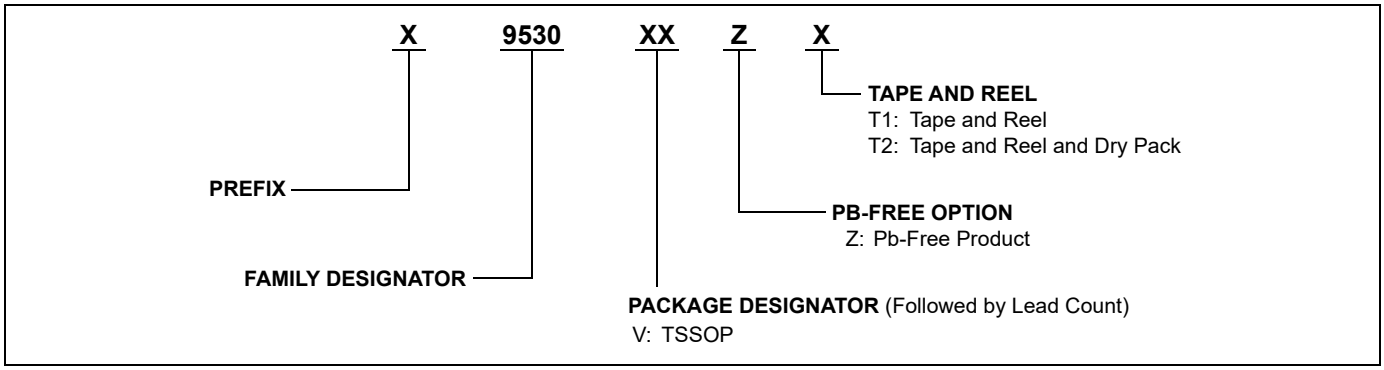
Digitally Controlled Capacitors (DCCs)



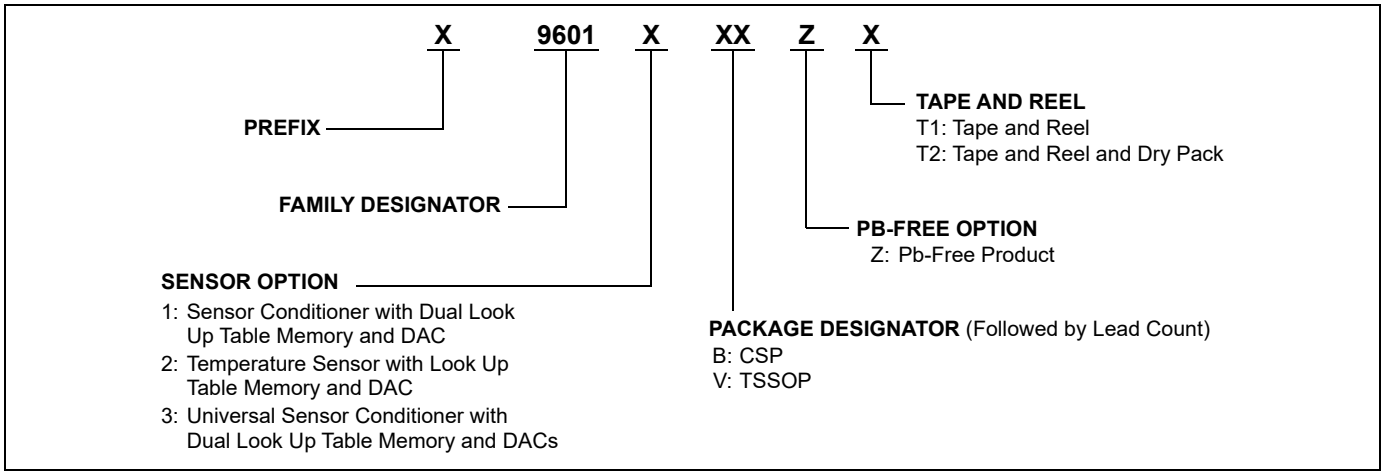
Bias and Control for Laser Diode with Integrated DCP



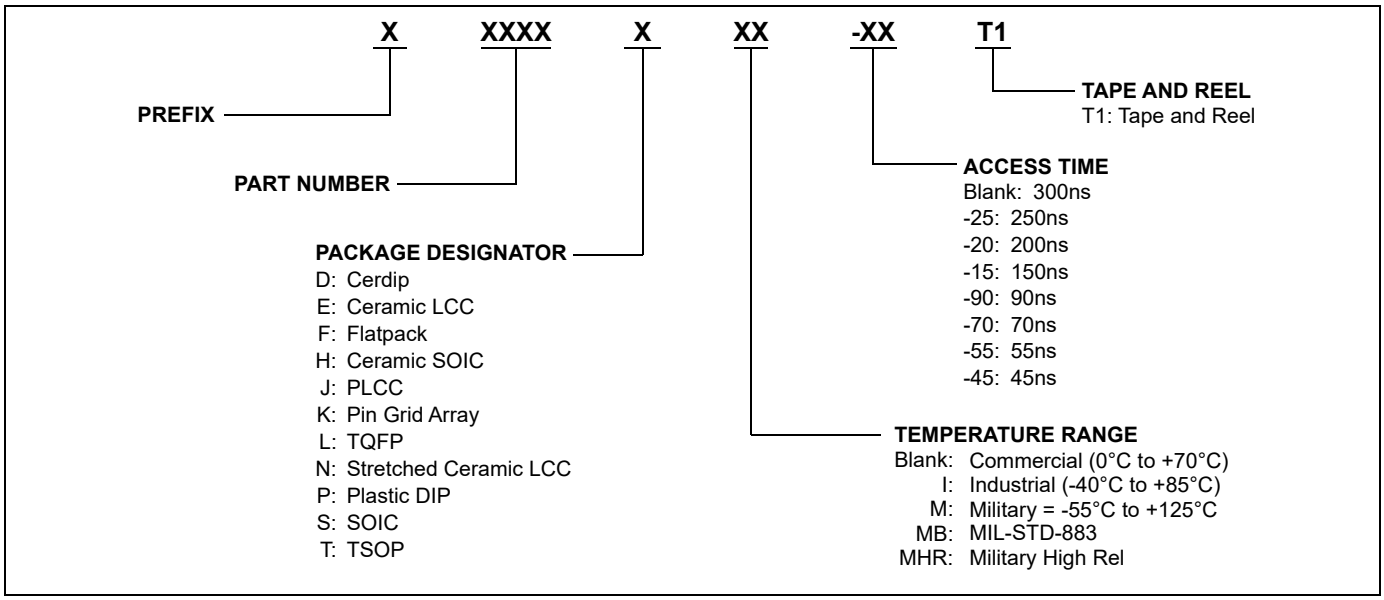
Bias and Control for Laser Diode



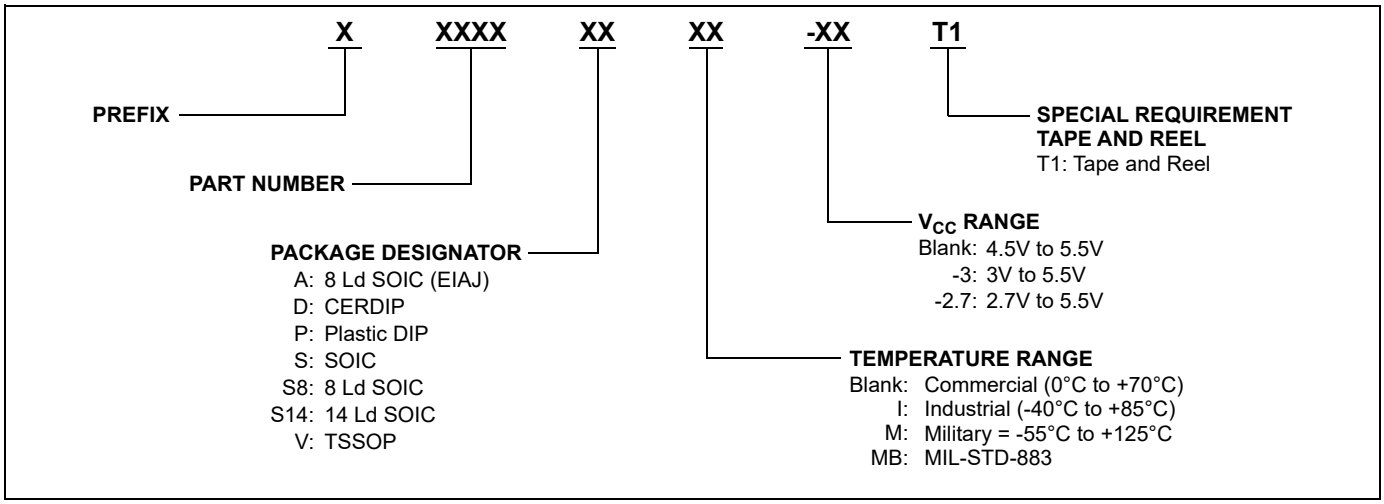
General Purpose Sensor Conditioners with Look-Up Table Memory



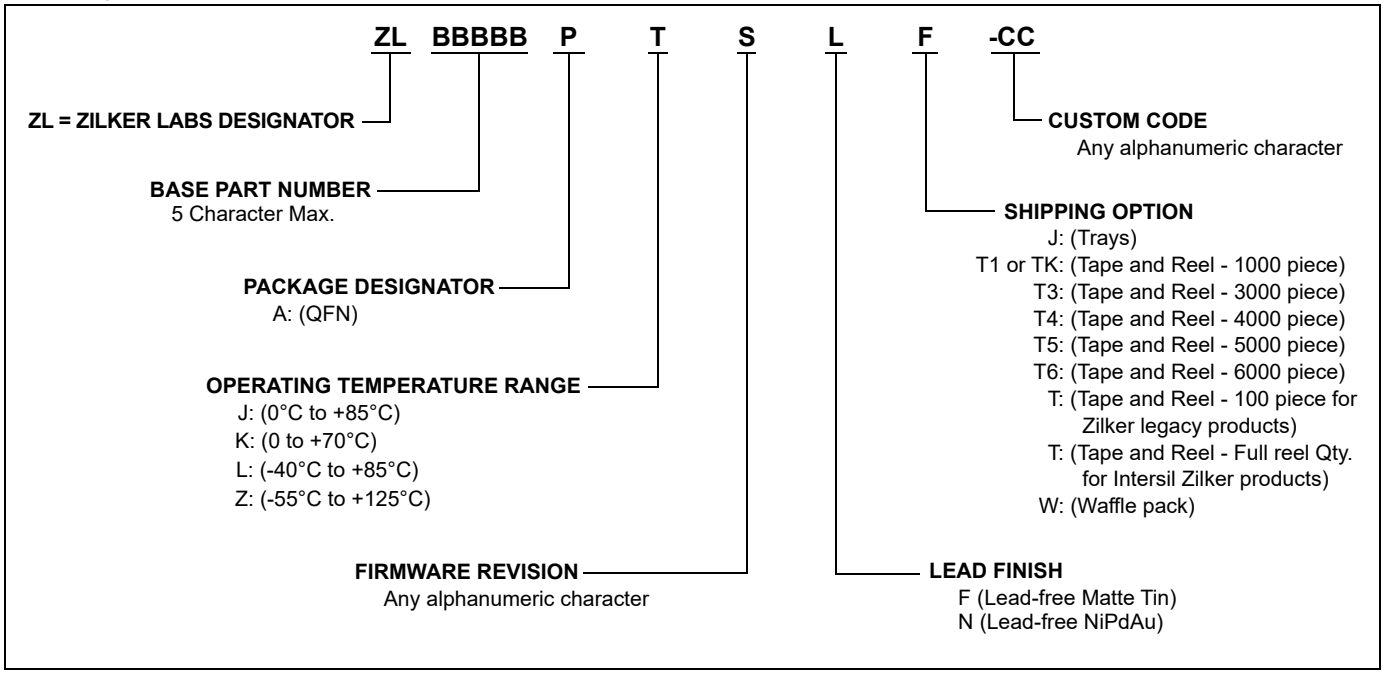
Parallel E^{2}PROM



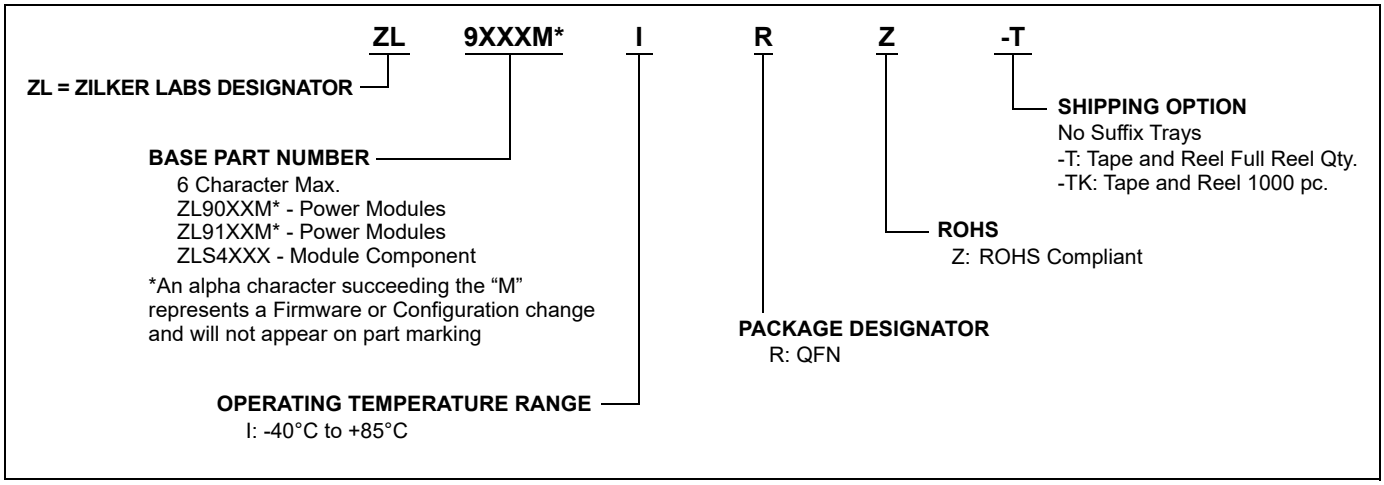
Serial E^{2}PROM



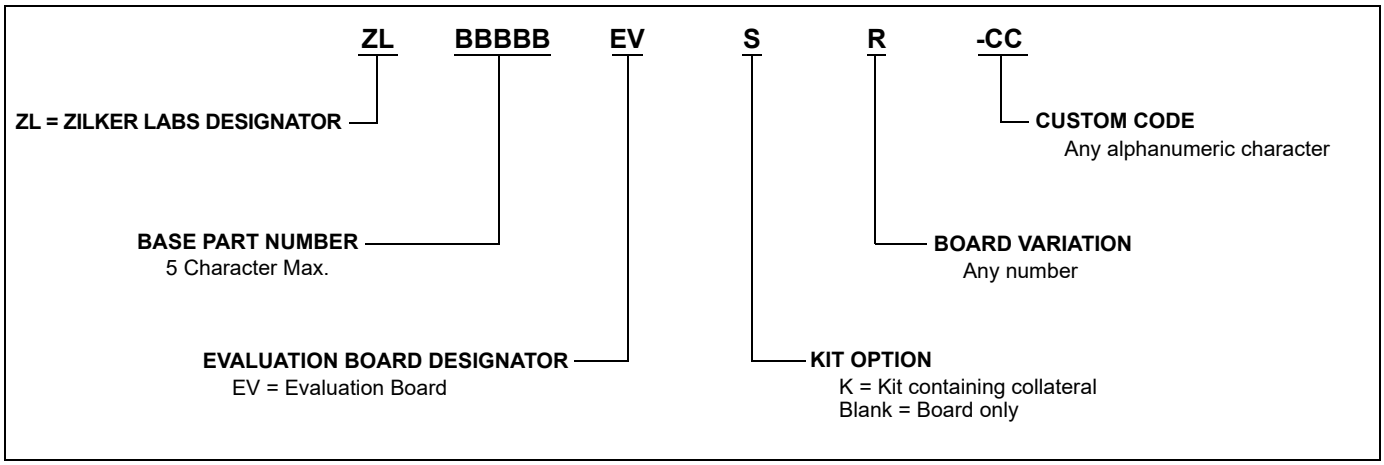
ZL Types



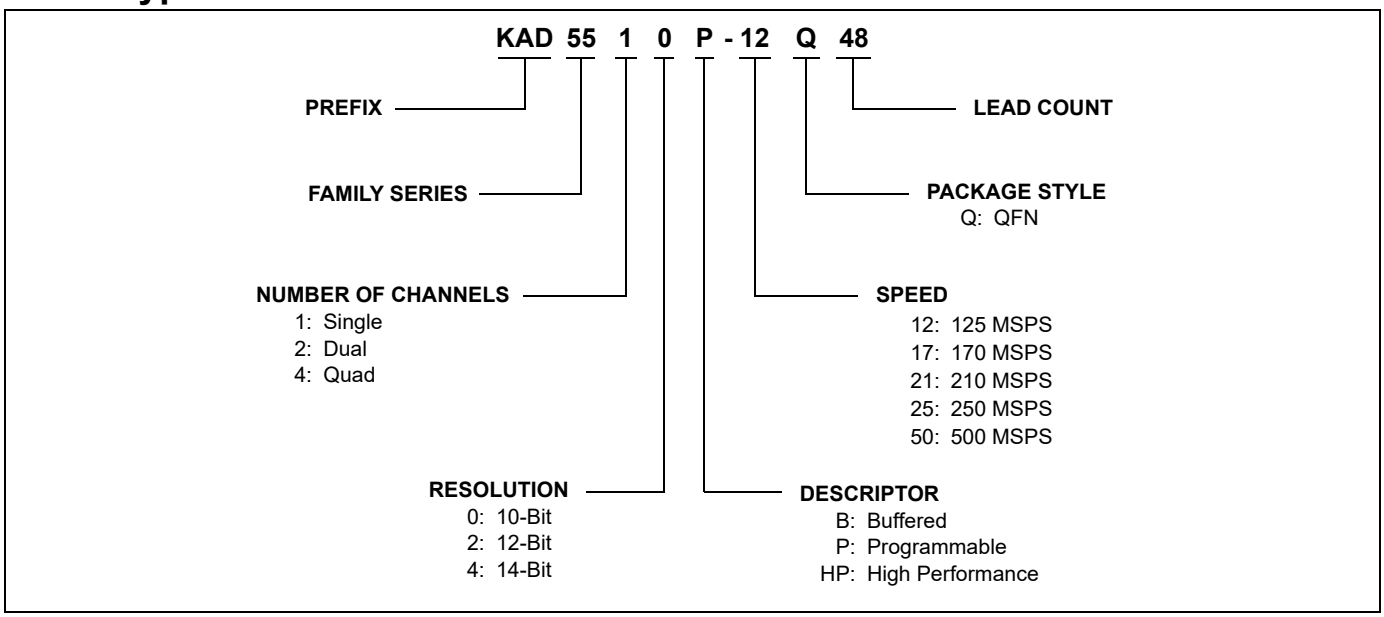
ZL Power Modules



ZL Evaluation Boards

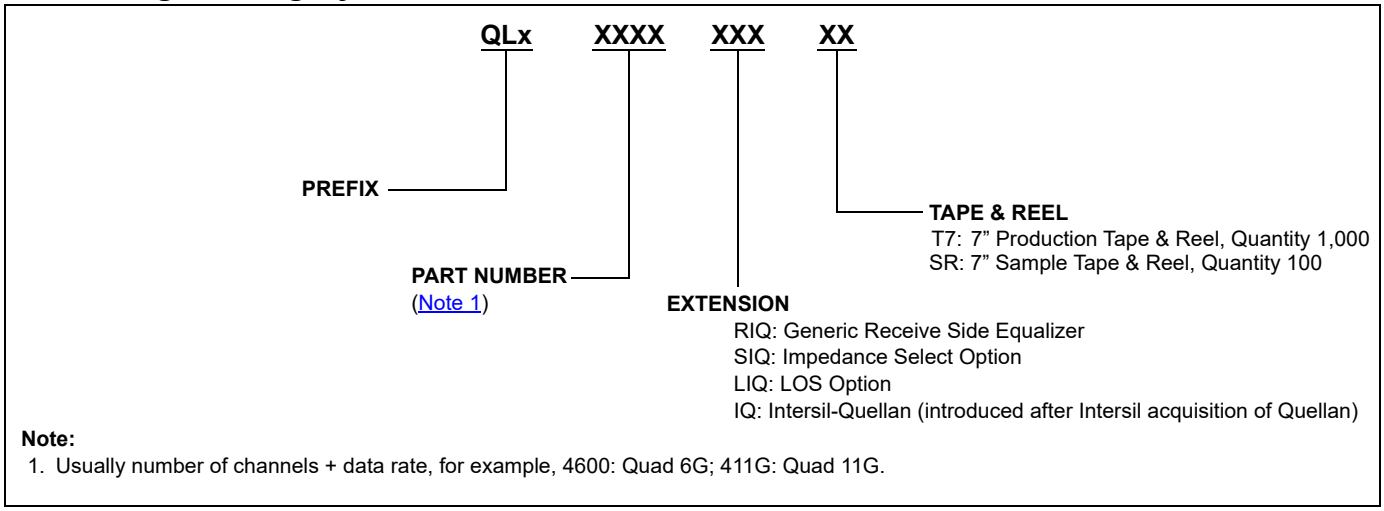


KAD Types



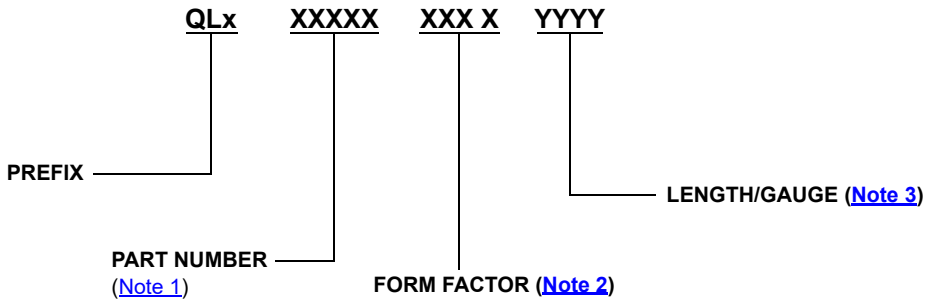
QLx Types

Wired Signal Integrity Parts



Note:
1. Usually number of channels + data rate, for example, 4600: Quad 6G; 411G: Quad 11G.

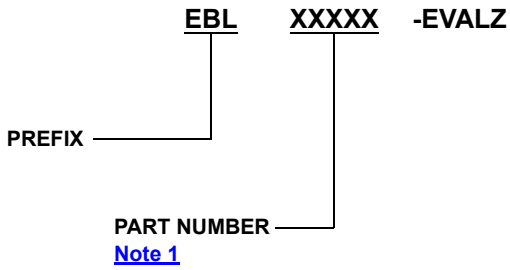
Active Cables



Notes:

1. Data Rate followed by Special Designator, followed by Customer Designator (if applicable), followed by "C" for cable.
   Special Designators:
   0: Half-active (chip on RX side only)
   1: Generic full-active (chips on both TX and RX ends)
   2: Full-active Ethernet
   Customer Designator:
   0: General market, other numbers for specific customers, for example: 600C (6G half-active cable), 4000C (40G half-active cable), 4100C (40G full-active cable)
2. For example, connector type or form-factor: SFP for SFP+, QSFP for QSFP, MSAS for Mini-SAS, SDP for mini DisplayPort, SDP for Standard DisplayPort, SMDP for mini-to-standard DisplayPort.
3. For example, 1028 = 10m 28 AWG.

QL Evaluation Boards

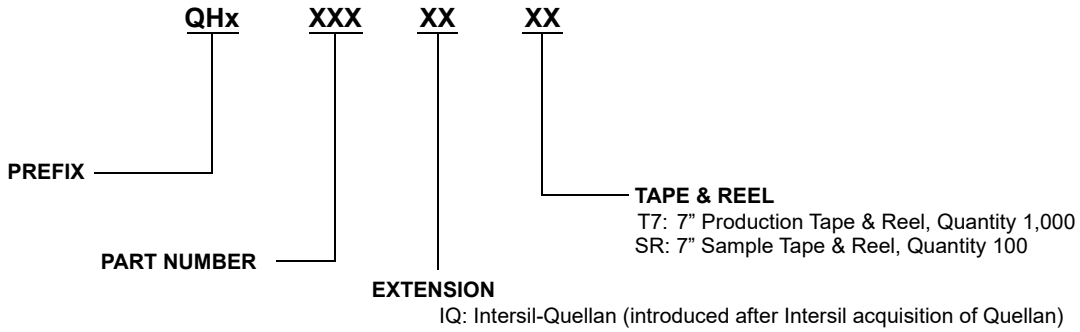


Note:

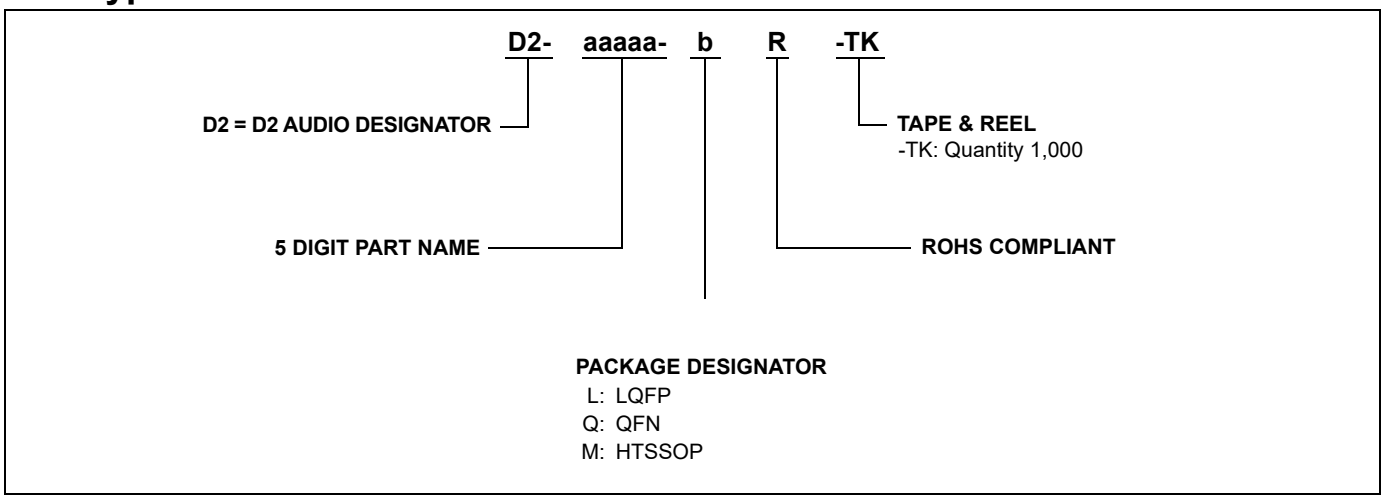
1. Same as the part marking on the respective IC.

QHx Types

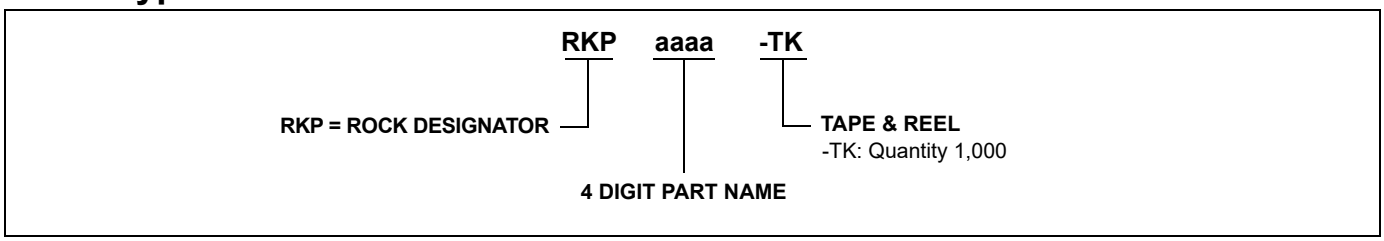
Wireless Noise Cancellation Parts



D2 Types



RKP Types



TW Types

TW aaaa bb - c d e f g# - h j k l

PREFIX

DEVICE NUMBER

AT: Auto Wafer
EP: Epi Wafer

c - PROCESS
This character is included in the marking of legacy products only.

PROCESS	CODE
TSMC, 0.35µm, Polycide, SPQM or SPTM Logic	A
TSMC, 0.25µm	B
X-FAB, 0.25µm	C
TSMC, 0.18µm	D
X-FAB, 0.18µm	E
TSMC, 0.18µm, EPI, Ar Anneal, Hi	G
Goyatek/Vanguard, 0.25µm	H
TSMC 0.25µm EPI, Ar Anneal, Hi	J
TSMC 0.18µm Automotive Process	K
TSMC 0.13µm	M
TSMC 90nm	N
Fujitsu 90nm	P
TSMC 0.13µm 12” Wafer	Q
TSMC 65nm	R
TSMC 45nm	S

d - ASSEMBLY VENDOR
This character is included in the marking of legacy products only.

ASSEMBLY VENDOR	CODE
ASEK	A
ASECL	B
GAPT	C
i2a/IPAC, Quick Pak	D
SPIL	E
ChipMOS	G
UTAC	J
Fujitsu	K
Amkor Korea	M

e -
Q: 12” Wafer

f - PACKAGE TYPE A

PACKAGE TYPE	CODE
BGA package	B
LQFP package	L
PQFP package	P
TQFP package	T
QFN package	N
PQFP package with Exposed Heat Spreader	E

g# - DIE REVISION
It starts from A1. If full layers are changed, the die revision changes like A1→B1→C1, etc.
If some layers are changed, the die revision changes like A1→A2→A3, etc.

h - PACKAGE TYPE B

PACKAGE TYPE	CODE
Green (Halogen Free) and Lead Free package	G (Note)
Normal package	N
Green (Halogen Free) and Lead Free package with Cu Bond Wires	C
Flip Chip	F

Note: The following FG’s also use Cu wire:
TW6815-LA1-GR
TW6816-LA1-GR
TW6817-LA1-GR
TW6818-LA1-GR
TW6932-LA1-GR

j - PACKAGE TYPE C

PACKAGE TYPE	CODE
Drop-in heat spreader	D
Exposed heat spreader	E
Regular package without heat spreader	R

k - PACKAGE VARIANT

PACKAGE VARIANT	CODE
This is only used when one product type is offered in 2 different sizes or lead counts of the same package style. The last FG# created will include the lead count.	128 (lead count)

l - OPTIONS
S = SLT
B = Burn-in
H = High Temp. Testing
I = Industrial
V = High Volt Testing
T = Tape & Reel Packing

5962 SMD/DLA - QML Types

5962 - XXXXX 0X X X X

SMD ID NUMBER
(Does Not Change) (ID Not Applicable in Earlier DLA Items)

TOTAL DOSE DESIGNATOR
-: Non-Rad Hard
M: 3krad(Si) L: 50krad(Si)
D: 10krad(Si) R: 100krad(Si)
P: 30krad(Si) F: 300krad(Si)

DRAWING NUMBER
(DLA and SMD)

DEVICE TYPE
(Paragraph 1.2.1 Of SMD/DLA Drawing)

DEVICE CLASS DESIGNATOR
(If Applicable)
Q: QML Class Q (MIL-PRF-38535)
M: QML Class B (MIL-STD-883)
V: QML Class V, (MIL-PRF-38535)
N: Non-Traditional Packages and Temp Ranges (i.e., Plastic Packages, -40°C to +85°C Temperature Range)
T: QML Class T, Star*Lite Flow

CASE OUTLINE
Case Outlines are Listed in the Specific SMD and Detailed in MIL-STD-1835, Section 4.

LEAD FINISH
A: Solder Dip
C: Gold

Note: Nomenclature Per MIL-PRF-38535

80C, 82CXXX Types

M D 80C86 - 2 /B Z

TEMPERATURE RANGE
C: 0°C to +70°C
I: -40°C to +85°C
M: -55°C to +125°C

PACKAGE DESIGNATOR
P: Dual-In-Line Plastic (PDIP)
D: Ceramic Dual-In-Line Frit-Seal (CERDIP)
or Ceramic Dual-In-Line Metal Seal (SBDIP)
G: Ceramic Pin Grid Array (CPGA)
R: Ceramic Leadless Chip Carrier (CLCC)
S: Plastic Leaded Chip Carrier (PLCC)
M: Small Outline Plastic (SOIC)
MS: OKI Pin for Pin Cross (PLCC)
MQ: OKI Pin for Pin Cross (MQFP)

PART NUMBER
80CXXX: CMOS Microprocessors
82CXXX: CMOS Peripherals

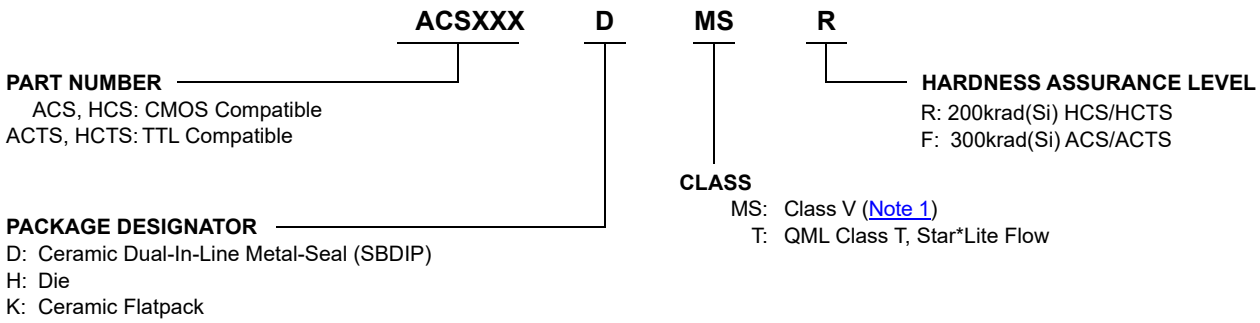
SPEED DESIGNATION

Peripherals	µProcessors
-5: 5MHz	Blank: 5MHz
Blank: 8MHz	-2: 8MHz
-10: 10MHz	-10: 10MHz
-12: 12MHz	-12: 12MHz
	-20: 20MHz
	-25: 25MHz

SUFFIX
/B: -55°C to +125°C with Burn-In
/883: Current Rev Compliant
/7: Thin EPI, Current Rev 883 Compliant

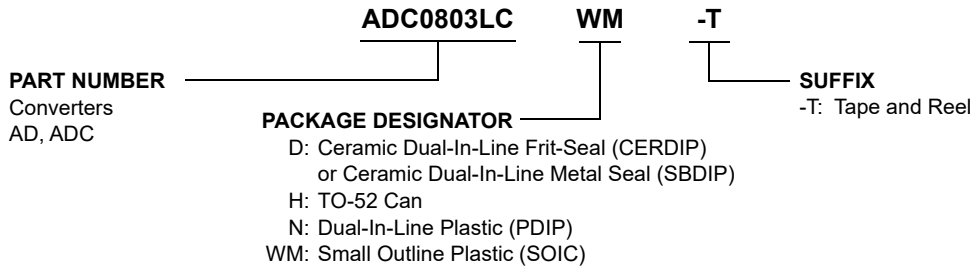
PB-FREE OPTION
Z: Pb-Free Product
ZA: Pb-Free with Anneal

ACS, ACTS, HCS, HCTS Radiation Hardened Types

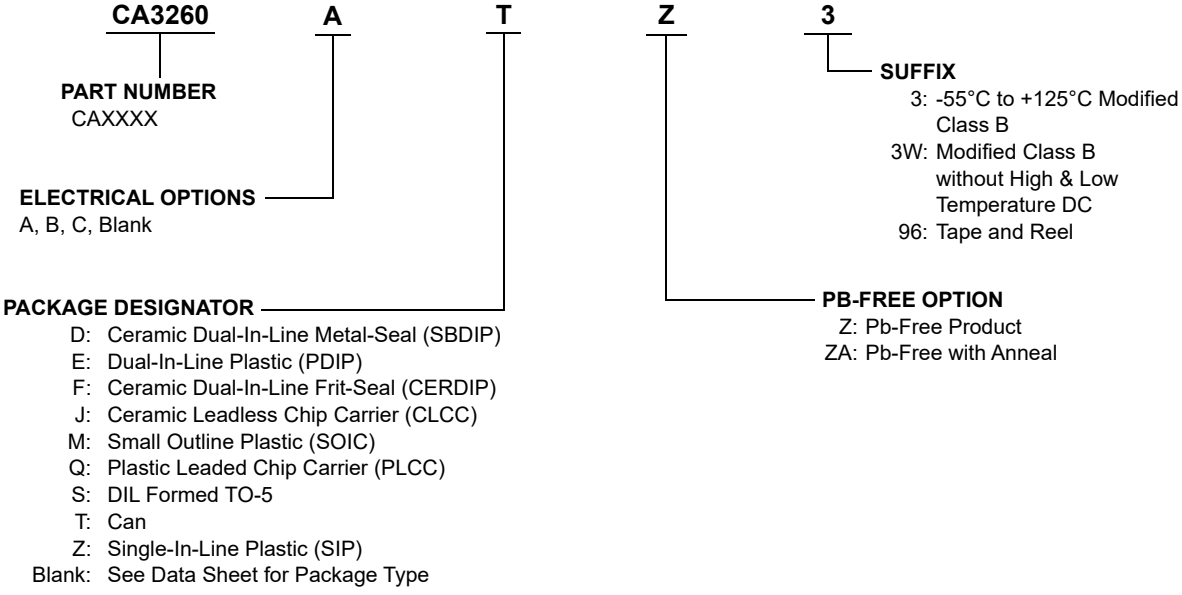


Note:
1. FLIGHT UNITS MUST BE ORDERED BY SMD#.
   A cross-reference table is available at: https://www.renesas.com/us/en/products/space-harsh-environment.html#resources

AD Types



CA Types



Note: If the part number contains three digits, add a leading zero when ordering. Example: CA555 becomes CA0555.

CD22XXX Types

CD22 — **PREFIX DESIGNATION** for Intersil Telecom ICs

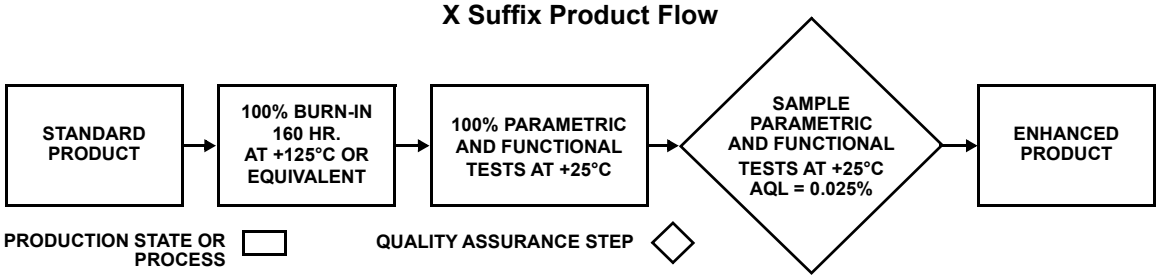
XXXXX — **PART NUMBER**

A — **REVISION**
A: 1st
B: 2nd etc.

E — **PACKAGE DESIGNATOR**
D: Ceramic Dual-In-Line Metal-Seal (SBDIP)
E: Dual-In-Line Plastic (PDIP)
F: Ceramic Dual-In-Line Frit-Seal (CERDIP)
M: Small Outline Plastic (SOIC)
Q: Plastic Leaded Chip Carrier (PLCC)
H: Chip

X — **SCREENING OPTION**
X: Enhanced Product Screening i.e., Burn-In (Optional for D, E Package Types)

X Suffix Product Flow



CD4000 Radiation Hardened Types

CD4000 — **PART NUMBER** CD4000

B — **SERIES**
B: Buffered
UB: Un-Buffered

D — **PACKAGE DESIGNATOR**
D: Ceramic Dual-In-Line Metal-Seal (SBDIP)
H: Die
K: Ceramic Flatpack

MS — **CLASS**
MS: Class V (Note 1)
NS: Class V with Neutron Irradiation (Note 1)
T: Class T, Star*Lite Flow

R — **HARDNESS ASSURANCE LEVEL**
R: 100krad(Si)

Note:
1. FLIGHT UNITS MUST BE ORDERED BY SMD#.
   A cross-reference table is available at: https://www.renesas.com/us/en/products/space-harsh-environment.html#resources

CDP Types

CDP1802 — **PART NUMBER** (CMOS LSI) CDP18XX

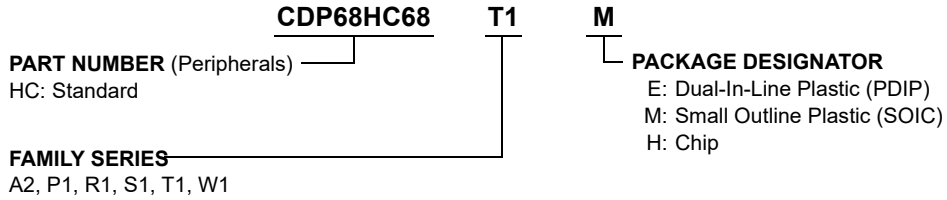
A — **REVISION**
A: 1st
B: 2nd

C — **VOLTAGE**
C: 5V Device

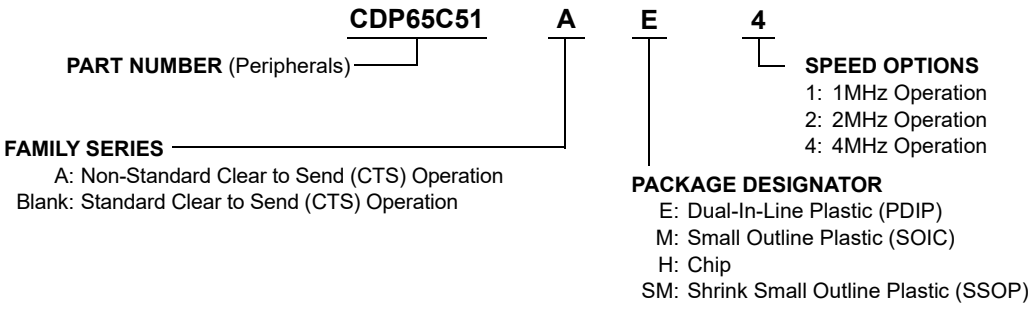
D — **PACKAGE DESIGNATOR**
D: Ceramic Dual-In-Line Metal-Seal (SBDIP)
E: Dual-In-Line Plastic (PDIP)
K: Ceramic Flatpack
Q or N: Plastic Leaded Chip Carrier (PLCC)

3 — **PRODUCT ASSURANCE LEVEL**
X: -40°C to +85°C with Burn-In
3: Non-Compliant with MIL-STD-883

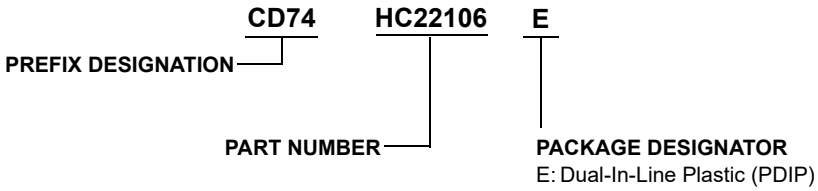
CDP68HC68 Types



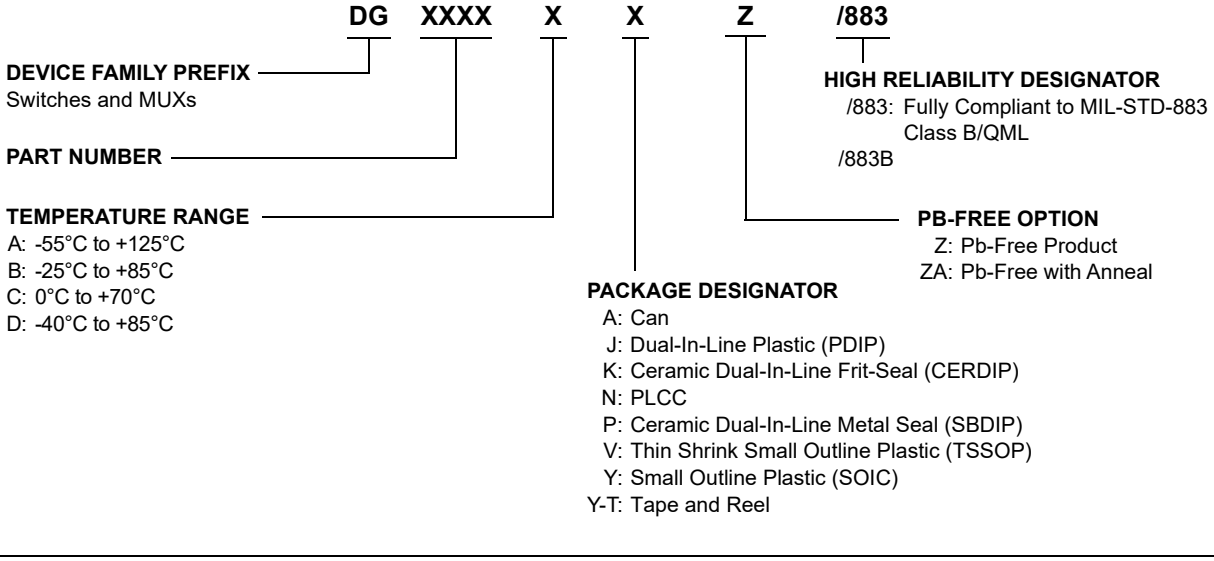
CDP65C51 Types



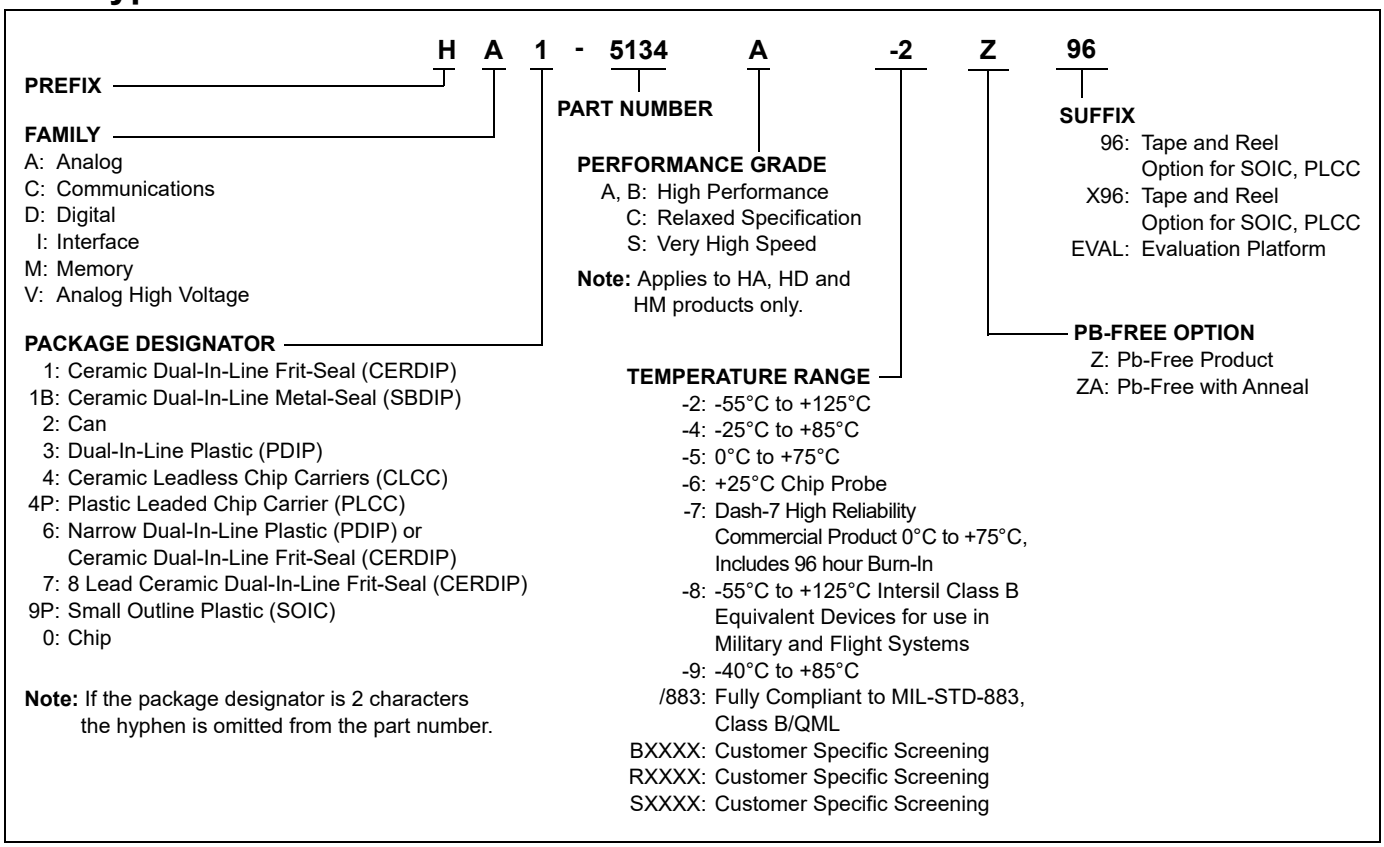
CD74HC Types



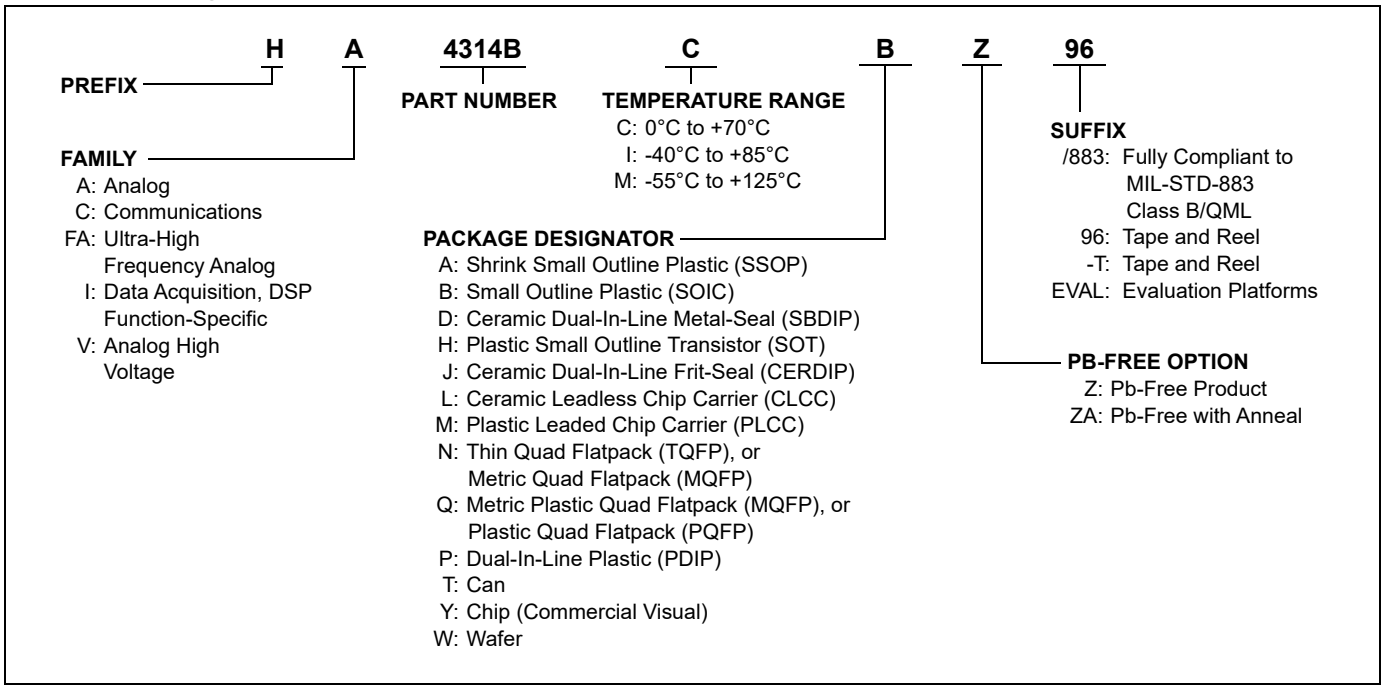
DG Types



HX Types



HX, HXX Types



HCS, HCTS, ACS, ACTS, Radiation Hardened Types

HCSXXX D MS R

PART NUMBER
ACS, HCS: CMOS Compatible
ACTS, HCTS: TTL Compatible

PACKAGE DESIGNATOR
D: Ceramic Dual-In-Line Metal-Seal (SBDIP)
H: Die
K: Ceramic Flatpack

CLASS
MS: Class V (Note 1)
T: Class T, Star*Lite Flow

HARDNESS ASSURANCE LEVEL
R: 200krad(Si) HCS/HCTS
F: 300krad(Si) ACS/ACTS

Note:
1. FLIGHT UNITS MUST BE ORDERED BY SMD#.
A Cross Reference table is Available at:
https://www.renesas.com/us/en/products/space-harsh-environment.html#resources

HIN Types

HIN XXX X X X Z - T

DEVICE FAMILY PREFIX
Interface

PART NUMBER

A: High Speed
E: 15kV ESD Protected

TEMPERATURE RANGE
C: Commercial (0°C to +70°C)
I: Industrial (-40°C to +85°C)

PACKAGE DESIGNATOR
A: Shrink Small Outline (SSOP)
B: 300 mil Small Outline Plastic (SOIC)
BN: 150 mil Small Outline Plastic (SOIC)
P: Dual-In-Line Plastic (PDIP)
Y: Die
J: Dual-in-Line Ceramic (CDIP)
N: Metric Quad Flat Package (MQFP)

PB-FREE OPTION
Z: Pb-Free Product
ZA: Pb-Free with Anneal

TAPE AND REEL

HIP Types

H I P 4082 I B * Z T

PREFIX

FAMILY
IP: Intelligent Power
V: High Voltage

FUNCTION CODE
00XX: Low Side Switches
10XX-XX: 00 to 29 Hot Plug
-XX: 30 to 99 High Side Switches
206X: Integrated MOSFETs
21XX-XX: 00 to 19 Half Bridges
40XX: Full or Three Phase Bridges
50XX: Integrated Controllers
60XX: PWM Controllers
62XX: ICs for Portable Applications
63XX: Multiphase Buck PWM Controllers
65XX: ACPI Controllers
66XX: Synchronous-Rectified Buck MOSFET Drivers
72XX: Automotive Communication (J1850)
9XXX: Special Function
(X: Sequential numbers assigned by design)

Note: Suffix EVAL: Evaluation Kit (Available for some products).

TEMPERATURE RANGE
A: Automotive (-40°C to +105°C)
C: Commercial (0°C to +70°C)
I: Industrial (-40°C to +85°C)
M: Military (-55°C to +125°C)
D: EDP (0°C to +85°C)
F: Full-Range Industrial (-40°C to +125°C)

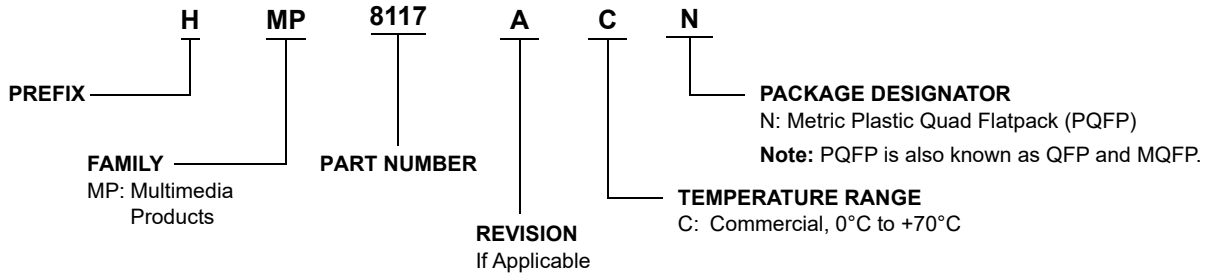
PACKAGE DESIGNATOR
B: Small Outline Plastic (SOIC)
D: Chip
K: SOT-23
M: Plastic Leaded Chip Carrier (PLCC)
P: Dual-In-Line Plastic (PDIP)
Q: Metric Plastic Quad Flatpack (MQFP)
S: Single-In-Line Plastic (SIP)
V: TSSOP
W: Wafer
Y: Die
RT: Thin Quad/Dual Flat No Lead (TQFN/TDFN

SPECIAL SELECTIONS
Optional characters to denote operating conditions, voltage selections defined in datasheet

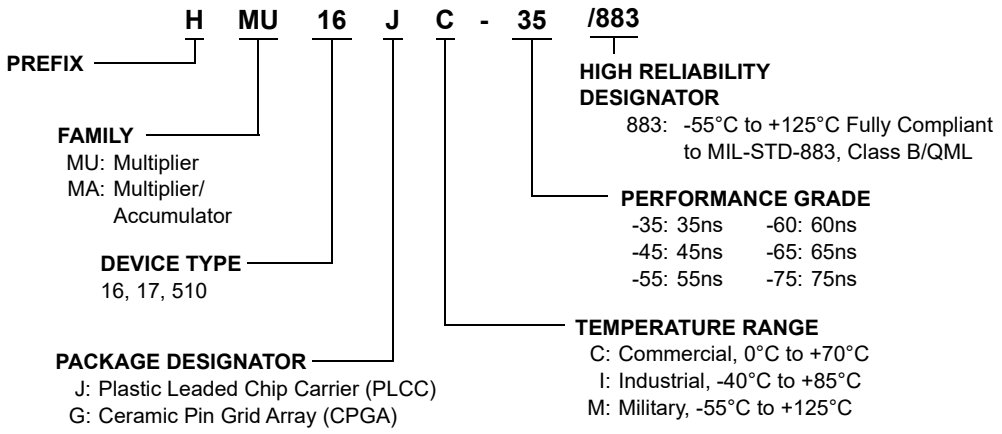
PB-FREE OPTION
Z: Pb-Free Product

PACKING DESIGNATOR
T: Tape and Reel (If Available)
(See Note)

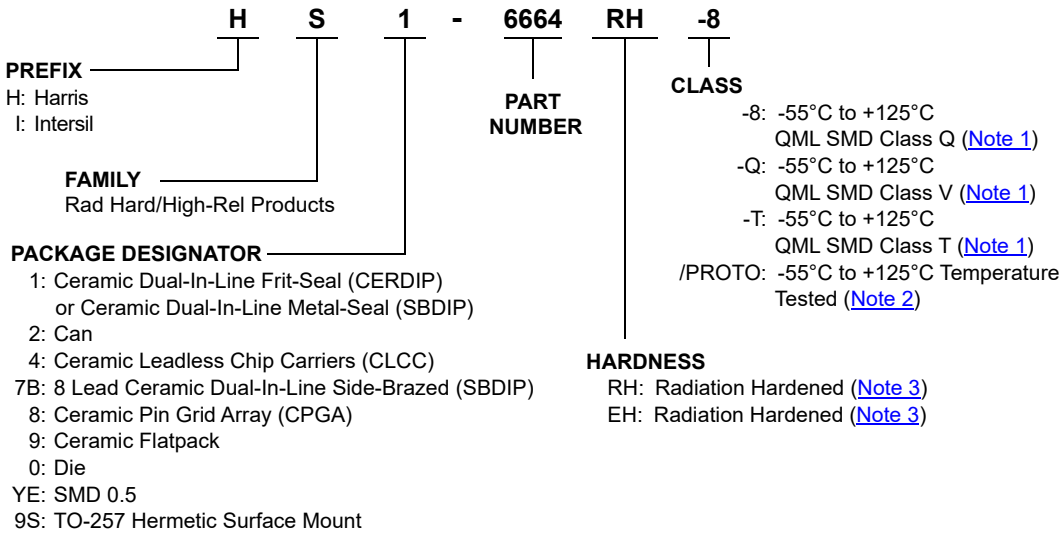
HMP Types



HMU/HMA Types



HS/IS Radiation Hardened Types



Notes:

1. >>FLIGHT UNITS MUST BE ORDERED BY SMD#.
   A cross reference table is available https://www.renesas.com/us/en/products/space-harsh-environment.html#resources
2. /PROTO available for design-in/breadboarding - NOT FOR FLIGHT.
3. See specific device type SMD for radiation hardness level.

HSP Types

H SP XXXXX A J C - XX /883

PREFIX

FAMILY
SP: Signal Processing,
DSP Function-Specific

DEVICE TYPE
43XXX: Digital Filters
45XXX: Signal Synthesis/Special Function
48XXX: Image Processing
95XX: Building Blocks
50XXX: Freq. Conversion and Modulation/
Demodulation

MASK REVISION

PACKAGE DESIGNATOR
D: Die
G: Ceramic Pin Grid Array (CPGA)
J: Plastic Leaded Chip Carrier (PLCC)
P: Dual-In-Line Plastic (PDIP)
S: Small Outline Plastic (SOIC)
V: Metric Quad Flatpack (MQFP)
W: Wafer

TEMPERATURE RANGE
C: Commercial, 0°C to +70°C
I: Industrial, -40°C to +85°C
M: Military, -55°C to +125°C

SPEED GRADE IN MHz

HIGH-RELIABILITY DESIGNATOR
/883: -55°C to +125°C Fully Compliant to MIL-STD-883, Class B/QML

Note: Suffix EV, EVAL: Evaluation Kit (Available for some products).

ICL, ICM Types

ICL 8069D C B A Z T

DEVICE FAMILY
ICL
ICM

PART NUMBER

TEMPERATURE RANGE
C: Commercial, 0°C to +70°C
I: Industrial, -25°C to +85°C or -40°C to +85°C
(Specified on Data Sheet)
M: Military, -55°C to +125°C

PACKAGE DESIGNATOR
B: Small Outline Plastic (SOIC)
D: Ceramic Dual-In-Line Metal-Seal (SBDIP)
F: Ceramic Flatpack
H: Small Outline Transistor Plastic (SOT)
J: Ceramic Dual-In-Line Frit-Seal (CERDIP)
M: Metric Plastic Quad Flatpack (MQFP)
P: Plastic Dual-In-Line
S: TO-52 Can
T: Can (TO-99, TO-100)
Z: TO-92 (Plastic)
/W: Wafer
/D: Chip

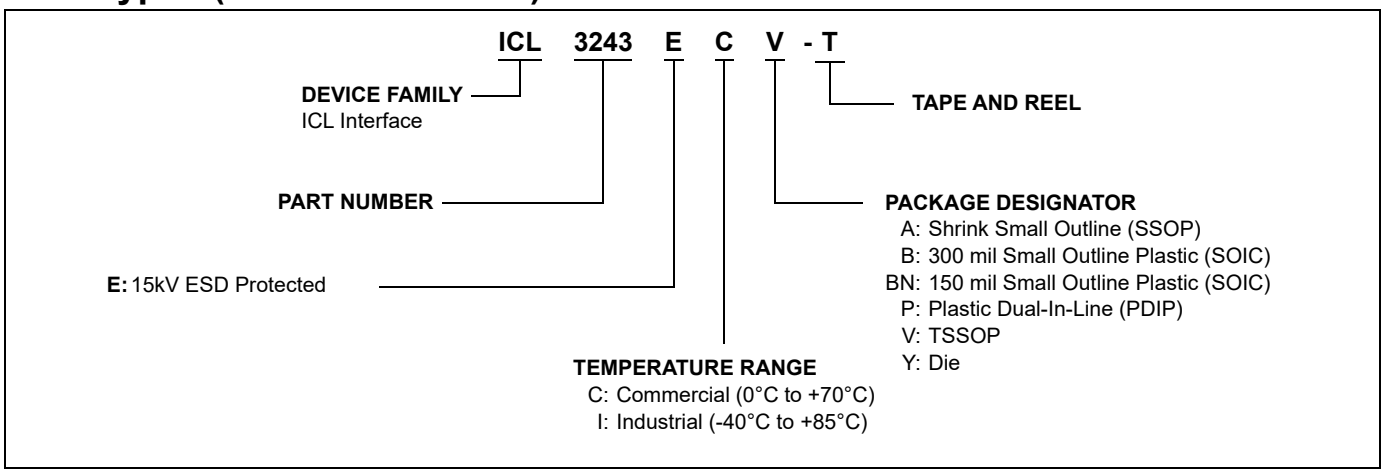
PIN COUNT DESIGNATOR

SUFFIX	PIN COUNT	DIAMETER
A	8	
B	10	
C	12	
D	14	
E	16	
F	22	
G	24	
H	42	
I	28	
J	32	
K	35	
L	40	
N	18	
P	20	
Q	2	
R	3	
V	8	0.200″ Pin Circle, Isolated Case
W	10	0.230″ Pin Circle, Isolated Case
X	10	0.230″ Pin Circle, Case to Pin 5
Y	8	0.200″ Pin Circle, Case to Pin 4
Z	8	0.230″ Pin Circle, Case to Pin 5
44	44	

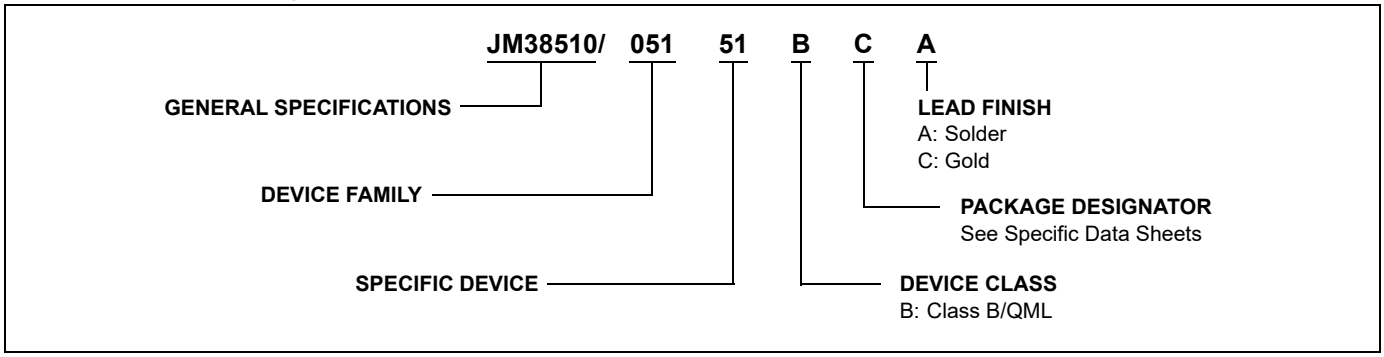
SUFFIX
/883B: Fully Compliant to MIL-STD-883 Class B/QML
T: Tape and Reel

PB-FREE OPTION
Z: Pb-Free Product
ZA: Pb-Free with Anneal

ICL Types (Interface Circuits)



JM JAN-QML Types



IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.