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1. Register Descriptions

The register descriptions section describes the behavior and function of the customer-programmable volatile-memory registers in the 5x1503 (5X1503/5L1503) clock generator. For information on product operation, see the *5X1503 Datasheet*.

2. MicroClock Clock Generator Register Set

The 5X1503/5L1503 contains volatile (RAM) 8-bit registers and non-volatile 8-bit registers (see Figure 1). The non-volatile registers are One-Time Programmable (OTP), and pre-programmed at the factory with a custom dash-code configuration.

The device operates according to settings in the RAM registers. The device contains two complete configurations. At power-up, a pre-programmed configuration is transferred from OTP to the RAM registers. The device behavior can then be modified by reprogramming the RAM registers through I2C.

The device can start up in “I2C mode” or in “Dynamic Frequency Control mode” (DFC), depending upon the status of the SEL_DFC pin 2 at power-up (see also the datasheet). I2C access is only possible when the device has started up in I2C mode. Pre-programming settings determine which of the four DFC configurations is loaded into the RAM registers at power-up in I2C mode. Using I2C commands, the configuration can be changed and there are also commands to reload a DFC configuration.

Table 1. 5X1503/5L1503 Family of Products

Product	Description	Package
5X1503	1.8V integrated with an internal 52MHz crystal (standard 5X1503).	10-DFN
5L1503	1.8V using an external crystal (standard 5L1503).	10-DFN
5X1503L	1.8V integrated with an internal 52MHz crystal, low output swing at channel 1.	10-DFN
5L1503L	1.8V using an external crystal, low output swing at channel 1.	10-DFN
5X1503S	1.8V integrated with an internal 52MHz crystal. (support spread spectrum clock).	10-DFN
5L1503S	1.8V using an external crystal. (support Spread spectrum clock).	10-DFN

3. Limit of VCO for Each MicroClock Device

- For standard 5X1503 / standard 5L1503:
  FVCO: 50MHz – 130MHz
- For 5X1503L / 5L1503L:
  FVCO: 50MHz – 130MHz
- For 5X1503S / 5L1503S:
  FVCO: 500MHz – 1100MHz

4. User Configuration Table Selection on PLL

Dynamic Frequency Control (DFC) mode is to use either four different fractional feedback divider values, or two complete configurations with two different fractional feedback divider values which are used to control VCO frequency applying only to PLL.

At power-up, the voltage at SEL_DFC (pin 2) is latched and used to select the function on SEL_DFC/SDA/DFC0 (pin 2) and SCL/OE3/DFC1 (pin 1) pins on the device (see (Table 2_Table_1:_).

When a pull-down resistor (0Ω-10KΩ) is placed on SEL_DFC (pin 2), the SEL_DFC/SDA/DFC0 and SCL/OE3/DFC1 pins are configured to be hardware selection as DFC inputs, DFC0 and DFC1. Connecting DFC0 and DFC1 to VDD33 and/or GND selects one of four DFC configuration sets, DFC 0 through DFC 3, which is then loaded into the volatile configuration registers to configure the clock synthesizer frequencies. The DFC 0 through DFC 3 configurations are preprogrammed at the factory according to customer specifications and assigned a specific dash code as part number.

When a pull-up resistor (1.8KΩ-10KΩ) is placed on SEL_DFC (pin 2), the pins SEL_DFC/SDA/DFC0 and SCL/OE3/DFC1 are configured as an I^2C interface's SDA and SCL slave bus. DFC configuration 0 is loaded into the volatile configuration registers by default to configure the clock synthesizer. The host system can use the I^2C bus to update the volatile RAM registers to change the configurations and to read status registers.

The pull-up resistor on SEL_DFC will become the pull-up resistor for the SDATA line of the I^2C interface. 10KΩ is commonly used when the 5x1503 is the only device on the bus, and smaller values may be needed when the I^2C interface is shared with multiple devices.

Table 2. Power-Up Setting of Hardware Select Pin vs. I2C Mode, and Default OTP Configuration Register

SEL_DFC Strap at Power Up	DFC1/SCL pin	DFC0/SDA pin	Function
Pull-Down	0	0	DFC 0 used to initialize RAM configuration registers.
	0	1	DFC 1 used to initialize RAM configuration registers.
	1	0	DFC 2 used to initialize RAM configuration registers.
	1	1	DFC 3 used to initialize RAM configuration registers.
1.8KΩ-10kΩ Pull-Up	SCL	SDA	I2C bus enabled to access registers. DFC 0 used to initialize RAM configuration registers.

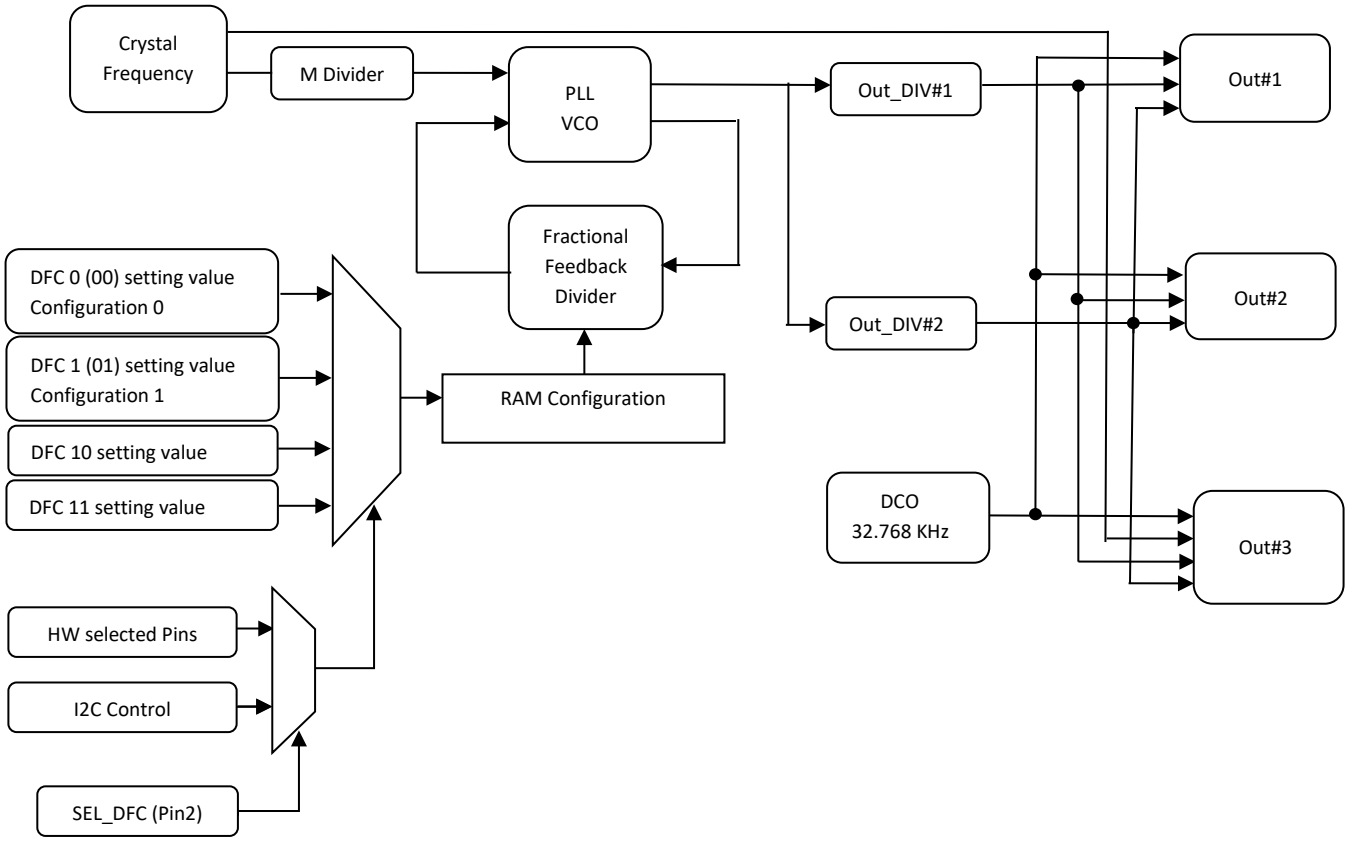


Figure 1. DFC Block Diagram on PLL

5. I2C Interface and Register Access

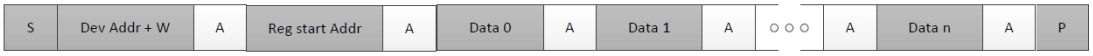
When powered up in I^2C mode, the device allows access to internal RAM registers. The default device address is 0xD0 for 8 bits or 0x68 for 7 bits. The device can be pre-programmed for addresses in the range 0xD0-D2-D4-D6 for 8 bits, or 0x68-69-6A-6B for 7 bits. The device acts as a slave device on the I2C bus using one of the four I2C addresses to allow multiple devices to be used in the system. The interface accepts byte-oriented block write and block read operations. Two address bytes specify the register address of the byte position of the first register to write or read. Data bytes (registers) are accessed in sequential order from the lowest to the highest byte (most significant bit first). Read and write block transfers can be stopped after any complete byte transfer. During a write operation, data will not be moved into the registers until the STOP signal is received, at which point, all data received in the block write will be written simultaneously in the registers.

For full electrical I^2C compliance, it is recommended to use external pull-up resistors for SDA (Serial Data) and SCL (Serial Clock). There are no internal pull-up or pull-down resistors.

Current Read

Sequential Read

Sequential Write



from master to slave

from slave to master

S = start
Sr = repeated start
A = acknowledge
Abar= none acknowledge
P = stop

Table 3. DFC Register Map Summary [1]

Register Address	Function Explanation
0x00	Configuration selection / I2C settings
0x01	Xtal divider / Dash Code ID
0x02	Crystal Oscillator / PPS mode settings
0x03	OPT protection / PPS mode settings
0x04	PLL and integer feedback divider settings
0x05	Integer feedback divider setting
0x06	Fractional feedback divider setting
0x07	
0x08	Spread-spectrum setting
0x09	
0x0A	
0x0B	Reference divider setting
0x0C	PLL loop filter R setting
0x0D	PLL charge pump control
0x0E	Output Dividers 1 setting
0x0F	Output Dividers 2 setting
0x10	OE#1 and OE#2 function selection
0x11	OUT#1, OUT#2, and OUT#3 clock selection
0x12	PLL and PPS timer control
0x13	Output control setting
0x14	OUT#1 and DIV4 control

1. See Table 4 for details at the bit level.

Table 4. RAM Register Map

Register Address		Register Bit	Default	Function explanation
Decimal	Hex			
00	0x00	7	0	OTP in Device preprogrammed? 0 = Non-Programmed, 1 = Programmed.
		6	0	Device TRIM bits preprogrammed? 0 = No , 1 = Yes
		[5..4]	00	I^2C Device address: 00=0xD0 / 0x68, 01 = 0xD2 / 0x69, 10 = 0xD4 / 0x6A, 11 = 0xD6 / 0x6B (1)
		3	0	OTP protection: 0 = Read/Write enabled , 1 = Write Blocked (2)
		2	0	OTP complete configuration selection: 0 = configuration 0 (Default), 1 = configuration 1
		[1..0]	00	DFC selection: 00 = DFC#0 (Default) 01 = DFC#1 10 = DFC#2 11 = DFC#3
01	0x01	7	0	Crystal divider for DCO: 0 = Crystal value / 2, 1 = Bypass without using divider.
		[6..0]	00-hex	Dash Code or Device ID information
02	0x02	[7..4]	0001	Crystal Oscillator Output pin Capacitance: C_{XOUT}(pF) = 9.0 + Bits[3..0] × 1.0
		$CL_{XTAL} = C_{XIN} \times C_{XOUT} / (C_{XIN} + C_{XOUT})$ $C_{XIN} = C_{XOUT}$ recommended for optimum oscillator gain: $CL_{XTAL} = C_{XIN} / 2 = C_{XOUT} / 2$ General CL_{XTAL} resolution is 0.5pF. Resolution of 0.25pF possible by setting C_{XIN} 1 bit lower than C_{XOUT}.		
		[3..2]	00	PPS Hysteresis voltage threshold setting: 00 = 20mV (Default) 01 = 40mV 10 = 60mV 11 = 80mV
		1	0	PPS Vbias programming Bit 1
		0	0	PPS Vbias programming Bit 0
03	0x03	7	0	OTP configuration 3 protection bit: 0 = Disabled , 1 = Enabled
		6	0	OTP configuration 2 protection bit: 0 = Disabled , 1 = Enabled
		5	0	OTP configuration 1 protection bit: 0 = Disabled , 1 = Enabled
		4	0	OTP configuration 0 protection bit: 0 = Disabled , 1 = Enabled
		[3..2]	00	PPS OE2 amplitude programming: 00 = 400mV (Default) 01 = 500mV 10 = 600mV 11 = 700mV
		[1..0]	00	PPS OE1 amplitude programming: 00 = 400mV (Default) 01 = 500mV 10 = 600mV 11 = 700mV
04 (Apply to 5X1503S)	0x04	7	0	Ultra power down bit: 0 = Disabled , 1 = Enabled
		6	0	Differential CLKIN on X1/X2: 0 = Disabled , 1 = Enabled (For 5X1503 Only) 11=0xD6 / 0x6B (1)
		5	0	PLL Spread Hi-resolution Selection: 0 = Normal , 1 = Enabled, Shifted to 4-bits
		4	0	PLL 3rd pole loop filter enable bit: 0 = Disabled , 1 = Enabled

Register Address		Register Bit	Default	Function explanation
Decimal	Hex			
		3	0	Reserved.
		[2:0]	000	PLL Feedback Integer Divider, Bits[10..8]. Supported values 16 ~ 2047. Default is 48
04 (Apply to 5X1503 /5X1503L)	0x04	7	0	Ultra power down bit: 0 = Disabled , 1 = Enabled
		6	0	Differential CLKIN on X1/X2: 0 = Disabled , 1 = Enabled (For 5X1503 Only) 11 = 0xD6 / 0x6B (1)
		5	0	PLL Spread Hi-resolution Selection: 0 = Normal , 1 = Enabled, Shifted to 4-bits
		4	0	PLL 3rd pole loop filter enable bit: 0 = Disabled , 1 = Enabled
		3	0	Selection of Divide by 4: 0 = Disabled , 1 = Enabled
		[2:0]	000	PLL Feedback Integer Divider, Bits[10..8]. Supported values 16 ~ 2047. Default is 48
05	0x05	[7..0]	28-hex	PLL Feedback Divider, Bits[7..0] of 11 bits total. See 0x04 for Bits[2:0]. 5X1503S = 28-hex in default 5X1503 / 5X1503L = 30-hex in default
06	0x06	[15:8]	00-hex	PLL Fractional Feedback Divider Bit[15:8] of 16 bits total, See 0x07 for Bit[7:0] Default is 00
07	0x07	[7:0]	00-hex	PLL Fractional Feedback Divider Bit[7:0] of 16 bits total, See 0x06 for Bit[15:8] Default is 00
08	0x08	[15:8]	00-hex	PLL Spread Spectrum Step Size Control Bit[15:8] of 16 bits total, See 0x09 for Bit[7:0], Default is 00 meaning no spread function.
09	0x09	[7:0]	00-hex	PLL Spread Spectrum Step Size Control Bit[7:0] of 16 bits total, See 0x08 for Bit[15:8], Default is 00 meaning no spread function.
10	0x0A	[7:0]	00-hex	PLL Spread Period Control, Bit[7:0] of 8 bits total. Default is 00 meaning no spread function.
11	0x0B	7	1	PLL Reference Divider, Divide-by-1: 0 = Disabled , 1 = Enabled 5X1503S = 1 (default) 5X1503 / 5X1503L = 0 (default)
		6	0	PLL Reference Divider, Divide-by-2: 0 = Disabled , 1 = Enabled
		[5..0]	011010	PLL Reference Divider, Divide by 1 ~ 63. Default is 26.
12	0x0C	7	0	PLL Reference Divider Doubler: 0 = Disabled , 1 = Enabled
		6	0	PLL Reference Current Selection, 0 = 1X, 1 = 2X 5X1503S = 1 (default) 5X1503 / 5X1503L = 0 (default)
		5	0	PLL Spread Spectrum Control: 0 = Disabled, 1 = Enabled
		[4..0]	00001	For 5X1503S PLL Loop Filter Resistor. Setting 00001 for 1KΩ only. R_{LF2} (KΩ) = 7K + (1K x PLL_R1K) + (12.5K x PLL_R12.5K) + (25K x PLL_R25K) + (50K x PLL_R50K) + (100K x PLL_R100K)
		[4..0]	00011	For 5X1503 / 5X1503L PLL Loop Filter Resistor. Setting 00011 for 44.5KΩ only. R_{LF2} (KΩ) = 7K + (12.5K x PLL_R12.5K) + (25K x PLL_R25K) + (50K x PLL_R50K) + (75K x PLL_R75K) + (100K x PLL_R100K)

Register Address		Register Bit	Default	Function explanation
Decimal	Hex			
13	0x0D	[7..0]	10111001	For 5X1503S PLL Charge Pump Multiplier = Bits[4..0] + 1. Range is 1 ~ 63. [10uA x (1+SIREF)(1XCP_1X + 1XCP_2X + 1XCP_4X + 1XCP_8X + 1XCP_16X + 1XCP_31X)] / 3XCP_/3 + 24XCP_/24 I_{CP2} (μA) = 10 × (1 + B11Bit[0]) × (1 + Bits[7..3]) / (Bit[2] / 24) or (Bit[1] / 3). Default is 11×(1+0)×(1+4)/(24) = 1.667μA
			00010110	For 5X1503 / 5X1503L PLL Charge Pump Multiplier = Bits[4..0] + 1. Range is 1 ~ 63. [10uA x (1+SIREF)(1XCP_1X + 1XCP_2X + 1XCP_4X + 1XCP_8X + 1XCP_16X + 1XCP_31X)] / 3XCP_/3 + 24XCP_/24 I_{CP2} (μA) = 10 × (1 + B11Bit[0]) × (1 + Bits[7..3]) / (Bit[2] / 24) or (Bit[1] / 3). Default is 11×(1+0)×(1+4)/(24) = 1.667μA
14	0x0E	[7:3]	01010	For 5X1503S Output Divider1 (DIV1) Value, Default is 10, Refer to Table 3 in datasheet on Page6
		[7:3]	00001	For 5X1503 / 5X1503L Output Divider1 (DIV1) Value, Default is 3, Refer to Table 3 in datasheet on Page6
		2	0	Divider2 (DIV2) source clock select: 0 = REF , 1 = PLL, See Bit0 for source clock.
		1	1	Divider1 (DIV1) source clock select: 0 = REF , 1 = PLL
		0	0	Divider2 (DIV2) source seed select: 0 = disable, 1 = from DIV1, See Bit2 for DIV2 clock selection.
15	0x0F	[7:3]	00001	Output Divider1 (DIV1) Value, Default is 3, Refer to Table 3 in datasheet on Page6
		2	0	Out#3 Output state select control: 0 = Normal, 1 = Tristate
		1	0	Out#2 Output state select control: 0 = Normal, 1 = Tristate
		0	0	Out#1 Output state select control: 0 = Normal, 1 = Tristate
16	0x10	7	1	Out#1 Output enable control: 0 = Disable, 1 = Enable (Default)
		[6:5]	00	OE1 pin function selection: 00 = OUT#1 output enable/disable control (Default) 01 = Power down # 10 = OUT#1 set as PPS mode 11 = DFC0
		4	1	Out#2 Output enable control: 0 = Disable, 1 = Enable (Default)
		[3:2]	00	OE2 pin function selection: 00 = OUT#2 output enable/disable control (Default) 01 = Config_SEL 10 = OUT#2 set as PPS mode 11 = DFC1
		1	1	Out#2 Output Free-run control: 0 = Free-run, 1 = Normal (Default)
		0	0	Out#1 Output Free-run control: 0 = Free-run (Default), 1 = Normal

Register Address		Register Bit	Default	Function explanation
Decimal	Hex			
17	0x11	[7:6]	00	Out#1 output clock selection: 00 = 32.768Khz (Default) 01 = Clock from OUTDIV2 10 = N/A 11 = Clock from OUTDIV1
		[5:4]	11	Out#2 output clock selection: 00 = 32.768Khz 01 = Clock from OUTDIV2 10 = N/A 11 = Clock from OUTDIV1(Default)
		[3:2]	10	Out#3 output clock selection: 00 = 32.768Khz 01 = Clock from OUTDIV2 10 = REF (Default) 11 = Clock from OUTDIV1
		1	1	Out#3 Output enable control: 0 = Disable, 1 = Enable (Default)
		0	0	DFC function control: 0 = Disable (Default), 1 = Enable
18	0x12	7	1	PLL Power Down Control bit, 0 = Power Down PLL , 1 = PLL in operational mode, Default is PLL in Normal Operational Mode
		6	1	PLL Lock Bypass enable selection, 0 = Bypass, 1 = Not Bypass (Lock mode), Default is PLL in Not Bypass Mode
		5	0	SCLK pin (Pin1) in Hardware mode function select: 0 = OE3, 1 = DFC1
		4	0	PPS Power Down enable control: 0 = Disable (Default), 1 = Enable
		[3:2]	00	OUT#2 / OE#2 PPS timer select: 00 = 100uS (Default) 01 = 200uS 10 = 400uS 11 = 800uS
		[1:0]	00	OUT#1 / OE#1 PPS timer select: 00 = 100uS (Default) 01 = 200uS 10 = 400uS 11 = 800uS
19	0x13	7	0	OUT#1 CLK invert control: 0 = Non-Invert (Default), 1 = Invert
		6	0	OUT#2 CLK invert control: 0 = Non-Invert (Default), 1 = Invert
		5	0	OUT#3 CLK invert control: 0 = Non-Invert (Default), 1 = Invert
		4	1	Out#3 Output Free-run control: 0 = Free-run, 1 = Normal (Default)
		[3:2]	00	OUT#2 Amplitude Select Control: 00 = 1.8V (Default) 01 = 1.0V 10 = 1.1V 11 = 1.2V
		[1:0]	00	OUT#3 Amplitude Select Control: 00 = 1.8V (Default) 01 = 1.0V 10 = 1.1V 11 = 1.2V

Register Address		Register Bit	Default	Function explanation
Decimal	Hex			
20	0x14	7	1	I2C part power down control bit: 0 = I2C function in power down (Default), 1 = I2C function in operational mode (Default)
		6	0	Reference clock output (OUT#2 / OUT#3): 0 = stop (Default), 1 = Free-run
		5	0	Output clocks free run control: 0 = OUT#2 Free-run (Default), 1 = OUT#2 / OUT#3 Free-run
		4	0	Power down polarity control: 0 = Non-Invert (Default), 1 = Invert
		3	0	Bypass AC cap in X1 for 5X1503 only: 0 = Normal (Default), 1 = Bypass
		2	0	For 5X1503 / 5X1503S Reserved Bit
		1	1	For 5X1503 / 5X1503S Reserved Bit
		0	1	For 5X1503 / 5X1503S Reserved Bit
		[2:0]	011	5X1503L CLK 32K Low drive amplitude select: 000 = 1.8V 001 = 0.8V 010 = 0.9V 011 = 1.0V (Default) 100 = 1.1V 101 = 1.2V

Note 1: To be able to read this information, you already need to know the device address.

Note 2: These two bits show the configuration number 0~3 that will be loaded from OTP into registers at power-up. When changing these bits through I^2C you instruct the chip to load another configuration from OTP. This is useful for switching between OTP configurations when in I^2C mode. This method is also used to step through each configuration for reading back OTP contents.

6. Block Diagrams

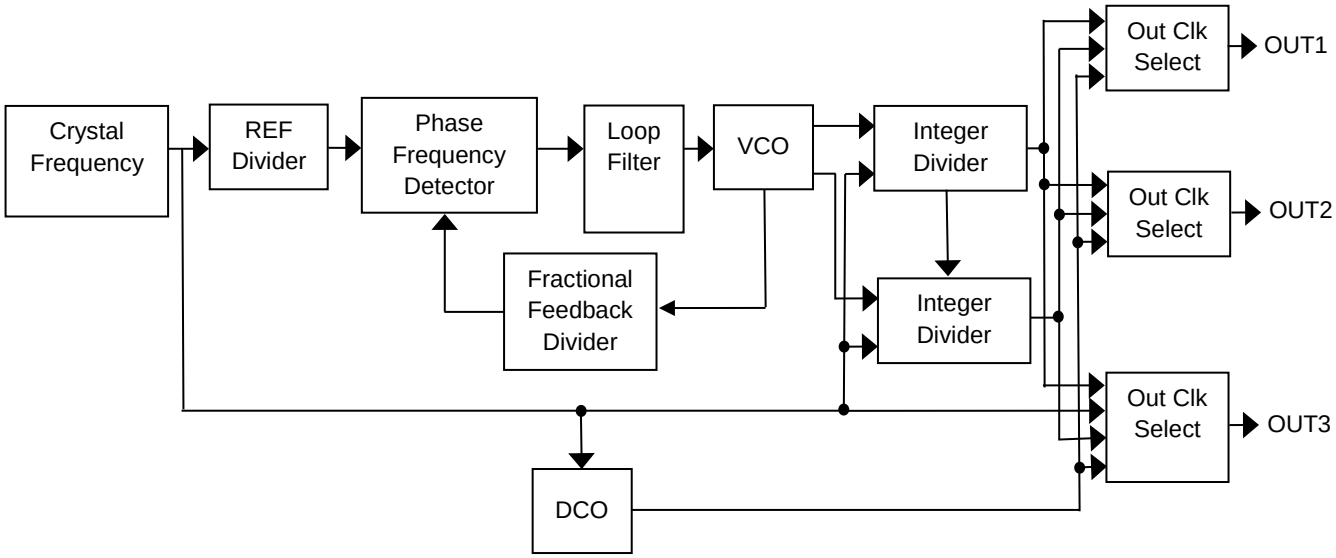


Figure 2. 5X1503 / 5X1503L

Equations:

$F_{VCO} = F_{CRYSTAL}$ / Ref Divider × (Total Feedback Divider) (see registers 0x04 ~ 0x07)

$F_{OUT1} = F_{OUT2} = F_{OUT3} = F_{VCO}$ / Integer Divider (see registers 0x14 [7:3] and 0x15 [7:3])

The total feedback divider value is the fractional and Integer counter settings.

Limit of VCO on each MicroClock Device:

For 5X1503S / 5L1503S

$F_{CRYSTAL}$: 10MHz ~ 52MHz

F_{VCO} : 500MHz ~ 1100MHz

Integer Output Divider: 1 ~ 88 (Refer to Table 3 in Datasheet)

For 5X1503 / 5X1503L / 5L1503 / 5L1503L

$F_{CRYSTAL}$: 10MHz ~ 52MHz

F_{VCO} : 50MHz ~ 130MHz

Integer Output Divider: 1 ~ 88 (Refer to Table 3 in Datasheet)

Appendix: PLL Configuration Regarding to Fractional Feedback Divider

The Fractional Feedback Divider (FFD) is composed of an 11-bit integer portion (addresses 0x04 and 0x05) and a 16-bit fractional portion (addresses 0x06 and 0x07).

FFD value P = INT(P) + FRAC(P) = F_{VCO} / F_{PFD} (1)

FFD Integer [10..0] = DEC2HEX(INT(P)) (2)

The FFD divides the VCO frequency F_{VCO} down to the phase-frequency detector frequency F_{PFD}.

F_{PFD} = F_{VCO} / (P).

Convert FRAC(P) to hex with Eq.2 where ROUND2INT means to round to the nearest integer. The round-off error of P in ppm is the output frequency error in ppm.

FFD Fraction [15..0] = DEC2HEX(ROUND2INT(2^{16}×FRAC(P))) (3)

Example: Assume a 25MHz crystal is used. If a desired frequency is 100.25MHz output clocks with a post-divider value to be 5, the VCO frequency then is 501.25MHz.

The Phase Frequency Detector frequency F_{PFD} = 25MHz and the FFD value is 501.25 / 25 = 20.05.

The integer portion is 20 so address 0x05 as <7:0> is 14-hex and address 0x04 as <10:8> is 00-hex

The fractional portion is 0.05.

FFD Fraction [15..0] = DEC2HEX(ROUND2INT(2^{16}×0.05) = DEC2HEX(ROUND2INT(3276.8))

= DEC2HEX(3277) = 0C CD

Address 0x06 as <15:8> = 0C-hex and address 0x07 as <7:0> = CD-hex.

There is a small error from the rounding. The actual FFD value is 20 + 3277 / 2^{16} = 20.050003052.

The rounding error is 20.050003052 / 20.05 – 1 = 0.152ppm.

Revision History

Revision	Date	Description
1.0	Jun.4.20	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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