

# F1912

6-Bit Digital Step Attenuator, 1MHz to 4000MHz

This document describes the specification for the Renesas F1912 Digital Step Attenuator. The F1912 is part of a family of *Glitch-Free™* DSAs optimized for the demanding requirements of Base Station (BTS) radio cards and numerous other non-BTS applications. These devices are offered in a compact 4mm x 4mm 20-pin QFN package with 50Ω impedances for ease of integration.

## Competitive Advantage

Digital step attenuators are used in receivers and transmitters to provide gain control. The F1912 is a 6-bit step attenuator optimized for these demanding applications. The silicon design has very low insertion loss and low distortion (> +60 dBm IIP3). The device has pinpoint accuracy. Most importantly, the F1912 includes Renesas' Glitch-Free™ technology, which results in low overshoot and ringing during MSB transitions.

- Glitch-Free™ technology so PA or ADC will not be damaged during when transitions.
- Extremely accurate with low distortion.
- Lowest insertion loss for best SNR

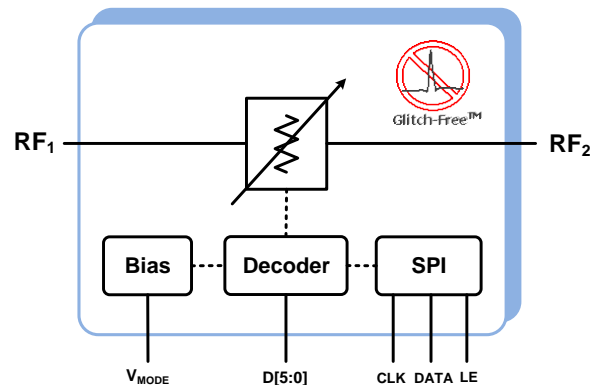
## Applications

- Base Station 2G, 3G, 4G, TDD radio cards
- Repeaters and E911 systems
- Digital Pre-Distortion
- Point to Point Infrastructure
- Public Safety Infrastructure
- WIMAX Receivers and Transmitters
- Military Systems, JTRS radios
- RFID Handheld and Portable Readers
- Cable Infrastructure

## Features

- Serial and 6-bit Parallel Interface
- 31.5dB Control Range
- 0.5dB step
- *Glitch-Free™*, low transient overshoot
- 3.0 V to 5.25 V supply
- 1.8 V or 3.3 V control logic
- Attenuation Error < 0.20 dB at 2GHz
- Low Insertion Loss < 1.4 dB at 2GHz
- Ultra Linear IIP3 > +60dBm
- IIP2 = +110 dBm typical
- Stable Integral Non-Linearity over temperature
- Low Current Consumption 550 μA typical
- -55 °C to +105 °C operating temperature
- 4 x 4 mm Thin QFN 20-pin package

## Block Diagram



## Part Number Details

Part#	Freq Range (MHz)	Resolution / Range (dB)	Control	IL (dB)	Pinout
F1950	150 - 4000	0.25 / 31.75	Parallel & Serial	1.3	PE43702 PE43701
F1951	100 - 4000	0.50 / 31.5	Serial Only	1.2	HMC305
F1952	100 - 4000	0.50 / 15.5	Serial Only	0.9	HMC305
F1953	400 - 4000	0.50 / 31.5	Parallel & Serial	1.3	PE4302 DAT-31R5
F1956	1 - 4000	0.25 / 31.75	Parallel & Serial	1.4	PE43705, RFSA3715
F1912	1 - 4000	0.50 / 31.5	Parallel & Serial	1.4	PE4312 PE4302

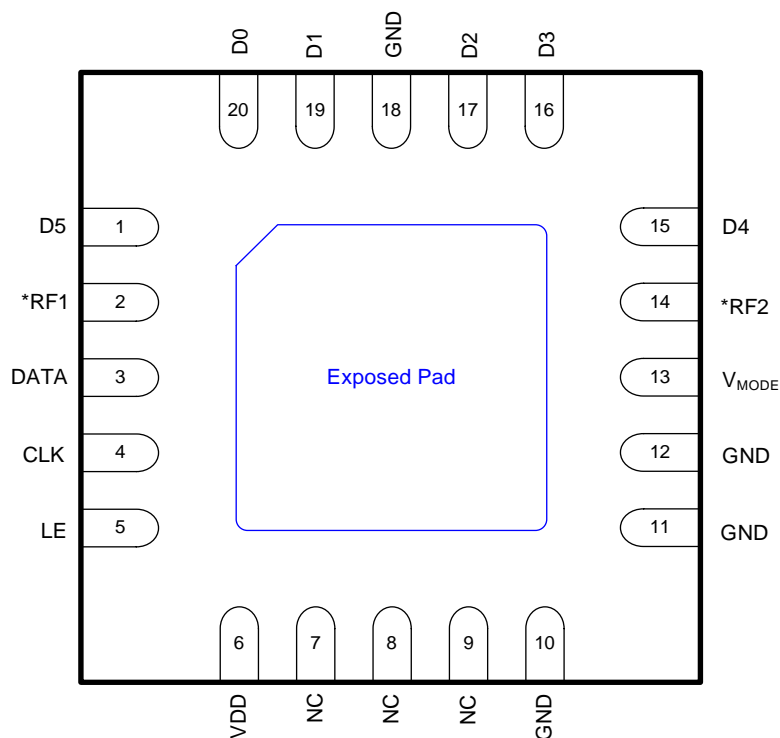
## Contents

<b>1. Pin Information</b>	<b>3</b>
1.1 Pin Assignments	3
1.2 Pin Descriptions	3
<b>2. Specifications</b>	<b>5</b>
2.1 Absolute Maximum Ratings	5
2.2 ESD Caution	5
2.3 Package Thermal and Moisture Characteristics	5
2.4 Recommended Operating Conditions	6
2.5 Electrical Specifications	7
<b>3. Functional Description</b>	<b>9</b>
3.1 Programming Options	9
3.2 Serial Control Mode	9
3.2.1 Serial Mode Register Timing Diagram	9
3.2.2 Serial Mode Default Startup Condition	10
3.3 Parallel Control Mode	11
3.3.1 Direct Parallel Mode	11
3.3.2 Latched Parallel Mode	11
<b>4. Typical Operating Conditions (TOC)</b>	<b>12</b>
<b>5. Evaluation Board</b>	<b>16</b>
5.1 Evaluation Kit Picture	16
5.2 Evaluation Kit Applications Circuit	17
5.3 Evaluation Kit BOM	17
<b>6. Applications Information</b>	<b>18</b>
6.1 F1912 Digital Pin Voltage and Resistance Values (Pins Not Connected)	18
6.2 Logic Voltage Applied before Power Supply	18
<b>7. Package Outline Drawings</b>	<b>18</b>
<b>8. Marking Diagram</b>	<b>19</b>
<b>9. Ordering Information</b>	<b>19</b>
<b>10. Revision History</b>	<b>19</b>

# 1. Pin Information

## 1.1 Pin Assignments

TOP View  
(looking through the top of the package)



\* Device is RF Bi-Directional

## 1.2 Pin Descriptions

Pin	Name	Function
1	D5	16 dB Attenuation Control Bit. Pull high for 16 dB ATTN.
2	RF1	Device RF input or output (bi-directional). Internally DC blocked.
3	DATA	Serial interface Data Input.
4	CLK	Serial interface Clock Input.
5	LE	Serial interface Latch Enable Input. Internal pullup (100K ohm).
6	VDD	Power supply pin.
7	NC	Internally unconnected.
8	NC	Internally unconnected.
9	NC	Internally unconnected.
10	GND	Connect to Ground. This pin is internally connected to the exposed paddle.

Pin	Name	Function
11	GND	Connect to Ground. This pin is internally connected to the exposed paddle.
12	GND	Connect to Ground. This pin is internally unconnected.
13	VMODE	Pull high for serial control mode. Ground for parallel control mode.
14	RF2	Device RF input or output (bi-directional). Internally DC blocked.
15	D4	8 dB Attenuation Control Bit. Pull high for 8 dB ATTN.
16	D3	4 dB Attenuation Control Bit. Pull high for 4 dB ATTN.
17	D2	2 dB Attenuation Control Bit. Pull high for 2 dB ATTN.
18	GND	Connect to Ground. This pin is internally unconnected.
19	D1	1 dB Attenuation Control Bit. Pull high for 1 dB ATTN.
20	D0	0.5 dB Attenuation Control Bit. Pull high for 0.5 dB ATTN.
EPAD	Exposed Paddle	Exposed Pad. Internally connected to GND. Solder this exposed pad to a PCB pad that uses multiple ground vias to provide heat transfer out of the device into the PCB ground planes. These multiple via grounds are also required to achieve the specified RF performance.

## 2. Specifications

### 2.1 Absolute Maximum Ratings

Parameter	Symbol	Minimum	Maximum	Unit
V <sub>DD</sub> to GND	V <sub>DD</sub>	-0.3	+5.5	V
DATA, LE, CLK, D[5:0]	V <sub>Logic</sub>	-0.3	Lower of (V <sub>DD</sub> +0.3, 3.9)	V
RF1, RF2	V <sub>RF</sub>	-0.3	+0.3	V
Maximum Input Power applied to RF1 or RF2 (>100 MHz)	P <sub>RF</sub>		+34	dBm
Operating Case Temperature			+105	°C
Maximum Junction Temperature	T <sub>Jmax</sub>		+140	°C
Junction Temperature	T <sub>jmax</sub>		140	°C
Continuous Power Dissipation			1.5	W
Storage Temperature Range	T <sub>st</sub>	-65	150	°C
Lead Temperature (soldering, 10s)			260	°C
Electrostatic Discharge – HBM (JEDEC/ESDA JS-001-2012)	V <sub>ESDHBM</sub>		2000 (Class 2)	Volts
ESD Voltage – CDM (Per JESD22-C101F)	V <sub>ESDCDM</sub>		500 (Class C2)	Volts

Stresses above those listed above may cause permanent damage to the device. Functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

### 2.2 ESD Caution

This product features proprietary protection circuitry. However, it may be damaged if subjected to high energy ESD. Please use proper ESD precautions when handling to avoid damage or loss of performance.

### 2.3 Package Thermal and Moisture Characteristics

$\theta_{JA}$ (Junction – Ambient)	50 °C/W
$\theta_{JC}$ (Junction – Case) [The Case is defined as the exposed paddle]	3 °C/W
Moisture Sensitivity Rating (Per J-STD-020)	MSL1

## 2.4 Recommended Operating Conditions

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Supply Voltage(s)	$V_{DD}$		3		5.25	V
Frequency Range	$F_{RF}$		1		4000	MHz
Operating Temperature Range	$T_{CASE}$	Exposed Paddle	-55		105	°C
RF CW Input Power	PCW	RF1 or RF2			See Figure 1	dBm
Source Impedance	$Z_{Source}$	Single Ended		50		$\Omega$
Load Impedance	$Z_{Load}$	Single Ended		50		$\Omega$

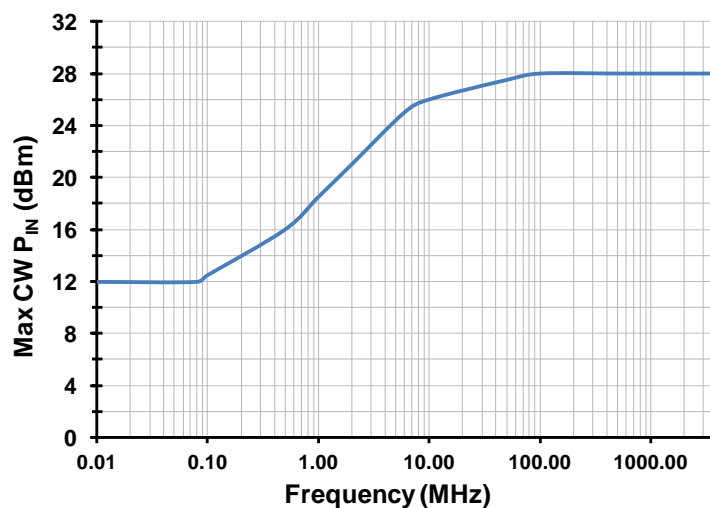


Figure 1. Maximum Continuous Operating RF input power versus Input Frequency

## 2.5 Electrical Specifications

Specifications apply at  $V_{DD} = +3.3\text{ V}$ ,  $T_{CASE} = +25\text{ }^{\circ}\text{C}$ ,  $F_{RF} = 2000\text{ MHz}$ ,  $P_{IN} = 0\text{ dBm}$ , Serial Mode ( $V_{MODE} > V_{IH}$ ),  $Z_{source} = Z_{Load} = 50\text{ }\Omega$  unless otherwise noted. EVKit losses are de-embedded.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit	
Logic Input High <sup>5</sup>	$V_{IH}$	All Control Pins					
		$V_{DD} > 3.9\text{ V}$	<b>1.17<sup>1</sup></b>		<b>3.6</b>	V	
		$3.0 \leq V_{DD} \leq 3.9\text{ V}$	<b>1.17</b>		Lower of ( $V_{DD}+0.3, 3.6$ )	V	
Logic Input Low <sup>5</sup>	$V_{IL}$	All Control Pins			<b>0.63</b>	V	
Logic Current	$I_{IH}, I_{IL}$	All Control Pins	<b>-35</b>		<b>+35</b>	$\mu\text{A}$	
Supply Current	$I_{DD}$	$V_{DD} = 3.3\text{ V}$		550	<b>830</b>	$\mu\text{A}$	
		$V_{DD} = 5.0\text{ V}$		620	<b>900</b>		
RF1 Return Loss	$S_{11}$			18		dB	
RF2 Return Loss	$S_{22}$			18		dB	
Attenuation Step	LSB	Least Significant Bit		0.5		dB	
Insertion Loss (Minimum Attenuation)	$A_{MIN}$	D[5:0]=[000000] (IL State)		1.4	<b>2.0</b>	dB	
Insertion Loss (Maximum Attenuation)	$A_{MAX}$	D[5:0]=[111111]=31.5 dB	$32^2$	33.0		dB	
Step Error	DNL			0.10		dB	
Absolute Error	INL	D[5:0]=[100111]= 19.5 dB	<b>-0.7</b>		<b>+0.5</b>	dB	
Relative Phase (max to min attenuation)	$\Phi_{\Delta}$	At 2 GHz		27		Deg	
		At 4 GHz		55			
Input IP3	IIP3	$P_{IN} = +10\text{ dBm/ tone}$ , Tone Spacing = 50 MHz				dBm	
		Attn = 0.0 dB, $RF_{in} = RF1$	60	64.0			
		Attn = 0.0 dB, $RF_{in} = RF2$	56	60.5			
		Attn =15.5 dB, $RF_{in} = RF1$	56	61.0			
	IIP3	Attn =15.5 dB, $RF_{in} = RF2$	57	61.5			
		Attn = 0.00 dB, $RF_{in} = RF1$ $P_{IN} = +22\text{ dBm per tone}$ 1 MHz Tone Separation					
		$F_{RF} = 0.7\text{ GHz}$	60	62.5		dBm	
		$F_{RF} = 1.8\text{ GHz}$	58	61.5			
$F_{RF} = 2.2\text{ GHz}$		58	61.0				
$F_{RF} = 2.6\text{ GHz}$	57	60.5					

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Input IP2	IIP2	$P_{IN} = +12\text{dBm}/\text{tone}$ , $V_{DD}=5.0\text{V}$ $F1=945\text{ MHz}$ , $F2= 949\text{ MHz}$ $F1+F2 = 1894\text{ MHz}$ $RF_{IN}= RF1$		110		dBm
0.1dB Compression <sup>3</sup>	$P_{0.1}$	D[5:0] = [000000] = 0 dB		31		dBm
MSB Step Time	$t_{LSB}$	LE rising edge to within $\pm 0.10$ dB Pout settling for 15.5 dB to 16.0 dB transition		500		ns
Maximum spurious level on any RF port <sup>4</sup>	$Spur_{MAX}$			-140		dBm
Maximum Switching Frequency	$SW_{FREQ}$			25		kHz
DSA Settling time	$\tau_{SET}$	Max to Min Attenuation to settle to within 0.5 dB of final value		0.9		$\mu\text{s}$
		Min to Max Attenuation to settle to within 0.5 dB of final value		1.8		
Control Interface	$SPI_{BIT}$			6		bit
Serial Clock Speed	$SPI_{CLK}$				<b>25</b>	MHz

1. Items in min/max columns in **bold italics** are confirmed by Test.
2. Items in min/max columns that are not bold/italics are confirmed by Design Characterization.
3. The input 0.1dB compression point is a linearity figure of merit. Refer to Absolute Maximum Ratings section for the maximum RF input power.
4. Spurious due to on-chip negative voltage generator. Typical generator fundamental frequency is 2.2 MHz.
5. The power supply voltage must be applied before all other voltages. See Applications Information.



## 3. Functional Description

### 3.1 Programming Options

F1912 can be programmed using either the parallel or serial interface, which is selectable via  $V_{MODE}$  (pin 13). Serial mode is selected by floating  $V_{MODE}$  or pulling it to a voltage logic high (greater than  $V_{IH}$ ) and parallel mode is selected by setting  $V_{MODE}$  to logic low (less than  $V_{IL}$ ).

### 3.2 Serial Control Mode

F1912 Serial mode is selected by floating  $V_{MODE}$  (pin 13) or pulling it to a voltage  $> V_{IH}$ . The serial interface is a 6 bit shift register to shift in the data MSB (D5) first. When serial programming is used, all the parallel control input pins (1, 15, 16, 17, 19, 20) **must** be grounded.

**Table 1. 6 Bit SPI Word Sequence**

D5	Attenuation 16 dB Control Bit
D4	Attenuator 8 dB Control Bit
D3	Attenuator 4 dB Control Bit
D2	Attenuator 2 dB Control Bit
D1	Attenuator 1 dB Control Bit
D0	Attenuator 0.5 dB Control Bit

**Table 2. Truth Table for Serial Control Word**

D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	Attenuation (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0.5
0	0	0	0	1	0	1
0	0	0	1	0	0	2
0	0	1	0	0	0	4
0	1	0	0	0	0	8
1	0	0	0	0	0	16
1	1	1	1	1	1	31.5

#### 3.2.1. Serial Mode Register Timing Diagram

With serial control, the F1912 can be programmed via the serial port on the rising edge of Latch Enable (LE), which loads the last 6 DATA line bits [formatted MSB (D5) first] resident in the SHIFT register followed by the next 5 bits.

Note The Timing Spec Intervals In [Blue](#).

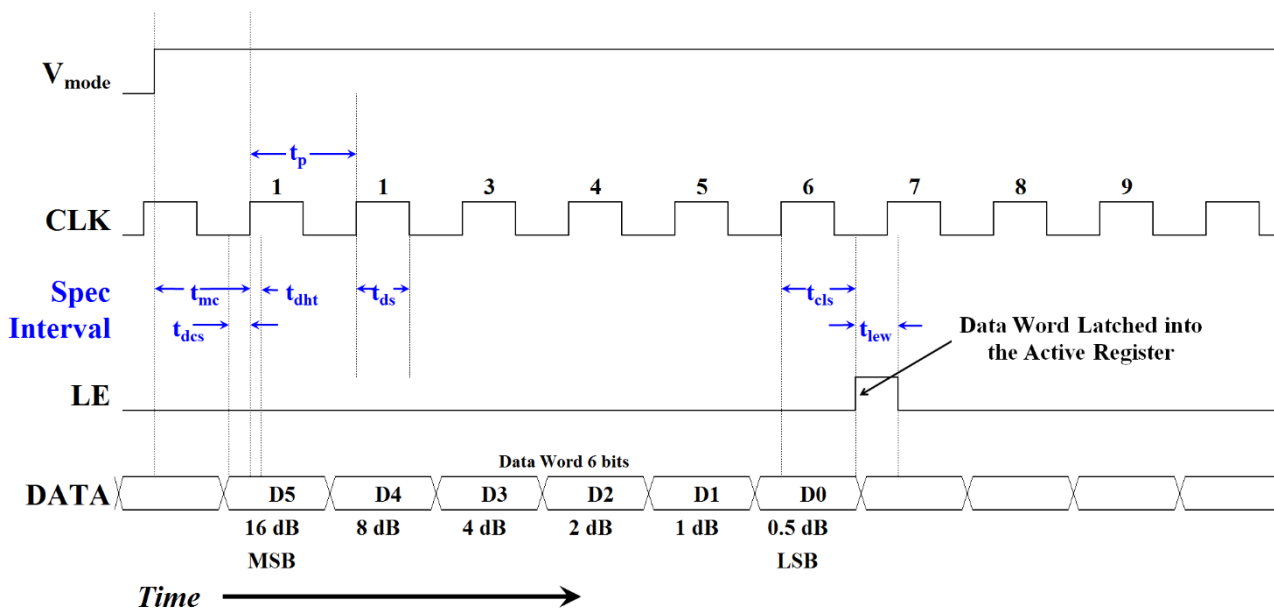


Figure 2. Serial Register Timing Diagram

Note: When Latch enable is high, the shift register is disabled and DATA is NOT continuously clocked into the shift register which minimizes noise. It is recommended that Latch enable be left high when the device is not being programmed.

Table 3. Serial Mode Timing Table

Interval Symbol	Description	Min Spec	Max Spec	Unit
$t_{mc}$	Parallel to Serial Setup Time - From rising edge of $V_{MODE}$ to rising edge of $CLK$ for D5	100		ns
$t_{ds}$	Clock high pulse width	10		ns
$t_{cls}$	LE Setup Time - From the rising edge of $CLK$ pulse for D0 to $LE$ rising edge minus half the clock period.	10		ns
$t_{lew}$	LE pulse width	30		ns
$t_{dsc}$	Data Setup Time - From the starting edge of Data bit to rising edge of $CLK$	10		ns
$t_{dht}$	Data Hold Time - From rising edge of $CLK$ to falling edge of the Data bit.	10		ns

### 3.2.2. Serial Mode Default Startup Condition:

When the device is first powered up it will default to the Maximum Attenuation of 31.5 dB independent of the  $V_{MODE}$  and parallel pin [D5:D0] conditions.

Table 4. Default Control Word for the Serial Mode

D5 (MSB)	D4	D3	D2	D1	D0 (LSB)	Attenuation (dB)
1	1	1	1	1	1	31.5

### 3.3 Parallel Control Mode

For the F1912 the user has the option of running in one of two parallel modes. Direct Parallel Mode or Latched Parallel Mode.

#### 3.3.1. Direct Parallel Mode

Direct Parallel Mode is selected when  $V_{MODE}$  (pin 13) is less than  $V_{IL}$  and LE (pin 5) is greater than  $V_{IH}$ . In this mode the device will immediately react to any voltage changes to the parallel control pins [pins 1, 15, 16, 17, 19, 20]. Use direct parallel mode for the fastest settling time.

#### 3.3.2. Latched Parallel Mode

Latched Parallel Mode is selected when  $V_{MODE}$  is less than  $V_{IL}$  and LE (pin 5) is toggled from less than  $V_{IL}$  to greater than  $V_{IH}$ . To utilize Latched Parallel Mode:

- Set  $LE < V_{IL}$
- Adjust pins [pins 1, 15, 16, 17, 19, 20] to the desired attenuation setting. (Note the device will not react to these pins while  $LE < V_{IL}$ .)
- Pull  $LE > V_{IH}$ . The device will then transition to the attenuation settings reflected by pins D5 – D0.

Latched Parallel Mode implies a default state for when the device is first powered up with  $V_{MODE} < V_{IL}$  and  $LE < V_{IL}$ . In this case the default setting is MAXIMUM Attenuation.

**Table 5 - Truth Table for the Parallel Control Word**

D5	D4	D3	D2	D1	D0	Attenuation (dB)
0	0	0	0	0	0	0
0	0	0	0	0	1	0.5
0	0	0	0	1	0	1
0	0	0	1	0	0	2
0	0	1	0	0	0	4
0	1	0	0	0	0	8
1	0	0	0	0	0	16
1	1	1	1	1	1	31.5

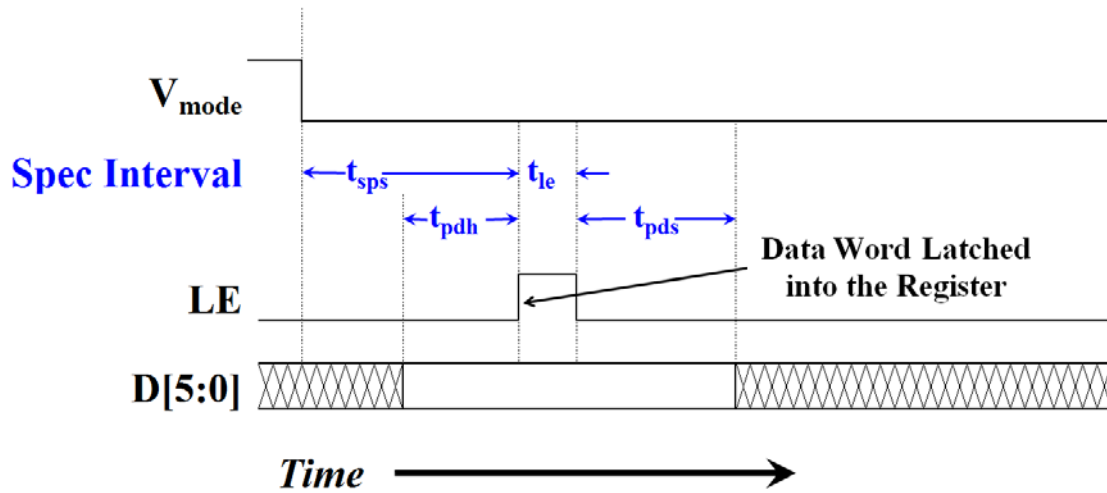


Figure 3. Latched Parallel Mode Timing Diagram

Table 6. Latched Parallel Mode Timing

Interval Symbol	Description	Min Spec	Max Spec	Unit
$t_{sps}$	Serial to Parallel Mode Setup Time	100		ns
$t_{pdh}$	Parallel Data Hold Time	10		ns
$t_{pds}$	LE minimum pulse width	10		ns
$t_{le}$	Parallel Data Setup Time	10		ns

## 4. Typical Operating Conditions (TOC)

Unless otherwise noted for the TOC graphs on the following pages, the following conditions apply.

- $V_{DD} = +3.30\text{ V}$
- $T_{CASE} = +25\text{ °C}$
- $F_{RF} = 2\text{ GHz}$
- $P_{IN} = 0\text{ dBm}$  for single tone measurements
- $P_{IN} = +10\text{ dBm/tone}$  for multi-tone measurements
- Tone Spacing = 50 MHz
- EVKit connector and board losses are de-embedded

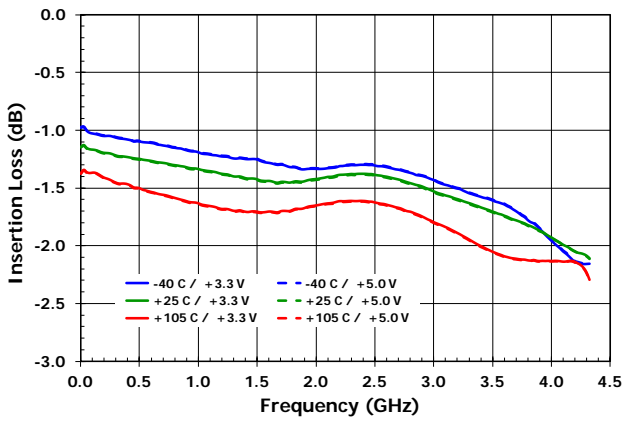


Figure 4. Insertion Loss vs Frequency

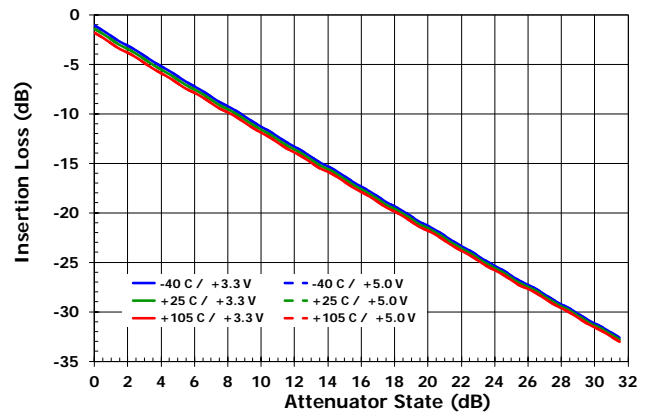


Figure 5. Insertion Loss vs Attenuation State

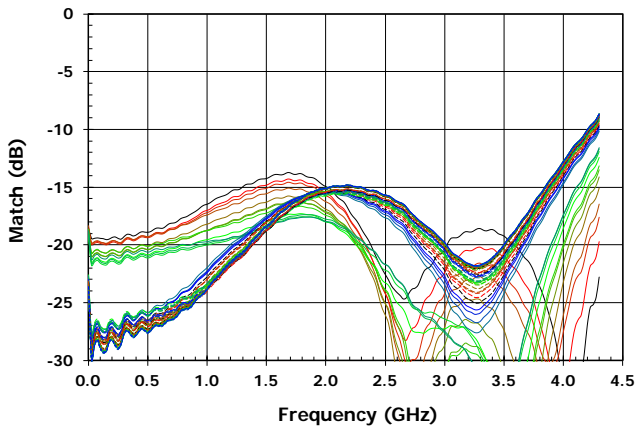


Figure 6. RF1 (Input) Return Loss vs Frequency [All States]

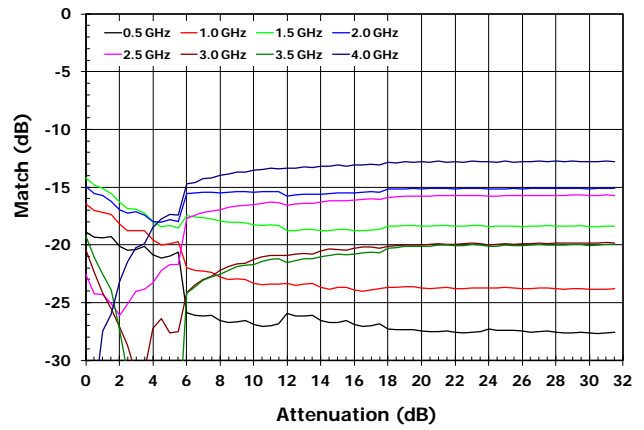


Figure 7. RF2 (Output) Return Loss vs Attenuation State

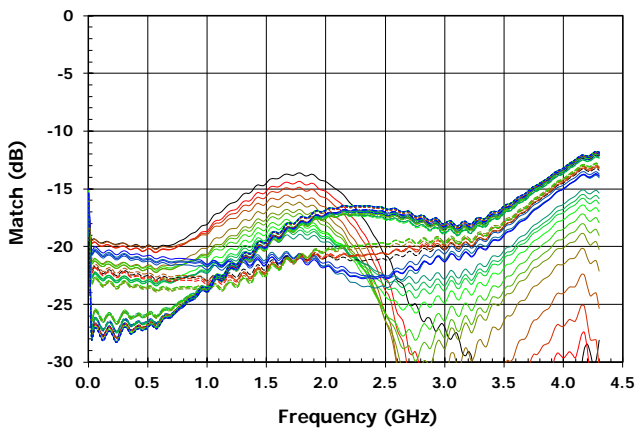


Figure 8. RF2 (Output) Return Loss vs Frequency [All States]

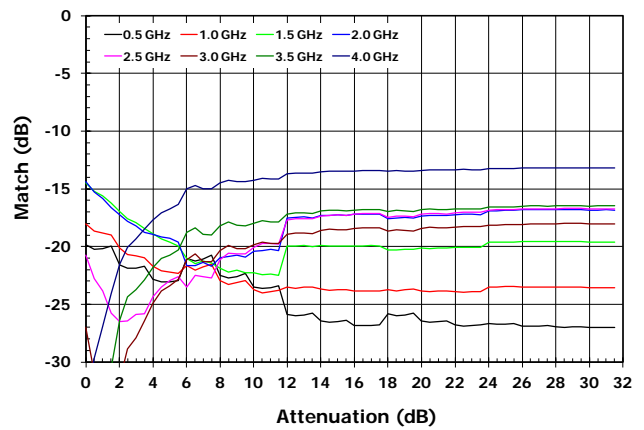


Figure 9. RF2 (Output) Return Loss vs Attenuation State

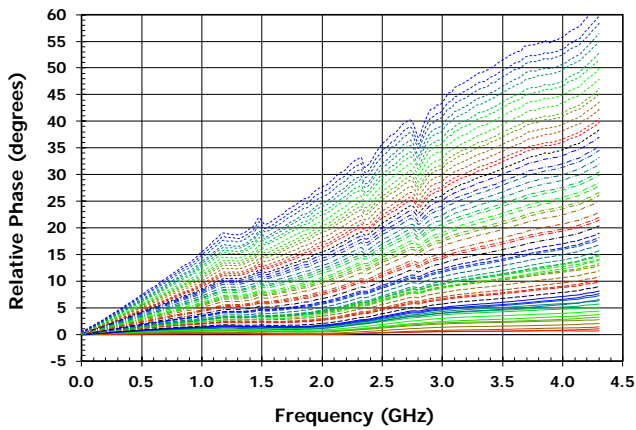


Figure 10. Relative Insertion Phase vs Frequency

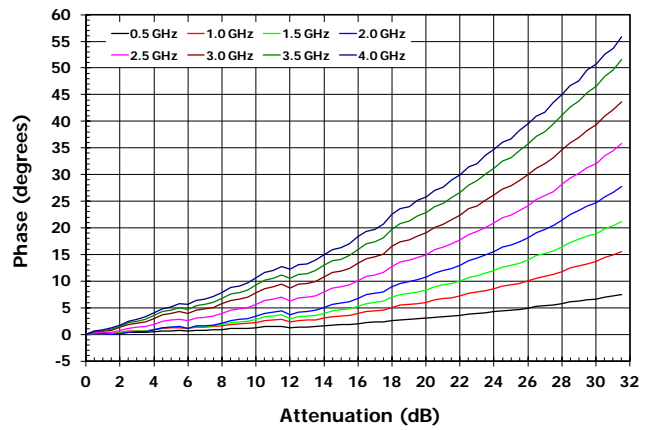


Figure 11. Relative Insertion Phase vs Attenuation

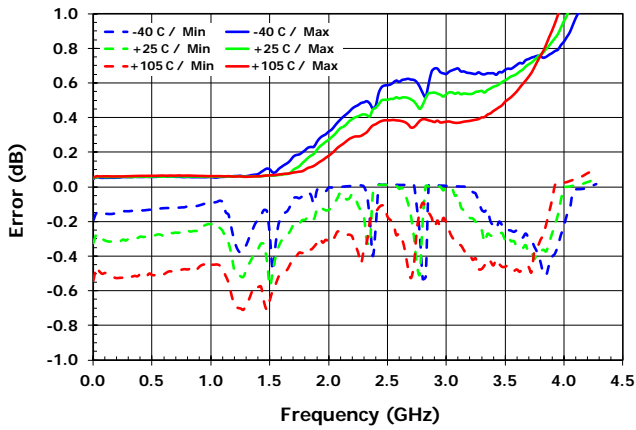


Figure 12. Worst Case Absolute Accuracy vs Frequency

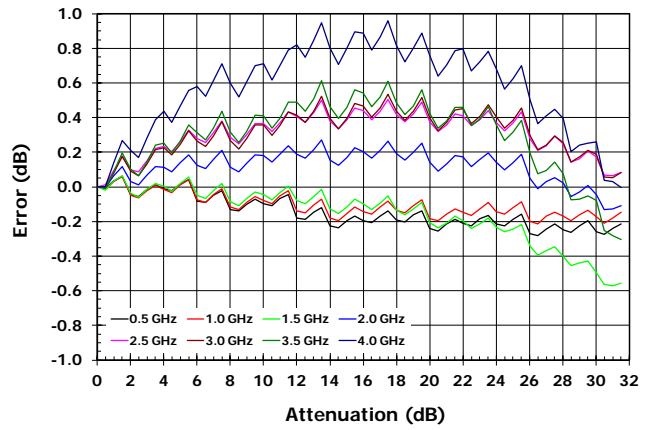


Figure 13. Absolute Accuracy vs Attenuation

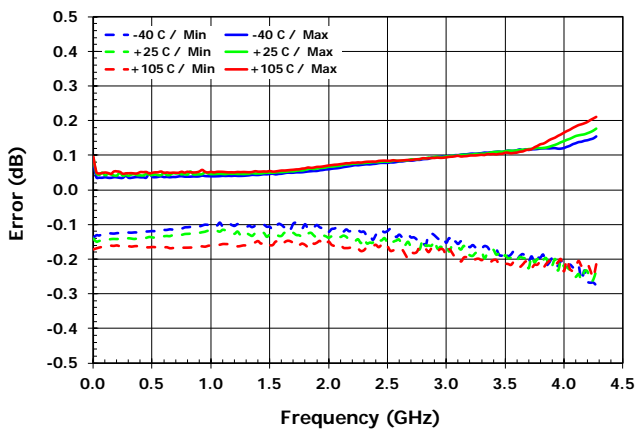


Figure 14. Worst Case Step Accuracy vs Frequency

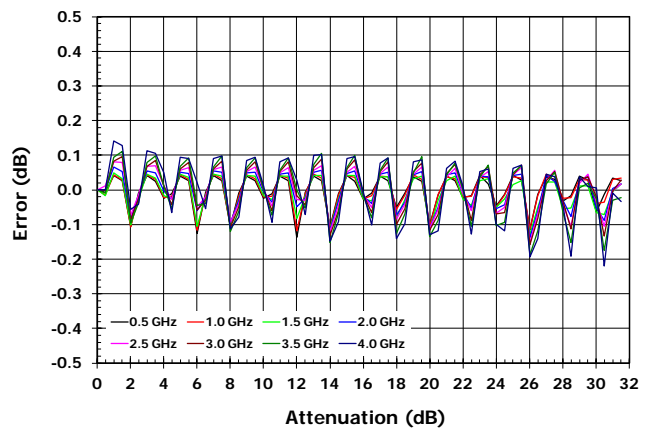


Figure 15. Step Accuracy vs Attenuation

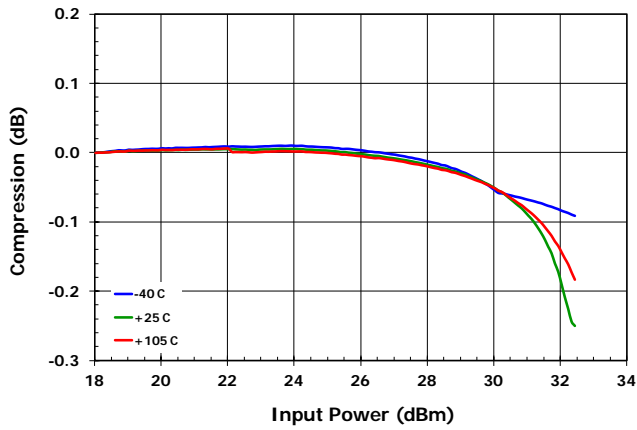


Figure 16. Compression at 0 dB and 2 GHz

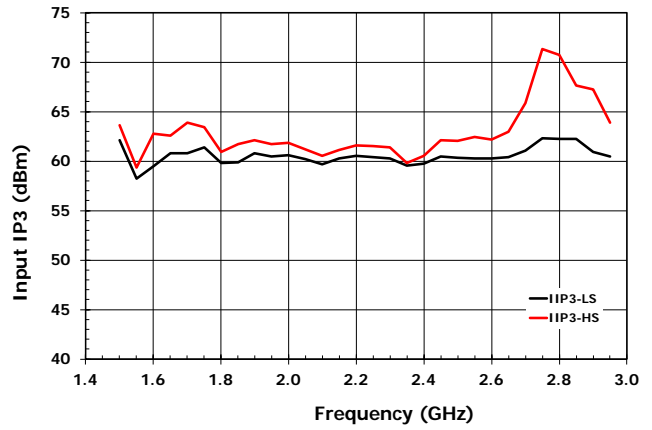


Figure 17. Input IP3 - 0 dB, +22 dBm, 1 MHz Tone Delta, RF1

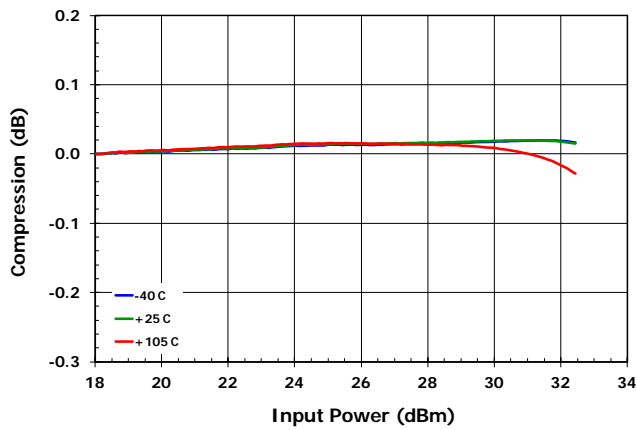


Figure 18. Compression at 15.5 dB and 2 GHz

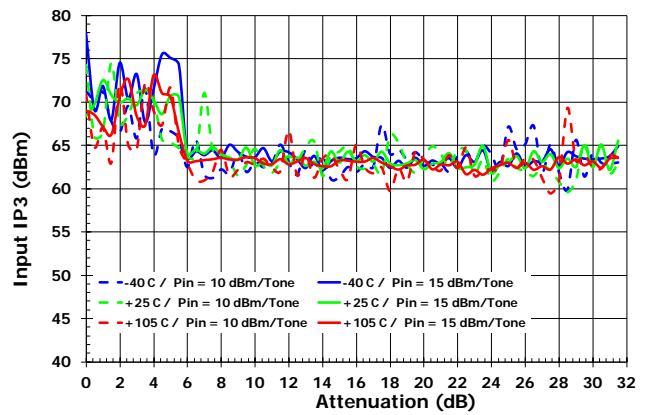


Figure 19. Input IP3 (Low Side) vs attenuation at 2GHz

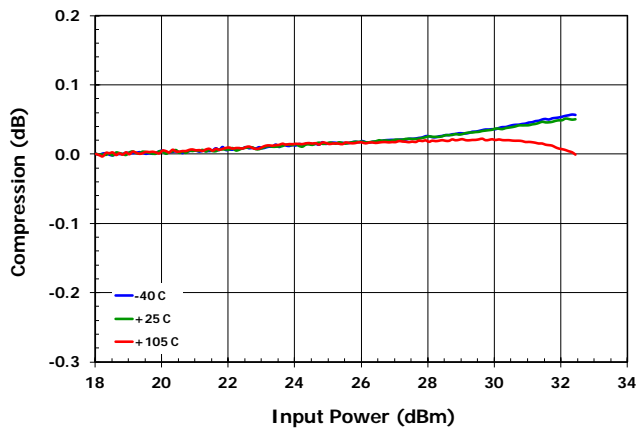


Figure 20. Compression at 31.5 dB and 2 GHz

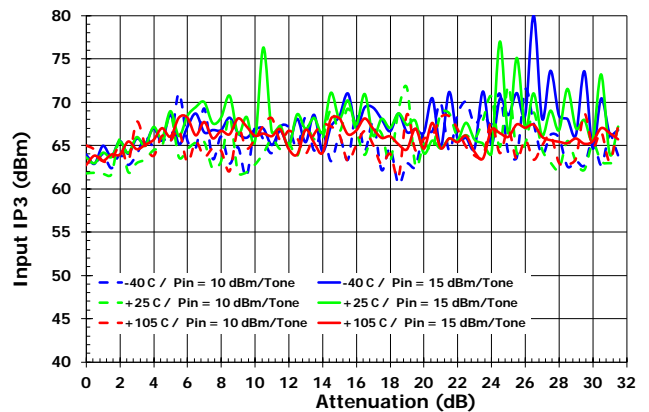
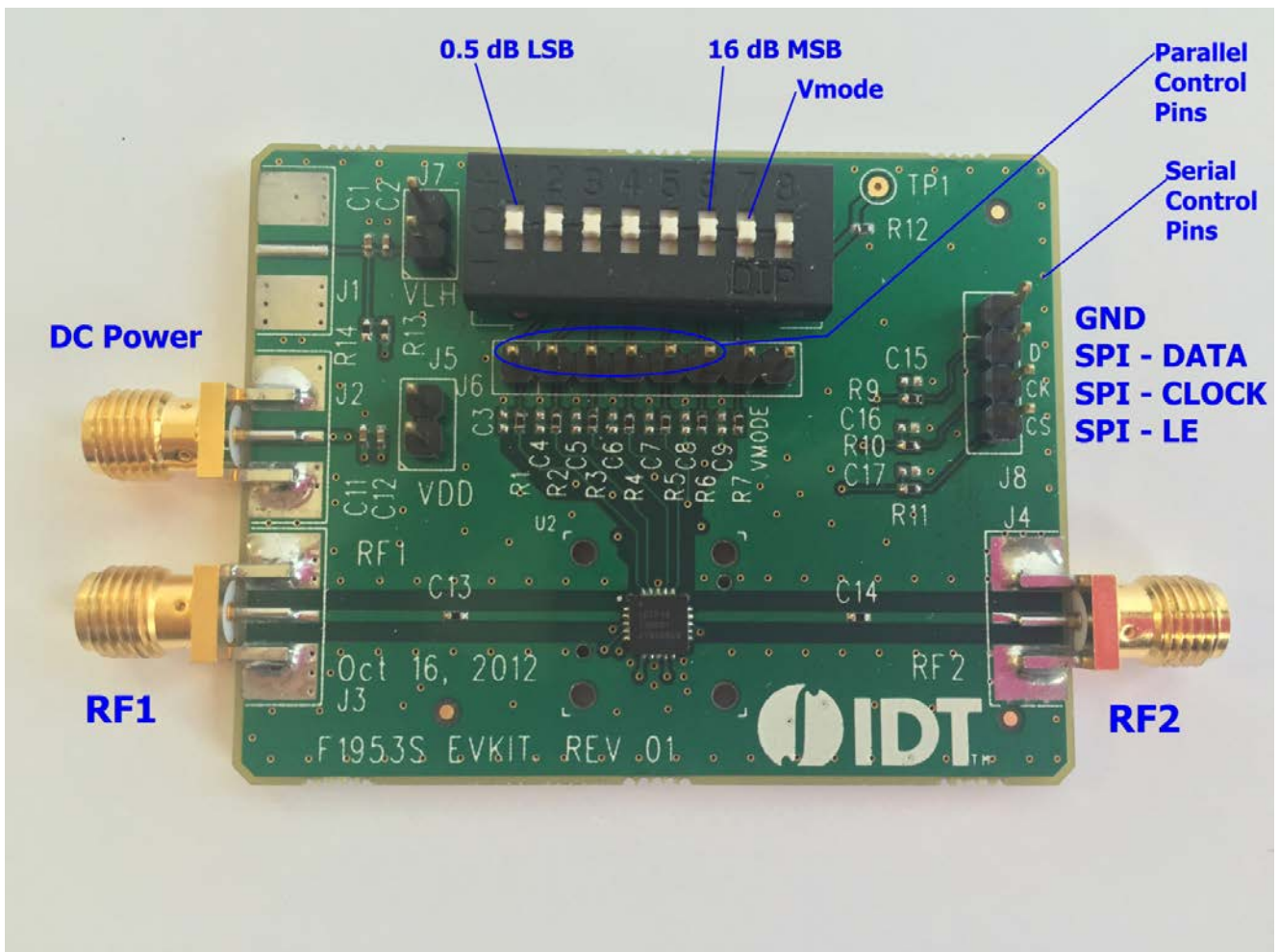


Figure 21. Input IP3 (High Side) vs attenuation at 2GHz

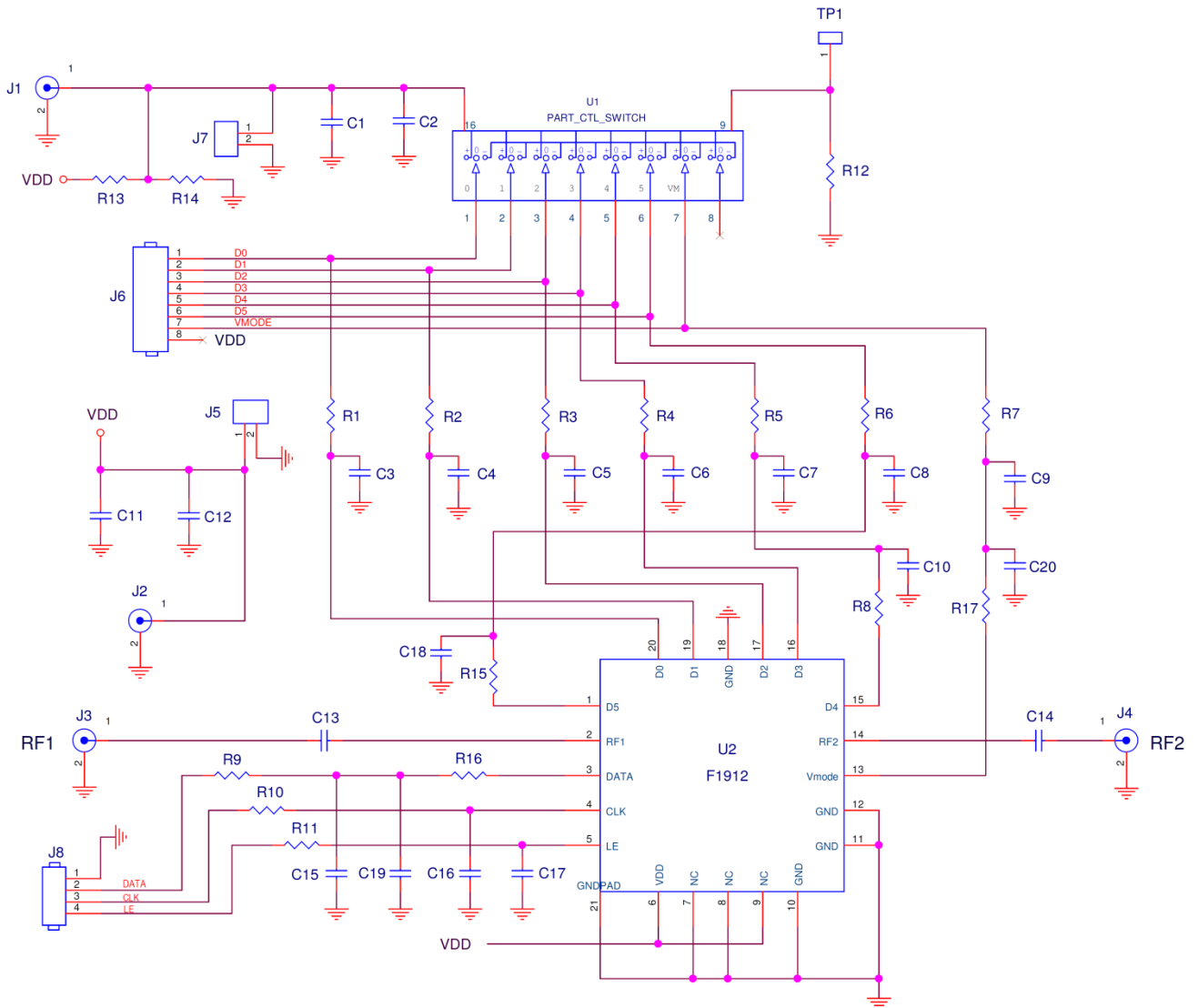
## 5. Evaluation Board

### 5.1 Evaluation Kit Picture





## 5.2 Evaluation Kit Applications Circuit



## 5.3 Evaluation Kit BOM

Item #	Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
1	C1, C11	2	100nF ±10%, 50V, X7R Ceramic Capacitor (0402)	GRM155R71H104K	MURATA
2	C2, C12	2	10nF ±5%, 50V, C0G Ceramic Capacitor (0402)	GRM155R71H103J	MURATA
3	R12, C13, C14	3	0Ω Resistors (0402)	ERJ-2GE0R00X	PANASONIC
4	R1-R7	7	100Ω ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1000X	PANASONIC
5	R9, R10, R11	3	3kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF3001X	PANASONIC
6	R8, R15, R16, R17	4	10kΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1002X	PANASONIC
7	R13	1	100KΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF1003X	PANASONIC
8	R14	1	267KΩ ±1%, 1/10W, Resistor (0402)	ERJ-2RKF2673X	PANASONIC

Item #	Part Reference	QTY	DESCRIPTION	Mfr. Part #	Mfr.
9	J5, J7	2	CONN HEADER VERT SGL 2 X 1 POS GOLD	961102-6404-AR	3M
10	J8	1	CONN HEADER VERT SGL 4 X 1 POS GOLD	961104-6404-AR	3M
11	J6	1	CONN HEADER VERT SGL 8 X 1 POS GOLD	961108-6404-AR	3M
12	J2, J3, J4	3	Edge Launch SMA (0.250 inch pitch ground, round)	142-0711-821	Emerson Johnson
13	U1	1	SWITCH 8 POSITION DIP SWITCH	KAT1108E	E-Switch
14	U2	1	DSA	F1912Z	IDT (Renesas)
15		1	Printed Circuit Board (Rev 01)	F1953S EVKit Rev 01	IDT (Renesas)
16			Bill Of Material (Rev 01)		

## 6. Applications Information

### 6.1 F1912 Digital Pin Voltage and Resistance Values (Pins Not Connected)

The following table lists the resistance between various pins and ground when no DC power is applied. When the device is powered up with +5 Volts DC these same pins should have the measured voltage to ground.

Pin	Name	DC Voltage (volts)	Resistance (ohms)
13	V <sub>MODE</sub>	2.5V	100 kΩ pullup resistor to internally regulated 2.5 V
3, 4, 5	DATA, CLK, LE	2.5V	100 kΩ pullup resistor to internally regulated 2.5 V

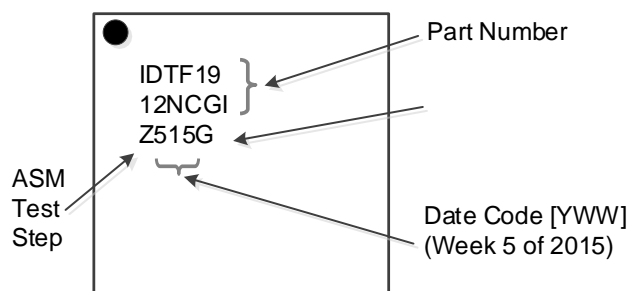
### 6.2 Logic Voltage Applied before Power Supply

Due to on-chip ESD protection circuitry, the V<sub>DD</sub> supply voltage is required to be present before the logic voltages can be applied to the logic pins (V<sub>MODE</sub>, DATA, LE, CLK, D[5:0]). If in the application this is not possible, then a series resistor of 3kΩ needs to be added in line with each of the logic pins, D0-D3. The other logic pins (V<sub>MODE</sub>, DATA, LE, CLK, D4, D5) already have a significant resistor value per the Bill Of Material (BOM). This resistor limits the current into the logic pin to a safe level when V<sub>DD</sub> is not present. The resistor should be placed close to the device to minimize the impact on switching speed due to stray PCB parasitics.

## 7. Package Outline Drawings

The package outline drawings are located at the end of this document and are accessible from the Renesas website. The package information is the most current data available and is subject to change without revision of this document.

## 8. Marking Diagram



## 9. Ordering Information

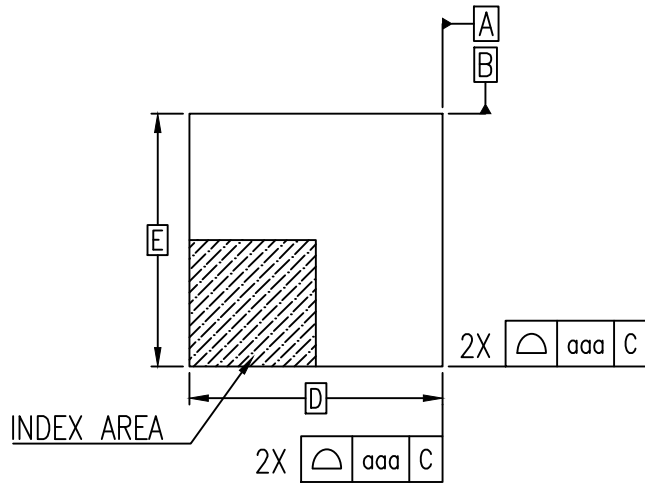
Part Number	Package Description	Carrier Type	Temperature Range
F1912NCGI8	<a href="#">20-QFN</a> 4.00 × 4.00 × 0.75 mm, 0.50mm Pitch	Tape and Reel	-40°C to +95°C
F1912NCGI	<a href="#">20-QFN</a> 4.00 × 4.00 × 0.75 mm, 0.50mm Pitch	Tray	

## 10. Revision History

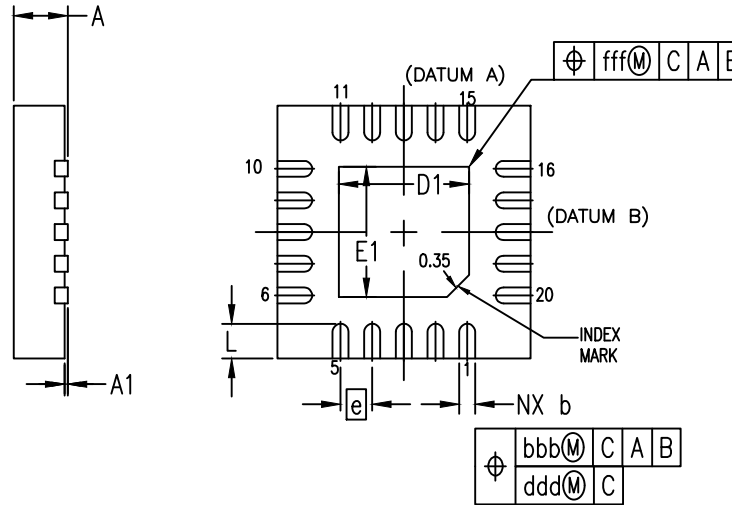
Revision	Date	Description
1.00	Nov 10, 2022	<ul style="list-style-type: none"> <li>Changed the recommended minimum operating range from -40°C to -55°C</li> <li>Reformatted the document with the latest template</li> </ul>
-	Jul 10, 2017	<ul style="list-style-type: none"> <li>Corrected logic voltages in absolute maximum rating table and operating condition table.</li> <li>Added paragraph in Application Information with respect to the logic and power supply voltages.</li> </ul>
-	May 26, 2017	Corrected pin label.
-	Jun 6, 2015	Initial release.

DATE CREATED		REVISIONS		
REV	DESCRIPTION	AUTHOR		
10/09/12	00	INITIAL RELEASE		KS
12/4/13	01	COMBINE POD & LAND PATTERN		J.H
2/19/14	02	ADD NOTE RECOMMENDED LAND PATTERN		J.H
9/11/17	03	UPDATE TO NEW FORMAT		J.H
12/14/20	04	ADD P2 AND DIMENSION TABLE		KC
11/16/21	05	ADD P3		CM

NOTE: REFER TO AGILE FOR OFFICIAL RELEASE



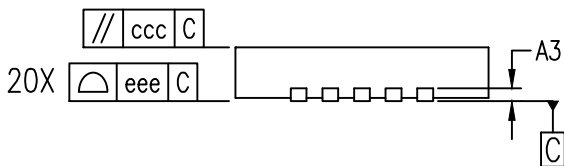
TOP VIEW



BOTTOM VIEW

COMMON DIMENSION

SYMBOL	DIMENSION		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	0.02	0.05
A3	0.20 Ref.		
D	4.00 BSC		
E	4.00 BSC		
D1	SEE EPAD OPTION		
E1	SEE EPAD OPTION		
e	0.50 BSC		
L	SEE EPAD OPTION		
b	0.20	0.25	0.30
N	20		
aaa	SEE EPAD OPTION		
bbb	0.10		
ccc	0.10		
ddd	0.05		
eee	0.08		
fff	0.10		



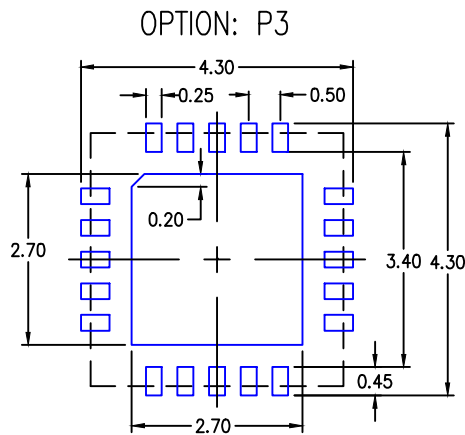
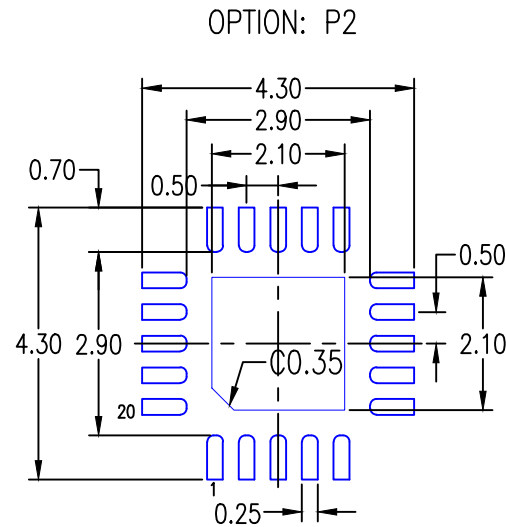
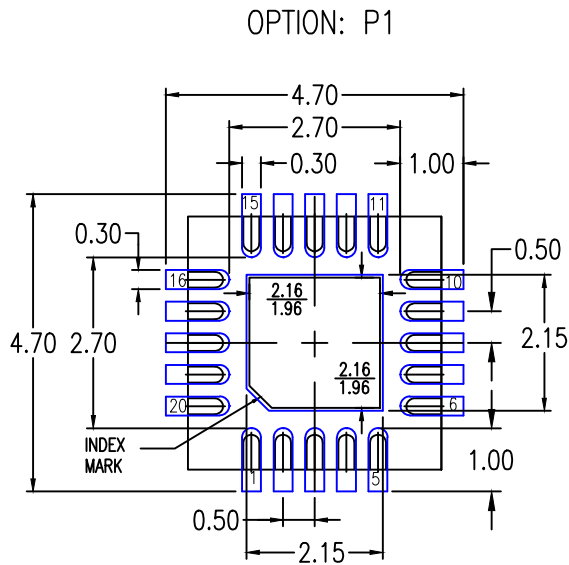
SIDE VIEW

EPAD OPTION

SYMBOL	P1			P2			P3		
	MIN	NOM	MAX	MIN	NOM	MAX	MIN	NOM	MAX
D1	1.96	2.06	2.16	2.00	2.10	2.20	2.60	2.70	2.80
E1	1.96	2.06	2.16	2.00	2.10	2.20	2.60	2.70	2.80
L	0.45	0.55	0.65	0.45	0.55	0.65	0.20	0.30	0.40
aaa	0.15			0.10			0.10		

- NOTE:
1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES
  2. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS  
COPLANARITY SHALL NOT EXCEED 0.06 MM
  3. WARPAGE SHALL NOT EXCEED 0.10
  4. REFER JEDEC MO-220

TOLERANCES UNLESS SPECIFIED DECIMAL ANGULAR XX± ±1° XXX± XXXX±	6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572		
	<b>RENESAS</b> TITLE 20-QFN, Package Outline Drawing 4.0 x 4.0 x 0.75 mm BODY 0.50mm PITCH NCG20		
SIZE C	DRAWING No. PSC-4445	REV 05	DO NOT SCALE DRAWING



RECOMMENDED LAND PATTERN DIMENSION

- NOTE:
1. ALL DIMENSION ARE IN MM. ANGLES IN DEGREES
  2. TOP DOWN VIEW AS VIEWED ON PCB
  3. LAND PATTERN RECOMMENDATION PER IPC-7351B GENERIC REQUIREMENT FOR SURFACE MOUNT DESIGN AND LAND PATTERN

		REVISIONS	
DATE CREATED	REV	DESCRIPTION	AUTHOR
10/09/12	00	INITIAL RELEASE	KS
12/4/13	01	COMBINE POD & LAND PATTERN	J.H
2/19/14	02	ADD NOTE RECOMMENDED LAND PATTERN	J.H
9/11/17	03	UPDATE TO NEW FORMAT	J.H
12/14/20	04	ADD P2 AND DIMENSION TABLE	KC
11/16/21	05	ADD P3	CM
NOTE: REFER TO AGILE FOR OFFICIAL RELEASE			

TOLERANCES UNLESS SPECIFIED		6024 Silver Creek Valley Rd San Jose, CA 95138 PHONE: (408) 284-8200 FAX: (408) 284-3572	
DECIMAL	ANGULAR		
XX±	±1°		
XXX±		TITLE 20-QFN, Package Outline Drawing 4.0 x 4.0 x 0.75 mm BODY 0.50mm PITCH NCG20	
XXXX±		SIZE C	REV 05
		DRAWING No. PSC-4445	
DO NOT SCALE DRAWING			SHEET 2 OF 2

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).