

RAA458100GNP / RAA457100GBM

Register Access Method from Transmitter System
to MCU of Receiver system in operation mode of AT3

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Introduction

This document describes RxMCU register access method from Tx system in AT3.

Target device

RAA457100GBM, RAA458100GNP

Note : The contents of this document are provided as a reference and do not guarantee the operation in the system.
When designing the actual system, thoroughly evaluate the product in the overall system and apply these contents on your own responsibility.

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Related document

The following documents are related to this application note. Also refer to the document when using this application note.

·RAA458100GNP /RAA457100GBM Low Power Wireless Charging System Configuration and Function

Abbreviations and the meanings

The following table shows the abbreviations and the meanings used in this document.

Term	Description
TxIC	Wireless charging system transmitter IC RAA458100GNP.
RxIC	Wireless charging system receiver IC RAA457100GBM.
TxROM, EEPROM	EEPROM in transmitter system.
TxMCU	The device connected to TxIC by 2-wire interface. (mainly microcomputer)
RxMCU	The device connected to RxIC by 2-wire interface. (mainly microcomputer)
Tx system	Wireless charging transmitter system. It is constructed by "TxIC only" or "TxIC and TxMCU" or "TxIC and EEPROM".
Rx system	Wireless charging receiver system. It is constructed by "RxIC only" or "RxIC and RxMCU".
WPT communication	Communication on wireless power transmission carrier signal.
Tx2Rx WPT communication	WPT communication from TxIC to RxIC.
Rx2Tx WPT communication	WPT communication from RxIC to TxIC.
T_Header	The header of Tx2Rx WPT communication packet.
R_Header	The header of Rx2Tx WPT communication packet.
T_0xXX D[X]	Register address and data bit of TxIC. (Example : T_0x02 D[4:1] means that TxIC register address is 0x02, register data bits are D4, D3, D2, D1)
R_0xXX D[X]	Register address and data bit of RxIC. (Example : R_0x10 D[7:5] means that RxIC register address is 0x10, register data bits are D7, D6, D5)

1. Battery charging system configuration and WPT communication packet in ATPC Mode

Table 1.1 shows the battery charging system configuration and pin setting by using TxIC and RxIC in ATPC Mode. In ATPC Mode, WPT communication packets with Header 0x00 to 0x0F are used (There are unused Header in 0x00 to 0x0F). Rx2Tx WPT communication packet is sent by RxIC periodically. Tx2Rx WPT communication is executed to access to RxIC or RxMCU register from Tx system (AT1, AT2, AT3). Table 1.3 shows Rx2Tx WPT communication response packet for Tx2Rx WPT communication packet. Refer to page 9 and page 10 of the related document "RAA458100GNP/RAA457100GBM Low Power Wireless Charging System Configuration and Function" regarding to the packet construction in detail.

Table 1.1 Battery charging system configuration and pin setting in ATPC Mode

Operation mode					TxIC pin setting					RxIC pin setting				
No.	Tx system		Rx system		MS	ATPC	DUTY6	DUTY7	DUTY8	MS	ATPC	ATCHG	ATR	WRC
	Master	Slave	Master	Slave										
ATPC Mode														
AT1	TxIC	TxROM	RxIC	-	H	H	L	L	L	H	H	L	X	L
AT2	TxMCU	TxIC	RxIC	-	L	H	L	L	L	H	H	L	X	L
AT3	TxMCU	TxIC	RxIC	RxMCU	L	H	L	L	L	H	H	L	X	L
AT4	TxMCU	TxIC	RxMCU	RxIC	L	H	L	L	L	L	H	H	X	L

X: Arbitrary value can be selected.

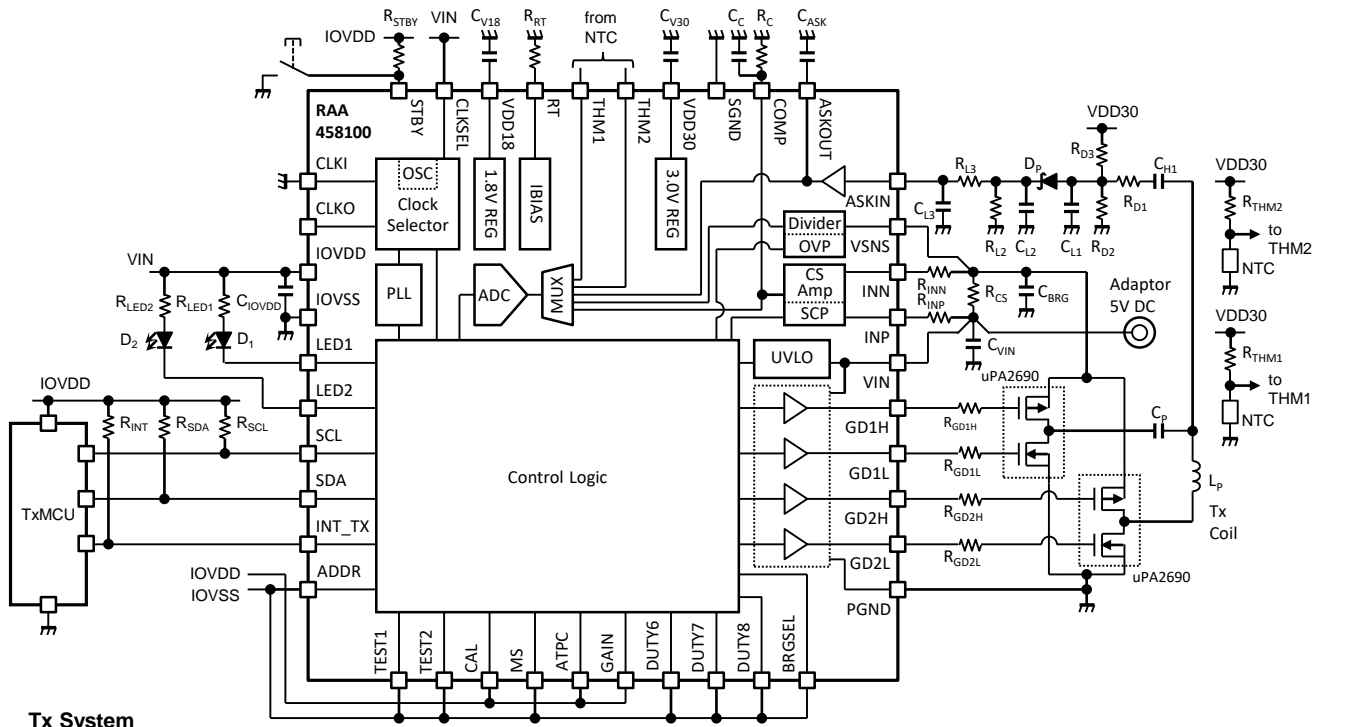
Table 1.2 Header list for each battery charging system in ATPC Mode

Operation mode					Tx2Rx WPT communication Header (T_Header)						Rx2Tx WPT communication Header (R_Header)					
No.	Tx system		Rx system		0x02	0x03	0x04	0x05	0x06	0x10 To 0xFF	0x00	0x01	0x02	0x03	0x04	0x10 To 0xFF
	Master	Slave	Master	Slave												
ATPC Mode																
AT1	TxIC	TxROM	RxIC	-	-	-	O	-	-	-	O	O	O	O	O	-
AT2	TxMCU	TxIC	RxIC	-	O	O	O	-	-	-	O	O	O	O	O	-
AT3	TxMCU	TxIC	RxIC	RxMCU	O	O	O	O	O	-	O	O	O	O	O	-
AT4	TxMCU	TxIC	RxMCU	RxIC	-	-	-	-	-	-	O	O	-	O	O	-

O : Used Header

Table 1.3 Rx2Tx WPT communication response packet (Header) for Tx2Rx WPT communication packet (Header)

ATPC Phase	T_Header	R_Header	Description	
Ping	-	-	TxIC does not receive R_Header 0x01 packet.	
Identification	-	0x01 RxIC ID & Config.	RxIC sends R_Header 0x01 packet to TxIC when RxIC is ready to communicate.	
Configuration or Battery Charge	No Send, 0x00, 0x01, 0x07 to 0x0F	0x03 RxIC Status	When RxIC does not receive Tx2Rx WPT communication packet, RxIC periodically sends R_Header 0x03 and 0x04 packet alternately to TxIC. If the status of RxIC is changed, RxIC sends R_Header 0x03 packet preferentially. If RxIC receives undefined Tx2Rx WPT communication packet (T_Header 0x00, 0x01, 0x07 to 0x0F), RxIC ignores that data. This behavior is the same as no Tx2Rx WPT communication.	
		0x04 Received Power		
		0x02 RxIC Reg. Read Req.	0x02 Response Reg. Read Req.	RxIC replies R_Header 0x02 packet (requested register address data) to TxIC when RxIC receives T_Header 0x02 packet (register read request to RxIC).
		0x03 RxIC Reg. Write Req.	0x03 RxIC Status	RxIC replies R_Header 0x03 packet (RxIC status) to TxIC when RxIC receives T_Header 0x03 packet (register write request to RxIC). When register write is normally executed, Message2 D[0] of R_Header 0x03 packet is set to "1".
		0x04 RxIC Reg. Write & Read Req.	0x02 Response Reg. Read Req.	When RxIC receives T_Header 0x04 packet (register write and read for verification request), RxIC performs register write processing and then replies R_Header 0x02 packet (requested register data) to TxIC.
		0x05 RxMCU Reg. Read Req.	0x02 Response Reg. Read Req.	When RxIC receives T_Header 0x05 packet (register read request from RxMCU), RxIC reads the register data from RxMCU by 2-wire interface and then RxIC replies R_Header 0x02 packet including the data. If communication error occurs in 2-wire interface, RxIC replies R_Header 0x03 packet (RxIC status) to TxIC.
		0x03 RxIC Status		
	0x06 RxMCU Reg. Write Req.	0x03 RxIC Status	When RxIC receives T_Header 0x06 packet (register write request to RxMCU), RxIC writes the register data to RxMCU by 2-wire interface and then RxIC replies R_Header 0x03 packet (RxIC status) to TxIC. When the register write is finished normally, Message2 D[0] of the packet is set to "1". When the communication error is occurred in 2-wire interface, Message2 D[0] of R_Header 0x03 packet is set to "0".	
ALL Phase	-	0x00 End Power Transfer	When RxIC detects particular error, RxIC sends R_Header 0x00 packet to TxIC.	



Tx System

Rx System

*Optional Parts

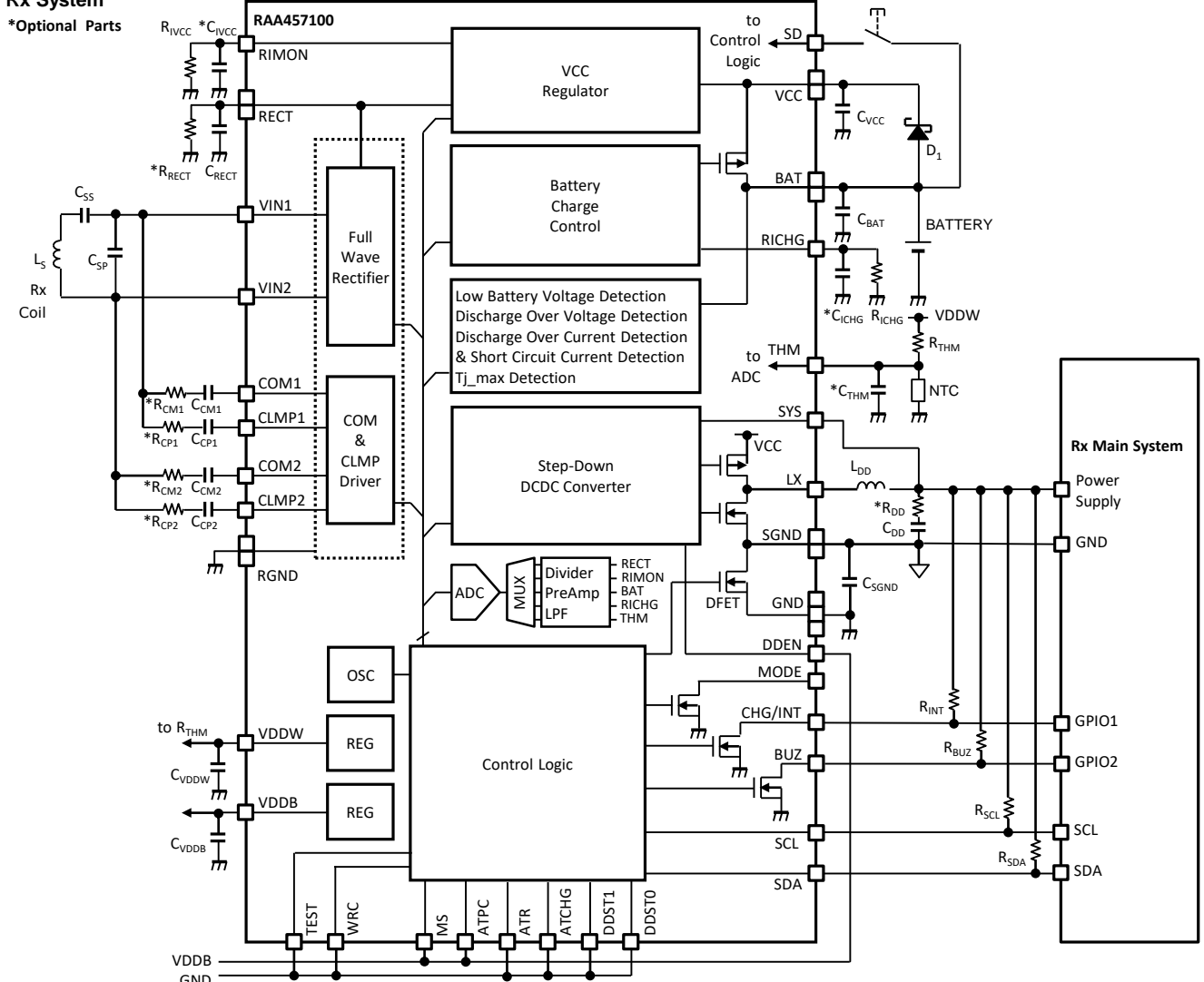


Figure 1.1 Wireless charging system configuration in AT3

2. RxMCU register access method by Tx2Rx WPT communication

2.1 RxMCU register write procedure

Table 2.1 shows RxMCU register write procedure. The DCDC converter of RxIC supplies power to Rx main system in Figure 1.1. RxIC executes the write procedure of RxMCU register when receiving T_Header 0x06 packet by Tx2Rx WPT communication. But there is a possibility that RxIC can't write RxMCU register normally if the DCDC converter of RxIC doesn't work normally. If RxIC has not written the RxMCU register normally, there is a possibility that the write completion flag in R_Header 0x03 packet become 1. Therefore TxMCU should confirm the status of the DCDC converter before writing the RxMCU register. We recommend that Tx system executes writing the RxMCU register after confirming normal operation of the DCDC converter.

Table 2.1 RxMCU register write procedure

No.	Item	Description
1	Setting the slave address of RxMCU for 2-wire serial communication	The slave address of RxMCU for 2-wire interface should be set R_0x0C D[6:0]. After TxMCU sets "Header(T_0x48) / Message1(T_0x49) / Message2(T_0x4A)" = "0x03 or 0x04 / 0x0C / the slave address of RxMCU for 2-wire interface" by 2-wire interface, it sets T_0x0E D[5]=1 (WPT communication start trigger). RxIC receives the packet and writes received data to the specified register. Then, RxIC replies Rx2Tx WPT communication packet (R_Header 0x03 or R_Header 0x02 packet) to TxIC. Once the slave address is set, it is held unless transmitting power stops.
2		After TxIC receives Rx2Tx WPT communication packet and confirms completion of the write processing in RxIC, it outputs low level from INT_TX pin. TxMCU confirms "T_0x1B D[2]=1" (write completion flag in ATPC Mode).
3		TxMCU sets "T_0x1B D[0]=1" for clearing T_0x1B D[2] and INT_TX pin returns to high level.
4	Confirmation of status of the DCDC converter in RxIC	TxMCU confirms the status of DCDC converter in RxIC(R_0x33). After TxMCU sets "Header(T_0x48) / Message1(T_0x49) / Message2(T_0x4A)" = "0x02 / 0x33 / 0x00" by 2-wire interface, it sets T_0x0E D[5]=1 (WPT communication start trigger). RxIC receives the packet and reads data from the specified register. Then, RxIC replies Rx2Tx WPT communication packet (R_Header 0x02 packet) to TxIC.
5		After TxIC receives Rx2Tx WPT communication packet and confirms completion of the read processing in RxIC, it outputs low level from INT_TX pin. TxMCU confirms "T_0x1B D[3]=1" (read completion flag in ATPC Mode).
6		The register data of RxIC is stored in T_0x44 D[7:0]. TxMCU reads data from the register. TxMCU confirms that R_0x33 D[7:4]=4'b0011 and the DCDC converter works normally. If the DCDC converter doesn't work normally, SDA pin and SCL pin voltage are abnormal. Therefore RxIC can't access the RxMCU normally.
7		TxMCU sets "T_0x1B D[0]=1" for clearing T_0x1B D[3] and INT_TX pin output returns to high level.
8	RxMCU register write	After TxMCU sets "Header(T_0x48) / Message1(T_0x49) / Message2(T_0x4A)" = "0x06 / RxMCU register address / RxMCU register data" by 2-wire interface, it sets T_0x0E D[5]=1 (WPT communication start trigger). RxIC receives the packet and writes received data to the specified register of RxMCU. Then, RxIC replies Rx2Tx WPT communication packet (R_Header 0x03 packet) to TxIC.
9		After TxIC receives Rx2Tx WPT communication packet and confirms completion of the write processing in RxIC, it outputs low level from INT_TX pin. TxMCU confirms "T_0x1B D[2]=1" (write completion flag in ATPC Mode).
10		TxMCU sets "T_0x1B D[0]=1" for clearing T_0x1B D[2] and INT_TX pin returns to high level.
11	-	Similarly, TxMCU confirms the status of DCDC converter and executes writing the RxMCU register.
12	Confirmation of status of the DCDC converter in RxIC	TxMCU confirms the status of DCDC converter as above procedure No.4~No.7. If the DCDC converter doesn't work normally, SDA pin and SCL pin voltage are abnormal. Therefore RxIC can't access the RxMCU normally.
13	RxMCU register write	TxMCU sets the RxMCU register address, data and executes Tx2Rx WPT communication as above procedure No.8~No.10.
14	.	.
	.	.
	.	.

2.2 RxMCU register read procedure

Table 2.2 shows RxMCU register read procedure. The DCDC converter of RxIC supplies power to Rx main system in Figure 1.1. RxIC executes the read procedure of RxMCU register when receiving T_Header 0x05 packet by Tx2Rx WPT communication. But there is a possibility that RxIC can't read RxMCU register normally if the DCDC converter of RxIC doesn't work normally. If RxIC has not read the RxMCU register normally, RxIC may determine that it has read RxMCU register normally. Therefore RxIC replies not R_Header 0x03 packet but R_Header 0x02 packet. Therefore TxMCU should confirm the status of DCDC converter before reading the RxMCU register. We recommend that TxMCU executes reading the RxMCU register after confirming normal operation of the DCDC converter.

Table 2.2 RxMCU register read procedure

No.	Item	Description
1	Setting the slave address of RxMCU for 2-wire serial communication	The slave address of RxMCU for 2-wire interface should be set R_0x0C D[6:0]. After TxMCU sets "Header(T_0x48) / Message1(T_0x49) / Message2(T_0x4A)" = "0x03 or 0x04 / 0x0C / the slave address of RxMCU for 2-wire interface" by 2-wire interface, it sets T_0x0E D[5]=1 (WPT communication start trigger). RxIC receives the packet and writes received data to the specified register. Then, RxIC replies Rx2Tx WPT communication packet (R_Header 0x03 or R_Header 0x02 packet) to TxIC. Once the slave address is set, it is held unless transmitting power stops.
2		After TxIC receives Rx2Tx WPT communication packet and confirms completion of the write processing in RxIC, it outputs low level from INT_TX pin. TxMCU confirms "T_0x1B D[2]=1" (write completion flag in ATPC Mode).
3		TxMCU sets "T_0x1B D[0]=1" for clearing T_0x1B D[2] and INT_TX pin returns to high level.
4	Confirmation of status of the DCDC converter in RxIC	TxMCU confirms the status of DCDC converter in RxIC(R_0x33). After TxMCU sets "Header(T_0x48) / Message1(T_0x49) / Message2(T_0x4A)" = "0x02 / 0x33 / 0x00" by 2-wire interface, it sets T_0x0E D[5]=1 (WPT communication start trigger). RxIC receives the packet and reads data from the specified register. Then, RxIC replies Rx2Tx WPT communication packet (R_Header 0x02 packet) to TxIC.
5		After TxIC receives Rx2Tx WPT communication packet and confirms completion of the read processing in RxIC, it outputs low level from INT_TX pin. TxMCU confirms "T_0x1B D[3]=1" (read completion flag in ATPC Mode).
6		The register data of RxIC is stored in T_0x44 D[7:0]. TxMCU reads data from the register. TxMCU confirms that R_0x33 D[7:4]=4'b001 and the DCDC converter works normally. If the DCDC converter doesn't work normally, SDA pin and SCL pin voltage are abnormal. Therefore RxIC can't access the RxMCU normally.
7		TxMCU sets "T_0x1B D[0]=1" for clearing T_0x1B D[3] and INT_TX pin output returns to high level.
8	RxMCU register read	After TxMCU sets "Header(T_0x48) / Message1(T_0x49) / Message2(T_0x4A)" = "0x05 / RxMCU register address / 0x00" by 2-wire interface, it sets T_0x0E D[5]=1 (WPT communication start trigger). RxIC receives the packet and reads data from the specified register of RxMCU. Then, RxIC replies Rx2Tx WPT communication packet (R_Header 0x02 packet) to TxIC.
9		After TxIC receives Rx2Tx WPT communication packet and confirms completion of the read processing in RxIC, it outputs low level from INT_TX pin. TxMCU confirms "T_0x1B D[3]=1" (read completion flag in ATPC Mode).
10		The register data of RxMCU is stored in T_0x44 D[7:0]. TxMCU reads and confirms the data.
11		TxMCU sets "T_0x1B D[0]=1" for clearing T_0x1B D[3] and INT_TX pin returns to high level.
12	-	Similarly, TxMCU confirms the status of DCDC converter and executes reading the RxMCU register.
13	Confirmation of status of the DCDC converter in RxIC	TxMCU confirms the status of DCDC converter as above procedure No.4~No.7. If the DCDC converter doesn't work normally, SDA pin and SCL pin voltage are abnormal. Therefore RxIC can't access the RxMCU normally.
14	RxMCU register read	TxMCU sets the RxMCU register address and executes Tx2Rx WPT communication as above procedure No.8~No.11.
15	.	.
	.	.
	.	.

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