D2 Audio DSP

Writing to EEPROM or SPI Flash Memories In D2 Audio Systems Using an External Microcontroller

Abstract

This application note describes how to write a firmware or parameter data image to an I^{2}C EEPROM or SPI Flash NVM memory as used with the D2 Audio family of sound processors, using an external system microcontroller.

Contents

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1. Overview

D2-1, D2-4/4P, and D2-3/6/3S Digital Audio Processor devices typically use an external Non-Volatile Memory (NVM) for storing firmware and/or parameter setting data. This memory is used interactively with the D2 Audio device during normal operating conditions, where the D2 Audio device's interface has direct control of read and write to that memory.

2. Hardware Connections Required

The hardware interface between the D2 Audio device and the external controller include:

- nRESET - D2 Audio reset bus
- SCL - D2 Audio I^2C bus 2-wire bit clock
- SDA - D2 Audio I^2C bus 2-wire data
- Boot mode - Logic high/low signal from controller, tied to the IRQx pins of the D2 Audio, establishes the D2 Audio's Boot mode during the booting and update process.

Note: These signals are present on the "SCAMP" connector header on the D2 Audio evaluation kit demo boards.

3. D2 Audio Device Firmware Images and Booting

Firmware source and booting operation is similar for all D2 Audio devices but is slightly different for each family of devices.

3.1 D2-4, D2-4P

- Firmware and default parameter data is embedded within the D2-4/4P device. All operation is controlled by that internal firmware and there is no provision for operating these devices from an external memory with external firmware.
- For these D2 Audio devices, an on-board external NVM can be used for storing parameter settings and providing register initialization data to override some default on-chip settings. This provides storage capability, register parameter, and setting data only and does not support alternate firmware.
- The Boot mode of these devices, established by the Boot mode pin's logic levels, defines whether the D2-4/4P loads external data from an external I^2C EEPROM operating as an I^2C slave from the D2 Audio, or as an I^2C slave receiving its boot data from an external controller operating as an I^2C master.
- The D2-4/4P supports writing and saving data only to an I^2C EEPROM. It also includes only one I^2C port that is shared between the D2 Audio control interface and the EEPROM. Booting is supported by using two different I^2C addresses.

3.2 D2-1, D2-3, D2-3S, D2-6

- Firmware and parameter data all originate from an external NVM or external controller. D2 Audio device operation is totally dependent on that memory's (or controller's) firmware content and the D2 Audio holds its operating firmware and data only within its on-chip RAM memory.
- The Boot mode of these devices, established by the Boot mode pin's logic levels, defines where the device obtains its operational firmware and parameter image upon startup. In typical system applications, that image comes from an external NVM operating as a slave to the D2 Audio master, or from an external controller where the D2 Audio is a slave through the D2 Audio device's I^2C control interface.
- For stand-alone operation, firmware and startup parameter data is held on an external NVM. Upon booting, the D2 Audio receives its firmware from that NVM. However, after the system is running after boot, an external controller can still control parameter settings through the I^2C control interface, writing to the active parameter data registers within the D2 Audio. It can also initiate commands to write present-session parameter settings to the on-board NVM, such as saving last user volume settings during power-off.

- Firmware and parameter data can also be provided directly from an external controller, not requiring an on-board NVM. This is the method used by the D2 Audio Customization GUI v3 software as it builds and loads a firmware image into the target D2 Audio hardware. This is also the method that initiates the process of configuring the D2 Audio device to begin writing its on-board NVM with data being provided through the I^{2}C control bus from that external controller.
- When system control is provided from an external microcontroller or host, that controller has direct access to only the D2 Audio device, where the D2 Audio device alone manages read/write control and writing of host data to the memory.
- The D2-3, D2-3S, and D2-6 support saving and writing firmware data to an SPI Flash memory and to an I^{2}C EEPROM while the D2-1 supports only an I^{2}C EEPROM.

4. Writing to EEPROM in D2-4/4P Designs

Writing to the EEPROM in D2-4/4P designs involves four basic steps:

1. Booting the D2-4/4P from the external controller, which includes writing of parameter and register setting data into the RAM of the D2 device.
2. If audio parameter setting changes are required to the defaults contained within this initial booting, those changes are written to their respective audio processing parameter registers.
3. After the D2 contains the register data and optionally any further audio parameter setting changes, issue a command from the controller to initiate the D2 to write its setting data to the EEPROM.
4. Resetting and re-booting the D2 Audio, this time booting from its I^{2}C EEPROM instead of the controller.

Booting from the external controller involves setting the Boot mode of the D2 Audio to operate as an I^{2}C slave, under control of the controller that is operating as an I^{2}C master.

The specific Boot mode of the D2-4/D2-4P devices is assigned based on the state of the IRQB and IRQA input pins at the time of reset deassertion. These two pins are each connected to a logic high or low state on the hardware with pull-up or pull-down electrical connections. Tying both of the IRQB and IRQA pins to ground enables the I^{2}C Slave (Boot Mode 0) operation.

The boot code for incorporating into the microcontroller is supplied by the D2 Audio DSP as a "[bootcode].hex" hex data file. It is provided in this form so that it can be directly copied into the microcontroller's own system code.

This boot code contains the initialization data only for startup of the D2 Audio devices. It does not contain audio processing parameter data that is assumed to be incorporated as normal operation of the microcontroller amplifier system operation. See Step 2 above regarding optionally changing settings.

The Boot operation is identical for the D2-4 and D2-4P devices. However, each of these has their own specific boot hex data.

4.1 Steps to Write for D2-4/4P

1. Configure the IRQA and IRQB device pins of the D2-4/4P. Typically, IRQB is tied low for a constant logic low level.
2. IRQA must be controlled by the external controller. During the initial boot process for loading the [bootcode].hex data file, IRQA must be pulled low by the controller. This causes the D2 Audio to boot as an I^{2}C slave receiving its boot data from an external controller operating as an I^{2}C master.
3. Upon system startup, the microcontroller initiates a reset of the D2 Audio device by asserting the nRESET pin.
4. Upon deassertion of reset, the microcontroller delays any additional I^{2}C communication to the D2 Audio device for approximately 200ms.
5. After this delay, the microcontroller outputs the data from the [bootcode].hex file, using address 0x88. This writes that boot code data to the registers within the D2 Audio (**Note**: Address 0x88 is used for boot operation only).

6. If additional audio parameter setting changes are required, they are now written to the D2 Audio's registers from the controller (**Note**: Address 0x88 is used for boot operation only). After boot is completed, further communication from the controller uses I^{2}C address 0xB2. This 0xB2 address is required for writing these additional parameters.
7. Now that the D2 Audio contains the final required setting image, it is written to the EEPROM. This is done by issuing a command from the controller to write (hex) 0x000000 to D2 Audio memory address 0x800000, using the I^{2}C address of 0xB2.
8. After completion of this write to EEPROM sequence, the controller again asserts nRESET to reset the D2 Audio device. It also must release its pull of IRQA low, allowing IRQA to become a logic high level.
9. Upon deassertion of nRESET, and with IRQA high, the D2 Audio now boots directly from the EEPROM, using its new data.

5. Writing to NVM in D2-1/3/3S/6 Designs

Writing to NVM in designs using D2-1, D2-3, D2-3S, or D2-6 involve additional steps beyond those for the D2-4/4P. In these device families, all firmware, in addition to setting parameter data, resides on the external NVM. Also, these D2 Audio devices use one I^{2}C port for external interface control, and another control port for connecting to the on-board NVM (on D2-1, the second NVM port is implemented using the GPIO6 and GPIO7 pins, and does not have pins with SDA or SCL names for this second port).

The external microcontroller or host has direct access to only the D2 Audio device through its external-interface I^{2}C port. Therefore, the D2 Audio device manages all read/write control and writing of host data to the memory.

In these D2 Audio designs, a special bootloader image first loads into the D2 Audio, where it becomes the operating firmware that performs the write-to-NVM function. Because the D2-1 uses only an I^{2}C EEPROM, and the D2-3/3S/6 use (typically) an SPI Flash, the bootloader image is different. But the process that follows is the same.

For these D2 Audio devices, it is assumed that audio parameter and setting data has previously been saved and exists within the final firmware hex image.

- That image is easily created using the D2 Audio Customization GUI v3 program.

Similar to the basic steps used with D2-4/4P designs, the process involves these basic steps:

1. Booting the D2 Audio from the external controller, which includes writing of the bootloader hex image into the RAM of the D2 Audio device. This image becomes the temporary execution code for the remaining process.
2. Using this operating bootloader in the D2 Audio, the system controller initiates a write sequence to the D2 Audio and references the firmware image hex file that is written to the D2 Audio board's NVM.
3. Upon completion of the update process, reboot the D2 Audio, this time booting from the on-board NVM.

5.1 Steps to Write for D2-1/3/3S/6

1. Configure the IRQA, B, C, D device pins of the D2 Audio devices. Boot modes for D2-3/3S/6 are IRQ[D:A] = 0000 for booting from an external controller, 0010 for booting from an SPI Flash (D2-3/3S/6 only), and 0001 for booting from an I^{2}C EEPROM (D2-1).
2. The IRQ[D:A] pins must be controlled by the external microcontroller. During the initial boot process for loading the [boootloader].hex data file, IRQ[D:A] must be set to 0000. This causes the D2 Audio to boot as an I^{2}C slave receiving its boot data from an external controller operating as an I^{2}C master.
3. Upon startup, the microcontroller initiates a reset of the D2 Audio device by asserting the nRESET pin.
4. Upon deassertion of reset, the microcontroller delays any additional I^{2}C communication to the D2 Audio device for approximately 200ms.

5. After this delay, the microcontroller outputs the data from the [bootloader].hex file, using address 0x88. This writes the bootloader firmware image into the RAM of the D2 Audio.
   a. The [bootloader].hex file is different depending upon whether the target NVM is EEPROM or SPI Flash. Ensure the correct file is used per the target NVM type.
6. Now that the D2 Audio contains the execution code to write to its NVM, the system controller initiates the write to NVM by writing the system firmware image hex file, using the I^2C address 0xB2.
7. After completion of this write to EEPROM sequence, waiting approximately 200ms, the controller asserts nRESET to reset the D2 Audio device. It also must release its pull of the IRQ pins low, allowing the respective IRQ pin to become a logic high level.
   a. For use with an I^2C EEPROM (D2-1) IRQ[D:A] = 0001
   b. For use with an SPI Flash (D2-3/3S/6) IRQ[D:A] = 0010
8. Upon deassertion of nRESET, and with IRQ[D:A] set to the NVM type, the D2 Audio now boots directly from that NVM using its new firmware and data.

6. Revision History

Rev.	Date	Description
1.00	May.24.19	Initial release

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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