# Single-Channel Breathing Example
# SLG47910

## Abstract

This application shows how to build a single channel breathing example using SLG47910 FPGA to control LED.

This application note comes complete with a design file which can be found in the References Section

## Contents



## 1. Terms and Definitions

| | |
|---|---|
| FPGA | Field Programmable Gate Array |
| FPGA Editor | Main FPGA design and simulation window |
| Go Configure Software Hub | Main window for device selection |
| ForgeFPGA Window | Main FPGA project window for debug and IO programming |

## 2. References

For related documents and software, please visit:

ForgeFPGA Low-density FPGAs | Renesas

Download our free ForgeFPGA™ Designer software [1] to open the .ffpga design files [2] and view the proposed circuit design.

[1] Go Configure Software Hub, Software Download and User Guide

[2] AN-FG-005 Single-Channel Breathing Example.ffpga, ForgeFPGA Design File

[3] SLG47910, Preliminary Datasheet

# 3. Introduction

Breathing control is a method of slowly fading an LED ON and OFF. This application shows how to build a single channel breathing examples using the SLG47910 ForgeFPGA to control LEDs. This design has a single Pulse Modulated (PWM) channel that drives the LED at 50 Hz. The top-level Verilog code has one instance of breathing module from the list of IP Blocks in the ForgeFPGA Workshop.

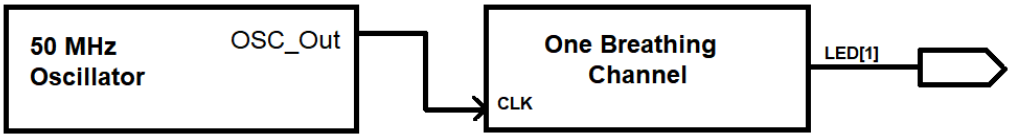



**Figure 1: Single Channel Breathing Application**

The following parameters can be set to program the breathing module.

| Name | Range | Default Value | Description |
|---|---|---|---|
| IN_CLK_HZ | 100MHz – 1MHz | 50MHz | Input Frequency |
| DEPTH | 16 - 2 | 8 | It's the depth value of the output PWM counter, defined in bits |
| PWM_FREQ_HZ | 100K - 2 | 100 | It's the output PWM frequency value, defined in Hz |
| RAMP_MULT | 256 - 1 | 2 | It's the value of the ramp multiplier counter, defined in decimal value |

For calculating breathing period time in Milli-seconds use the formula below:

**PERIOD = (2 * ((2 ^ DEPTH) - 1) * RAMP_MULT) / PWM_FREQ_HZ:**

The following signal names are the PINs that are used in the design.

- clk - input clock signal
- nreset - input negative reset signal
- en - input enable signal
- led[1] - output PWM signal

Using the ForgeFPGA Workshop software, the Verilog code was synthesized, and the bit stream was loaded on to the SLG47910 device. The design uses the internal oscillator as a clocking source for the application. The functional waveforms below (see Figure 2) show single channel that have different frequencies and pulse modulation. This channel drives an LED and turns it ON and OFF with a fading effect. A done signal is flagged as the LED has been through its fluctuations.

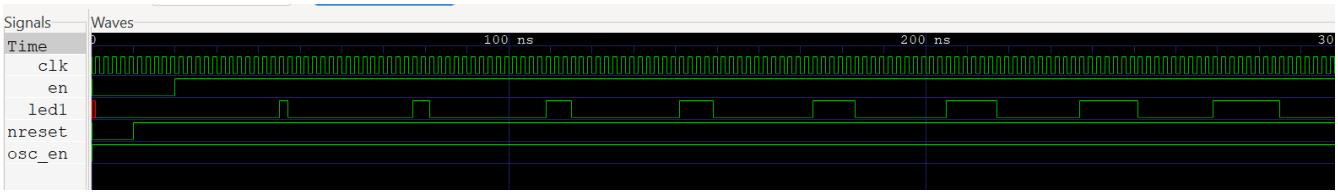



**Figure 2: Single channel Breathing Functional Waveform**

# 4. Ingredients

- ForgeFPGA Device SLG47910V
- ForgeFPGA Development Board with USB cable and power supply
- ForgeFPGA Socket Adaptor Board
- Latest Revision of ForgeFPGA Workshop software
- DIGILENT eight-LED Pmod board (PMOD8LD)

# 5. Single Channel Breathing Verilog Code

Shown below is the (*top*) module named DemoSequentialBreathing. It consists of a single placement of the "breathing" module which is based on the "breathing controller" IP Block. The Verilog Code for the Breathing IP block can be found in the complete design example. It is available for download (AN_FG_007 Single Channel Breathing Example.ffpga)

```
(* top *) module DemoSequentialBreathing #(
  parameter IN_CLK_HZ = 50000000,// 4.45MHz
  parameter DEPTH = 8
) (
  (* iopad_external_pin *) input nreset,
  (* iopad_external_pin, clkbuf_inhibit *) input clk,
  (* iopad_external_pin *) output osc_en,
  (* iopad_external_pin *) output led1_oe,
  (* iopad_external_pin *) output led1);

  // OSC config
  assign osc_en = 1'b1;

  //OE
  assign led1_oe = 1;

  wire done;
  wire next;
  assign next = done;

  reg [1:0] seq_counter;

  always @(posedge clk) begin
    if (!nreset)
      seq_counter <= 'h0;
    else if (next)
      seq_counter <= seq_counter + 1;
  end

  wire  en;
  assign en = (seq_counter == 0) ? 1 : 0;

  breathing #(
    IN_CLK_HZ,
    DEPTH,
    50, // Output PWM = 50 Hz
    1
  ) breathing_led1 (
    .clk (clk),
    .nreset (nreset),
    .en (en),
```

```
    .out (led1),
    .done (done)
  );

endmodule
```

# 6. Floorplan: CLB Utilization

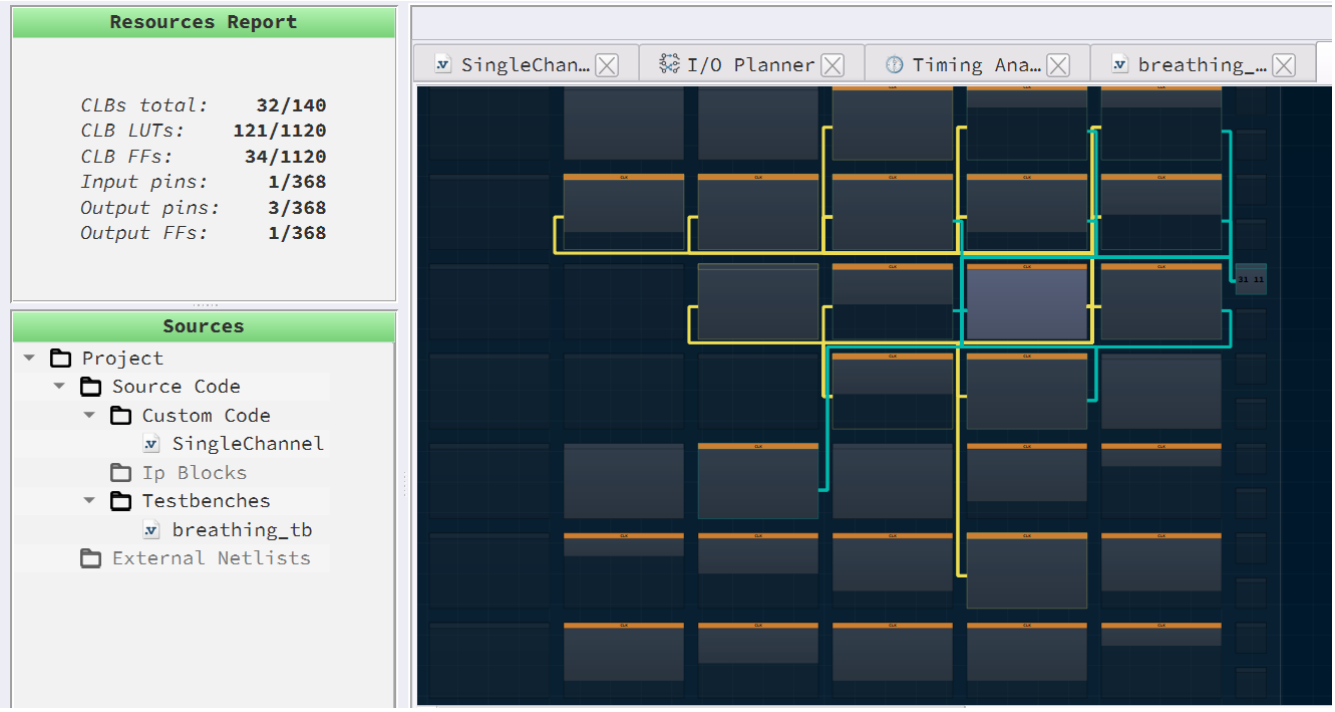



**Figure 3: Single Channel Breathing CLB Utilization**

The Floor planner tab in the FPGA Editor shows the placement of CLBs and FFs (Figure 3). The resource utilization is shown in the top left corner.

# 7. Design Steps

1. Launch the latest version of the Go Configure Software Hub. Select the SLG47910V device and the ForgeFPGA Workshop software will load.
2. Download the design example Single-Channel Breathing Example.ffpga. If you are not familiar with the ForgeFPGA Workshop software, review the Four-Bit Counter application notes that cover the basic design steps.
3. Open the Single-Channel Breathing Example.ffpga file after downloading.
4. Open the FPGA editor and review the Verilog code.
5. Open the IO planner tab on the FPGA editor and review the pin assignment.
6. Next click on the Synthesize button on the lower left side of the FPGA editor. Select the Generate Bitstream button on the lower left side of the FPGA editor. Check the Logger and Issues tabs to make sure that the bit steam was generated correctly.
7. Now click on the Floorplan tab and see the CLB utilization (Figure 3). Press the Ctrl and the mouse wheel to zoom-in or the icons on the bottom to zoom in/out. Confirm that the IOs selected in the IO Planner are shown in the floorplan.

8. Close the FPGA Editor and go to the ForgeFPGA Workshop widow (Figure 4). Selecting the Debug tab will enable the debug controls. Double click on the VDD pin and set VDD = 1.2v. Then double click on VDDIO pin and set VDDIO = 2.0v.
9. Double click on nSLEEP and nRST and select Force On. This ensures that all blocks are powered up.
10. The single channel breathing design is now ready to load onto the FPGA using the development board. Connect the development board to the adapter board. Connect the eight-LED PMOD board to the adapter board. Use PMODA connector on the adaptor board (Figure 5). Connect the USB and power supply to the development board.

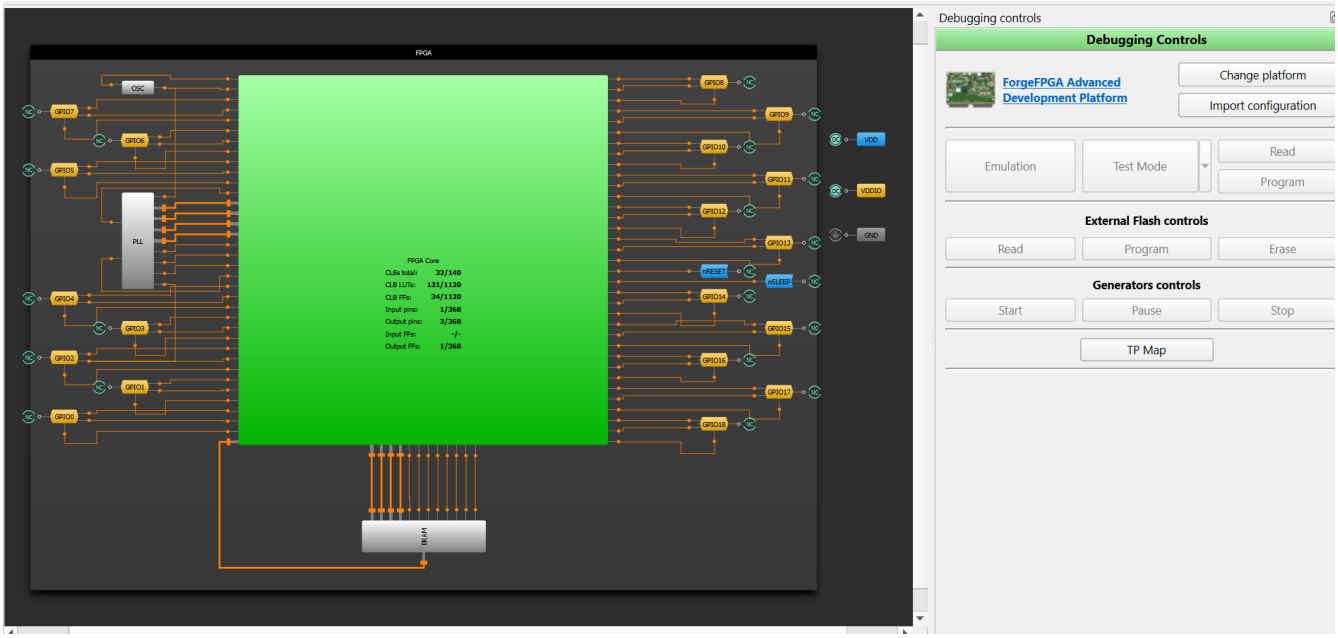
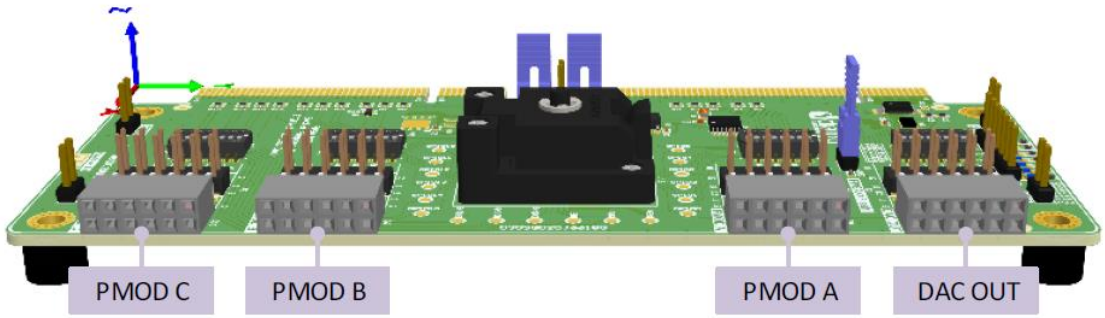



**Figure 4: ForgeFPGA Debug Window**

11. In the ForgeFPGA Workshop window, select Change platform on the Debugging Controls tab. Choose the ForgeFPGA Development Platform then select Emulation.

Now the design is loaded onto the FPGA device. GPIO0 will have the output of the FPGA. GPIO0 drives the LED4 on the Pmod board. The LEDs will be fading on and off.




Pin Numbering. View from the connector connection side (PCB, right view)

| | | | | | |
|---|---|---|---|---|---|
| 11 | 9 | 7 | 5 | 3 | 1 |
| 12 | 10 | 8 | 6 | 4 | 2 |

**Figure 5: ForgeFPGA Socket Adaptor**

# 8. Conclusions

This application note shows how the SLG47910 can be used to control a complicated sequencing of LEDs. This testcase is available for download (AN-FG-005 Single-Channel Breathing Example.ffpga). If interested, please contact the ForgeFPGA Business Support Team.

# 9. Revision History

| Revision | Date | Description |
|---|---|---|
| 1.0 | 21-Feb-2022 | Initial Version |
| 2.0 | 28-Dec-2023 | Updated the design file and AN according to BB revision |

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