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A New PSPICE Subcircuit for the Power MOSFET Featuring Global Temperature Options

Abstract

An empirical sub-circuit was implemented in PSPICE® and is presented. It accurately portrays the vertical DMOS power MOSFET electrical and, for the first time, thermal responses. Excellent agreement is demonstrated between measured and modeled responses including first and third quadrant MOSFET and gate charge behavior, body diode effects, breakdown voltage at high and low currents, gate equivalent series resistance, and package inductances for temperatures between -55^{o}C and 175^{o}C. Parameter extraction is relatively straightforward as described.

Introduction

Circuit simulation commonly uses one of the SPICE [1] programs. However, power circuits require proper models for unique devices which are not included in the supplied libraries. Efforts have been published to model the power MOSFET [2-10] with varying degrees of success. The more successful papers have used sub-circuit representation. To date, a thermal model has not been offered.

Objective

It is the goal of this effort to provide for the first time a thermal sub-circuit model capable of providing accurate simulation throughout all of the power MOSFET regimes. In addition, the sub-circuit should be readily understood and accepted by users, and the ease of parameter extraction should be demonstrated.

Method

A sub-circuit approach is employed which is empirical. It is developed to provide black box conformity to the power MOSFET throughout the operating regime normally traversed by the dictates of most power circuit applications, including junction temperature. Although device thermal behavior is the driving force, respect is maintained toward the physics and the SPICE algorithms.

The developed sub-circuit schematic is shown in Figure 1.

There are many forms of SPICE, each with its own strengths and weaknesses. PSPICE was chosen for the following reasons.

1. An evaluation copy capable of considerable circuit analysis for power circuits is available.
2. The PROBE feature provides excellent displays.
3. Programmed time slice defaults and DC convergence routines make it very friendly.
4. The switch algorithm of PSPICE provides a very smooth transition from off to on.

Other forms of SPICE were not investigated, but they should be amenable to the development of a similar sub-circuit by paralleling the teachings of this work.

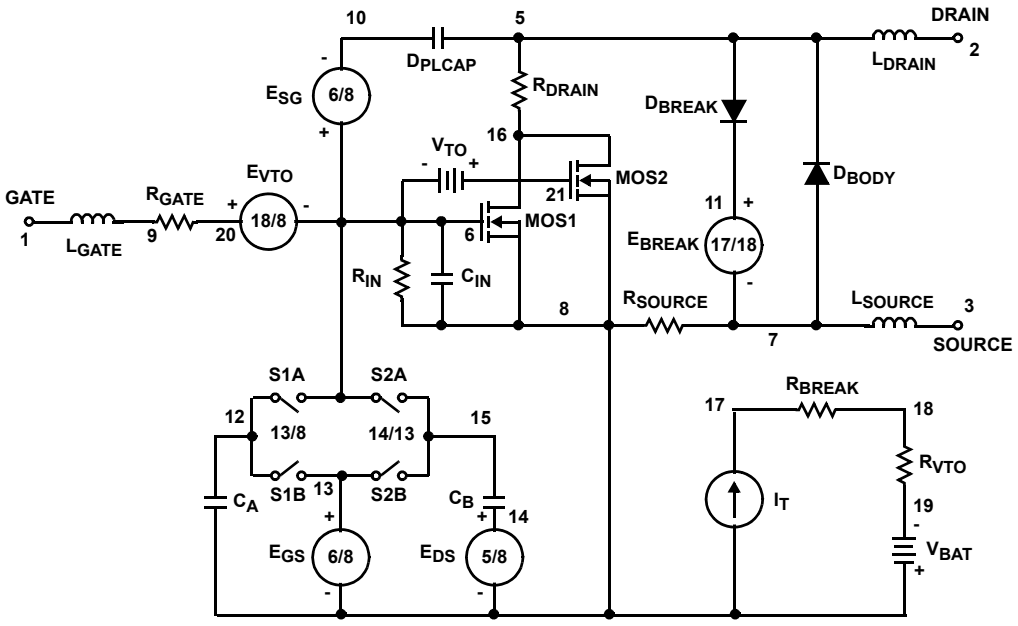

FIGURE 1. PSPICE MODEL SUBCIRCUIT

Driving constraints for this work were:

5. The SPICE device equations should not be modified.
6. Global temperature should be included.
7. All modes and levels of power MOSFET operation should be modeled.
8. The sub-circuit should be empirically developed to complement the device physics and the source code algorithms.
9. The sub-circuit should be acceptable to a circuit design user.
10. Parameter extraction should require little or no iteration.

Temperature Modeling

Use is made of voltage controlled voltage sources and model statements in order to form master/slave circuit relationships. In this manner, resistors can often be used to establish a first and second order temperature correction where direct PSpice algorithms will not permit thermal modeling.

An Overview (Figure 1)

The primary device for gate controlled positive or negative current flow is provided by Mos1 which is defined by the level 1 model MOSMOD. The second order effect of threshold voltage is set by Mos2 combined with the voltage V_{TO}. Model MOSMOD also defines Mos2 but with a 1 percent scaling.

It is necessary that R_{SOURCE} and R_{DRAIN} be provided as separate resistors, rather than being included with the MOSFETs. In this manner, 1st and 2nd order temperature effects may be added as described by model RDSMOD.

The thermal variation of KP as provided by the source code is a satisfactory representation. However, the threshold voltage of Mos1 must be modified by the voltage dependent voltage source E_{VTO}. E_{VTO} provides an additive or subtractive voltage in series with the gate as a function of temperature. It is equal to the sum of V_{BAT} and the product of It and R_{VTO}. Temperature variation is provided by model RVTOMOD.

Avalanche breakdown of the MOSFET is provided by the clamp circuit of D_{BREAK} in series with E_{BREAK}. The value of E_{BREAK} is provided by the multiplier of E_{BREAK} and the product of It times R_{BREAK}. Temperature variation is provided by model RBKMOD. High current voltage drops are provided by RS of the model DBKMOD including thermal sensitivity.

The power MOSFET being modeled contains a third quadrant diode as a fabrication consequence, and it is represented by D_{BODY}. Model DBDMOD provides the leakage current IS, the transit time for stored charge effects TT, the body diode series resistance RS, temperature dependence of this resistor TRS1 and TRS2, and the MOSFET output capacitance CJO.

The inductances associated with the device terminals are represented by L_{SOURCE}, L_{GATE}, and L_{DRAIN}.

The effective series resistance associated with the gate is modeled by the resistor R_{GATE}.

A gate to source input capacitance is represented by C_{IN}. MOSFET output capacitance is provided by model DBDMOD as described above. Feedback capacitance is provided by D_{PLCAP} as defined by model DPLCAPMOD. A diode was used for this function to provide a square root dependency with drain to source voltage. The voltage dependent voltage generator E_{SG} is added to assure that the drain to source voltage is imposed across the feedback capacitor while forcing the feedback current flow into the gate node. It is further necessary that the ideality factor N of model DPLCAPMOD be made large to exclude forward diode conduction during third quadrant operation of the MOSFET.

A capacitor C_A is switched in parallel with C_{IN} when the gate to source voltage becomes sufficiently negative. This switching is implemented by the switch S1A. Model S1AMOD defines the switch closed resistance, open resistance, and the gate to source voltages through which the fully on to fully off transition occurs. During this transition, switch S1B also transitions from fully off to fully on. Switch S1B is defined by model S1BMOD. Voltage controlled voltage generator E_{GS} provides the proper charge state for C_A when switch S1A is open.

In a similar manner, the capacitor C_B is switched in parallel with C_{IN} when the drain to gate voltage becomes negative. Switch S2A is defined by model S2AMOD for the on resistance, off resistance, and drain to gate voltage transition range. During this transition, switch S2B also transitions as defined by model S2BMOD. Voltage controlled voltage generators E_{DS} and E_{GS} provide the proper charge state for C_B when switch S2A is open.

In order to facilitate DC convergence, PSPICE provides a minimum conductance between all nodes as defined by the PSPICE analysis options. In order to assure that a floating gate initial condition will not exist should a modeler drive from a current source, a very large gate to source resistor R_{IN} is added. Inclusion of R_{IN} is recommended but not required.

All sub-circuit elements are treated as being independent of temperature if they are not otherwise defined.

Gate propagation effects [15], radiation effects, and inherent VDMOS design deficiencies are not modeled. This is discussed later.

All discussions apply equally to the P channel, although the N channel is discussed exclusively.

Applications

The sub-circuit combined with external circuitry may be analyzed for responses. Three circuits are modeled to demonstrate the capability of the PSPICE sub-circuit model. A synchronous rectifier producing 100W at 5VDC from a 100KHz square wave demonstrates the ability to handle the first and third quadrant regimes of two MOSFETs, including conversion efficiency versus temperature. Calculated waveforms are presented, but they are unsupported by measured data. The diode recovery waveform is modeled and compared to the measured response. Switching waveforms of the power MOSFET are also modeled and are compared to the measured results.

SYNCHRONOUS RECTIFIER

The schematic of a synchronous rectifier circuit is shown in Figure 2. The rectifier power MOSFETs are a pair of

cross coupled RFH75N05 megaFET devices. Conduction is offered by a forward gate bias with negative drain current (third quadrant mosfet operation) and voltage blocking is assured by a slightly negative gate bias for first quadrant MOSFET operation.

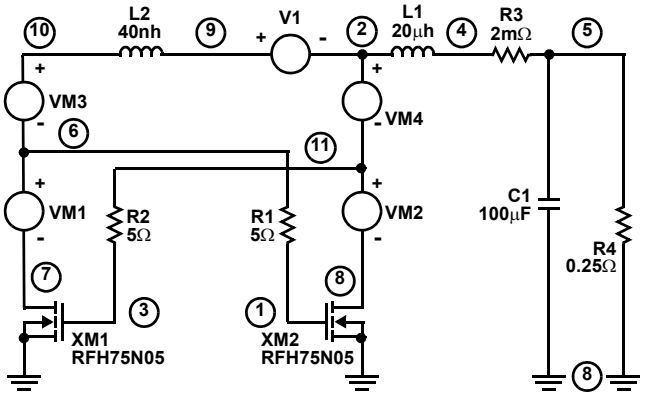

FIGURE 2. SYNCHRONOUS RECTIFIER CIRCUIT

VM1 to VM4 are voltage sources of zero potential and are used to permit a recording of branch currents. The transformer secondary normally used in a supply of this sort is represented by voltage source V1 and leakage inductance L2. Filter inductor L1 and capacitor C1 provide energy storage and smoothing for the 100KHz square wave of V1. Rise and fall times of the square wave are not critical, but were set at 40ns. Gate coupling resistors R1 and R2 are somewhat critical, in that too high a value will restrict the conduction transition time of the MOSFET. Alternatively, a value too low will permit a high voltage drain spike to appear on the gate of the MOSFET.

The calculated output voltage turn on transient is shown in Figure 3. Of course this represents a feed forward circuit response only. In practice, the modeled drive circuit with pulse width modulation and feedback would provide a much faster response which would be slew rate limited. The ripple voltage is 5mV RMS.

The efficiency for this portion of the synchronous rectifier circuit is plotted in Figure 4 as a function of temperature from -25^{O}C to 150^{O}C. As a convenience, the equation used by PROBE (PSPICE's waveform plotter routine) is included. This equation yields a solution rapidly.

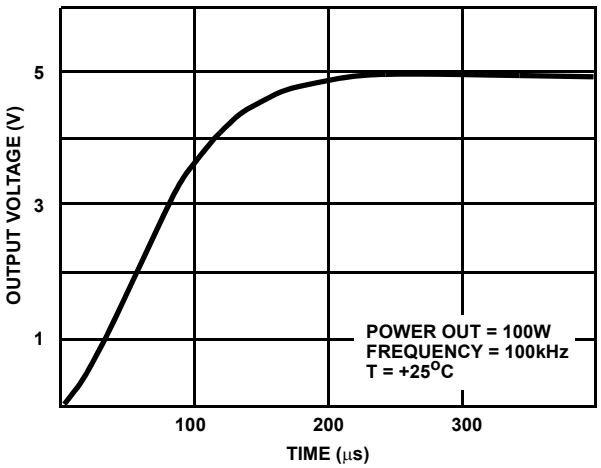

FIGURE 3. RECTIFIER OUTPUT VOLTAGE

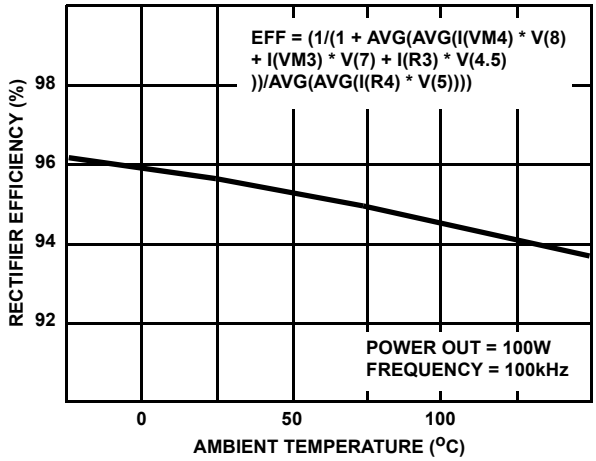

FIGURE 4. RECTIFIER EFFICIENCY

Transition voltage waveforms of the input voltage, one drain voltage, and one gate voltage are plotted in Figure 5. The value of drain voltage during third quadrant conduction is approximately -0.2 volts. Other waveforms are readily available by use of the PSPICE system.

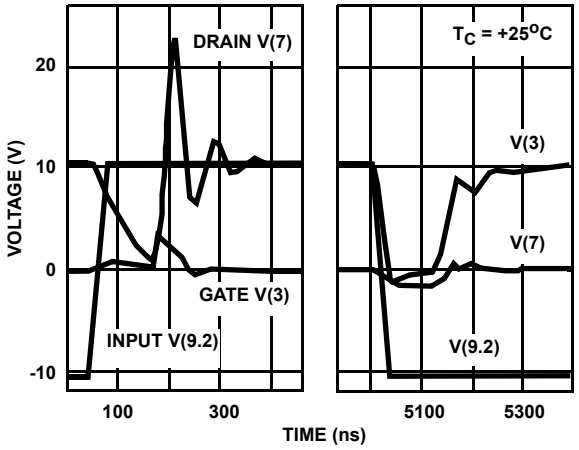

FIGURE 5. TRANSITION VOLTAGE WAVEFORMS

RECOVERY WAVEFORMS

Figure 6 shows the MOSFET current of the parasitic 3rd quadrant diode vs time as modeled with the sub-circuit and as measured using the Berman SM30 equipment. Measurements show very little temperature sensitivity. Therefore it is not modeled.

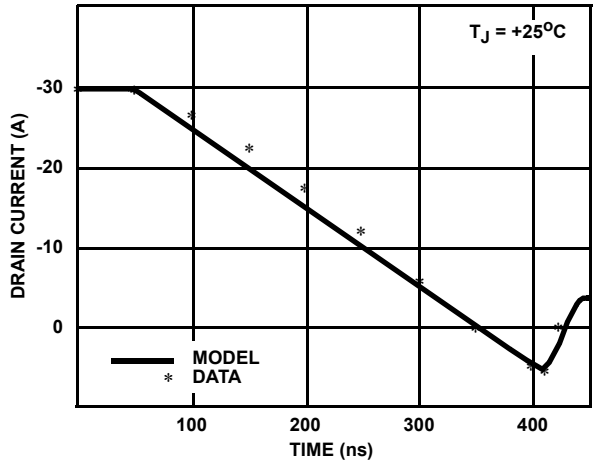

FIGURE 6. DIODE RECOVERY WAVEFORMS

SWITCHING WAVEFORMS

Switching time measurements of the power MOSFET are usually taken in a circuit similar to that of Figure 7. Although parasitic wiring inductance is not normally shown, it exists and is modeled as shown. The waveforms of gate and drain voltages are presented as measured and modeled in Figure 8. Switching times of Figure 8 are listed in Table 1.

TABLE 1. SWITCHING TIME DATA

PARAMETER	DATA	MODEL	UNITS
Turn on Delay Time	72	67	ns
Rise time	238	208	ns
Turn Off Delay Time	440	460	ns
Fall Time	259	240	ns

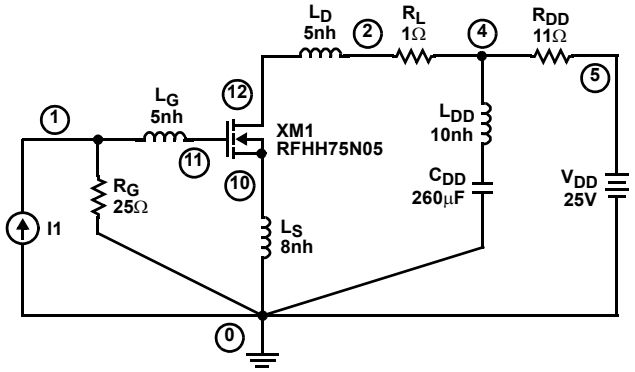

FIGURE 7. SWITCHING TIME CIRCUIT

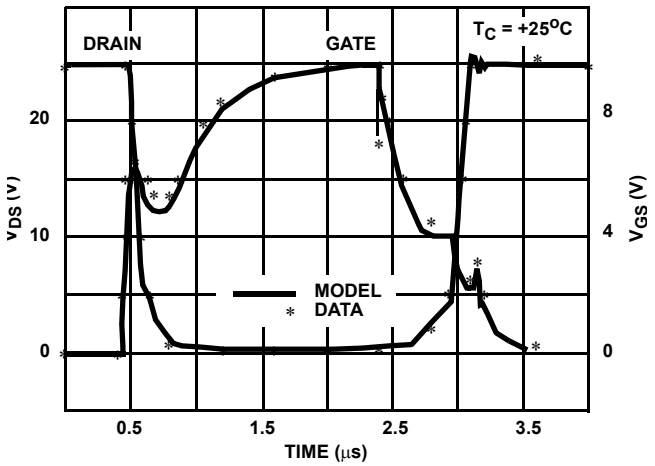

FIGURE 8. SWITCHING TIME WAVEFORMS

Measured vs Modelled Characteristics

The device characteristics have been measured (data points) and modeled (solid line) as plotted in Figures 9 to 19. Thermal responses were omitted from some figures to improve the clarity of presentation.

Discussion Of Results

Excellent correlation generally exists between measured and modeled information over the current range from zero to three times the device rated current. As the drain voltage is increased from zero volts with a constant gate voltage, the MOSFET transitions from the linear mode to the saturated mode. Conformance of modeled to actual data is very good in the constant current regime (saturated mode). A forcing of conformance exists for the very high gate voltages in the linear mode, with departure existing for the linear mode with lesser values of constant gate voltages.

The actual drain voltage in the linear mode is seen to be as much as 20 percent below the modeled value in worst cases. This represents a conservative error for circuit calculations in that the conduction loss is somewhat less than modeled. In addition, the gate drive is usually high under MOSFET conduction, thereby avoiding operation in the regions of discussion.

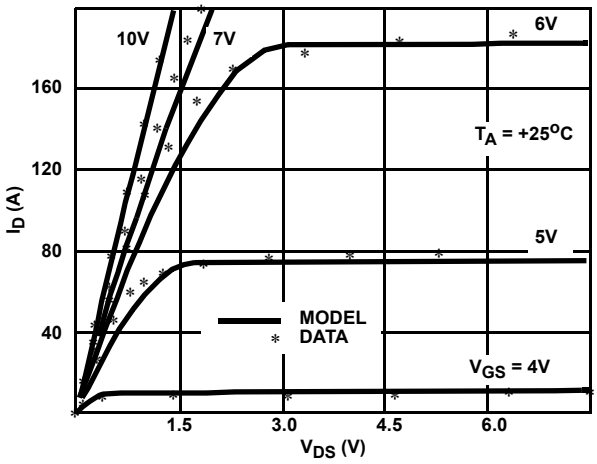

FIGURE 9. OUTPUT CURVES

The discrepancy results because the PSPICE algorithm for a mosfet assumes the channel surface concentration to be constant. In the power MOSFET, the surface concentration is Gaussian along the channel length. Hence, the observed behavior is as would be expected.

The modeled response can be improved by changing the PSPICE algorithm, however changes of this type were ruled out for this work.

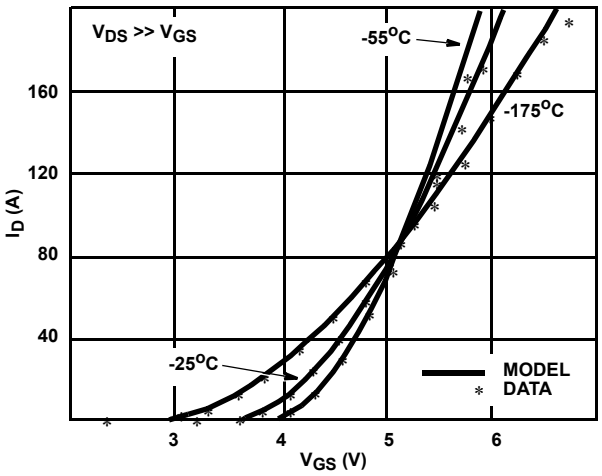

FIGURE 10. TRANSFER CURVES

Excellent agreement exists.

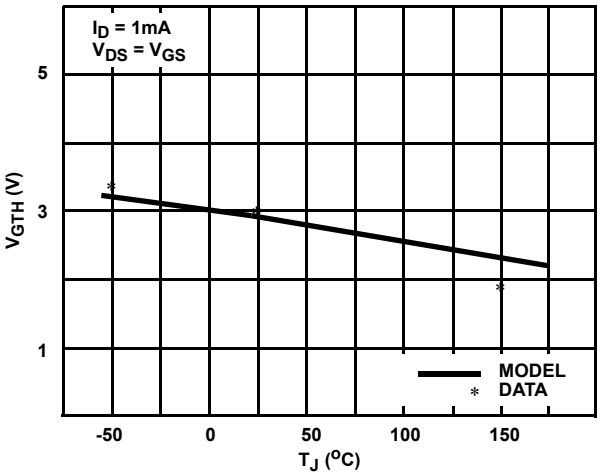

FIGURE 11. THRESHOLD VOLTS

Excellent agreement exists. This would not be so without the inclusion of Mos2 to represent the sharp corners of the many hexagonal cells of the structure. The flat part of the hex cells results in a two dimensional diffusion during processing and the establishment of a source to body junction cross-over concentration at the surface, resulting in Mos1 as modeled. However, the corners of the hex cells introduce a three dimensional diffusion resulting in a lower source to body junction cross-over concentration at the surface. The unpublished work of Klodzinski, et al [11] processed test and control devices upon a common wafer where the corners of the hex source implant were excluded versus included, revealing threshold voltages approximately 0.4 volts higher for the test.

Omission of Mos2 would not impact circuit performance, however a reverence of attached importance to the MOSFET threshold voltage mandates modelled to measured agreement.

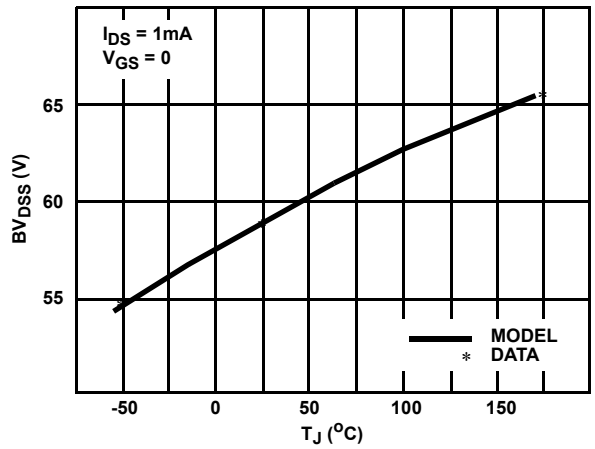

FIGURE 12. BREAKDOWN VOLTAGE, LOW CURRENT BV_{DSS}

Excellent agreement exists.

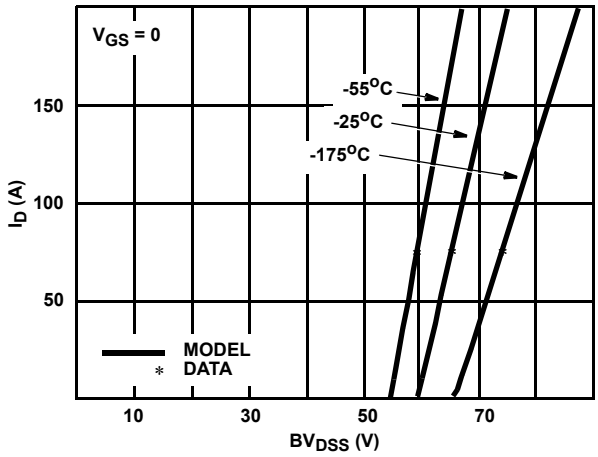

FIGURE 13. BREAKDOWN VOLTAGE, HIGH CURRENT BV_{DSS}

Excellent agreement exists.

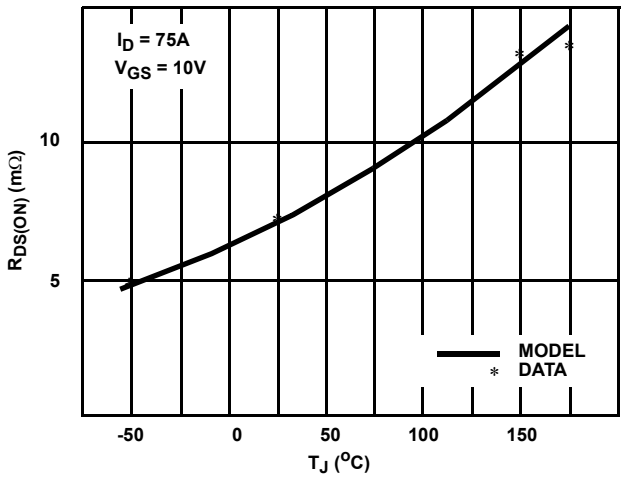

FIGURE 14. ON RESISTANCE vs TEMPERATURE

Excellent agreement exists.

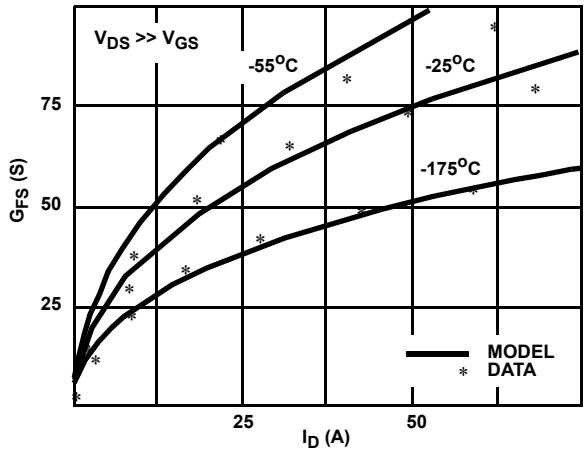

FIGURE 15. TRANSCONDUCTANCE CURVES

Excellent agreement exists.

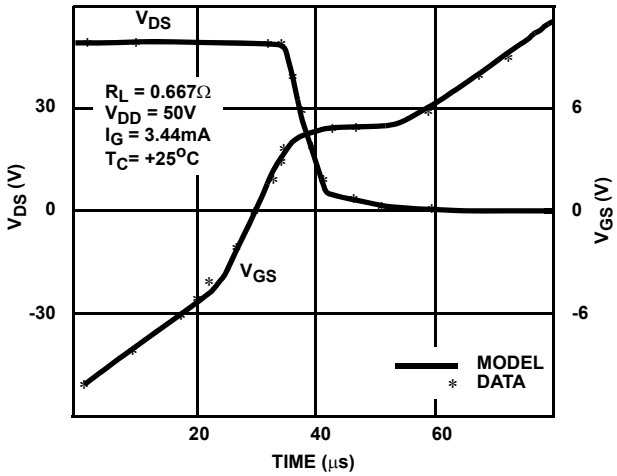

FIGURE 16. GATE CHARGE CURVES

Excellent agreement exists. The non linear behavior of gate charge for negative gate bias is seldom shown. A significant increase in turn on delay results by operating from a negative gate voltage.

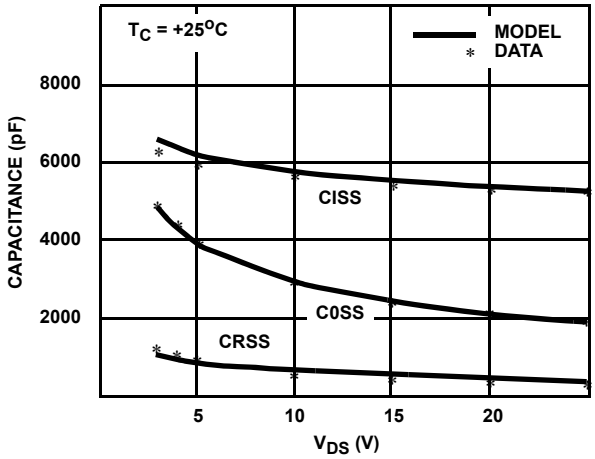

FIGURE 17. CAPACITANCE CURVES

Excellent agreement exists.

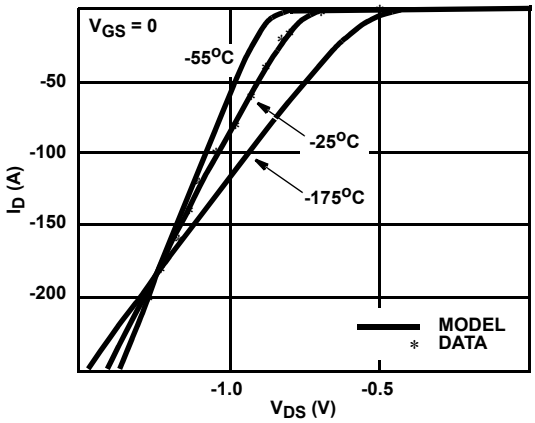

FIGURE 18. BODY DIODE CURVES

All three measured data curves were noted to cross at a drain current of 180amps. Excellent agreement exists.

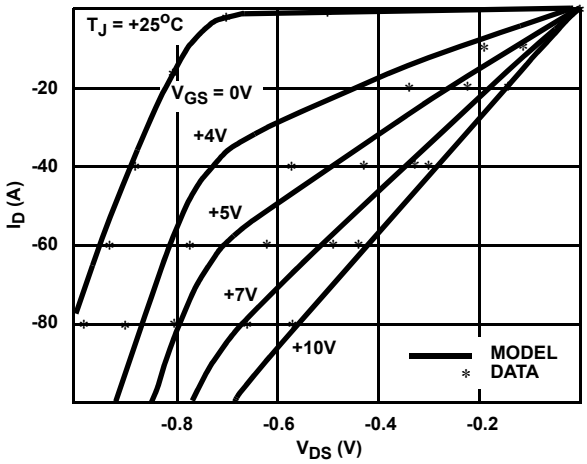

FIGURE 19. 3RD QUADRANT MOSFET CURVES

Good agreement exists. The departure seen between modelled and measured exists for the same reason as the departure of the output curves in the linear regime. This would also be improved by changing the PSpice algorithm as suggested relative to Figure 9.

Parameter Extraction

The sub-circuit is chosen to minimize interdependencies between parameters. A listing of the sub-circuit is presented in Table 2 as a template which routes the Modeler through extraction with guiding comments. Although the template is a complete and workable PSPICE sub-circuit listing, all parameter values except KP and VTO are chosen to be transparent to the results of the analysis. As the transparent values are replaced with extracted values, the model is developed. The listing in Table 2 is structured so that parameters being extracted have very little dependency upon those values which are not yet determined. If desired after completing the extraction, an iteration may be made for the comfort of the Modeler.

EXTRACTION OF MODEL PARAMETERS FROM PHYSICAL MEASUREMENTS

TABEL 2. TEMPLATE		TABLE 3. FINAL MODEL
.SUBCKT TEMPLATE 2 1 3 ; rev 12/17/90 *Nom Temp=25 deg C		.SUBCKT RFH75N05 2 1 3 ; rev 3/20/91 *Nom Temp=25 deg C
Mos1 16 6 8 8 MOSMOD M=0.99 ; .MODEL MOSMOD NMOS (VTO=3 KP=10 +IS=1e-30 N=10 TOX=1 L=1u W=1u)	Step 1	Mos1 16 6 8 8 MOSMOD M=0.99 .MODEL MOSMOD NMOS (VTO=3.48 KP=78.5 +IS=1e-30 N=10 TOX=1 L=1u W=1u)
Mos2 16 21 8 8 MOSMOD M=0.01 ; Vto 21 6 0	Step 2	Mos2 16 21 8 8 MOSMOD M=0.01 Vto 21 6 0.6
Rsource 8 7 RDSMOD 1e-12 ;	Step 3	Rsource 8 7 RDSMOD 2e-3
Rdrain 5 16 RDSMOD 1e-12 ;	Step 4	Rdrain 5 16 RDSMOD 3.07e-3
.MODEL RDSMOD RES (TC1=0 TC2=0)	Step 5	.MODEL RDSMOD RES (TC1=5.2e-3 TC2=1.37e-5)
Evto 20 6 18 8 1 ; Rvto 18 19 RVTOMOD 1 It 8 17 1 Vbat 8 19 DC 1 .MODEL RVTOMOD RES (TC1=0 TC2=0)	Step 6	Evto 20 6 18 8 1 Rvto 18 19 RVTOMOD 1 It 8 17 1 Vbat 8 19 DC 1 .MODEL RVTOMOD RES (TC1=-3.78e-3 TC2=-7.51e-7)
Ebreak 11 7 17 18 1000 ; Dbreak 5 11 DBKMOD Rbreak 17 18 RBKMOD 1	Step 7	Ebreak 11 7 17 18 58.4 Dbreak 5 11 DBKMOD Rbreak 17 18 RBKMOD 1
.MODEL RBKMOD RES (TC1=0 TC2=0) ;	Step 8	.MODEL RBKMOD RES (TC1=9.5e-4 TC2=-1.17e-6)
.MODEL DBKMOD D (RS=0 TRS1=0 TRS2=0) ;	Step 9	.MODEL DBKMOD D (RS=8e-2 TRS1=2.5e-3 TRS2=0)
Dbody 7 5 DBDMOD ; .MODEL DBDMOD D (IS=1e-30 RS=0 TRS1=0 +TRS2=0 CJO=0 TT=0)	Step 10	Dbody 7 5 DBDMOD .MODEL DBDMOD D (IS=2.23e-12 RS=2.28e-3 TRS1=2.98e-3 +TRS2=2.22E-12 CJO=7.55e-9 TT=4e-8)
Lgate 1 9 1e-12 ; Ldrain 2 5 1e-12 Lsource 3 7 1e-12 Rgate 9 20 1	Step 11	Lgate 1 9 5e-9 Ldrain 2 5 1e-9 Lsource 3 7 3e-9 Rgate 9 20 1.2
Cin 6 8 1e-15 ;	Step 12	Cin 6 8 4.48e-9
Dplcap 10 5 DPLCAPMOD ; .MODEL DPLCAPMOD D (CJO=0 IS=1e-30 N=10) Esg 6 10 6 8 1	Step 13	Dplcap 10 5 DPLCAPMOD .MODEL DPLCAPMOD D (CJO=2.14e-9 IS=1e-30 N=10) Esg 6 10 6 8 1
Ca 12 8 1e-15 ; S1a 6 12 13 8 S1AMOD S1b 13 12 13 8 S1BMOD .MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=-3 VOFF=-1) .MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=-1 VOFF=-3) Egs 13 8 6 8 1	Step 14	Ca 12 8 8.98e-9 S1a 6 12 13 8 S1AMOD S1b 13 12 13 8 S1BMOD .MODEL S1AMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=-2.48 VOFF=-0.48) .MODEL S1BMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=-0.48 VOFF=-2.48) Egs 13 8 6 8 1
Cb 15 14 1e-15 ; S2a 6 15 14 13 S2AMOD S2b 13 15 14 13 S2BMOD .MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=-2.5 VOFF=2.5) .MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=2.5 VOFF=-2.5) Eds 14 8 5 8 1	Step 15	Cb 15 14 8.81e-9 S2a 6 15 14 13 S2AMOD S2b 13 15 14 13 S2BMOD .MODEL S2AMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=-2.25 VOFF=2.75) .MODEL S2BMOD VSWITCH (RON=1e-5 ROFF=0.1 +VON=2.75 VOFF=-2.25) Eds 14 8 5 8 1
Rin 6 8 1e9 ;	Step 16	Rin 6 8 1e9
.ENDS		.ENDS

OBTAINING EXPERIMENTAL DATA

When the authors experienced difficulty in parameter extraction the problems were traceable to erroneous data in all cases. The following caveats are offered:

11. Obtain all data from a single device.
12. Read gate voltage data to the nearest 0.01 volt.
13. Employ Kelvin sensing to the package leads.
14. Avoid self heating (a difficult assignment)
15. Inconsistencies lurk in data sheet curves and specifications.

FINAL MODEL

The final model for the RFH75N05 is shown in Table 3 and serves as an aid to understanding as it is developed from the template.

STEP 1 - MODEL MOSMOD (VTO AND KP)

The square root of drain current is plotted versus the gate to source voltage for the MOSFET in the saturated regime; a straight line results. The zero current intercept defines VTO and the slope defines the square root of (KP/2). Vary VTO and KP to obtain the best fit to data for the low to medium current experimental data at 25^{O}C.

VTO is not the threshold voltage as measured. In order to use the algorithm of the PSPICE Level 1 model, W (the channel width) and L (the channel length) are defined as one micron. Therefore KP times W divided by L reduces to the model value called KP. Likewise IS, N, and TOX are set to values chosen to avoid other algorithm problems. Figure 20 shows the PSPICE generated curve after the correct values of KP and VTO of model MOSMOD are chosen.

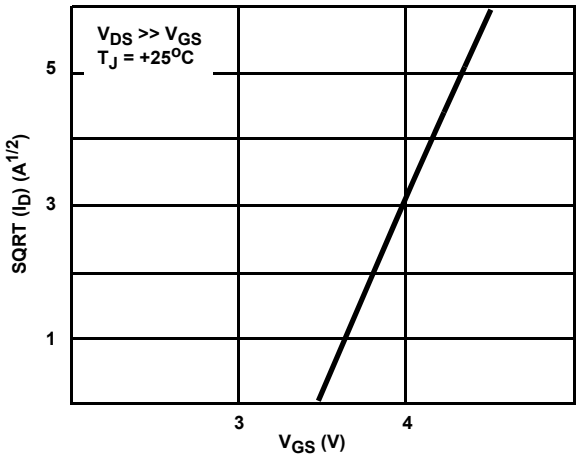

FIGURE 20. SQUARE ROOT OF I_D

STEP 2 - V_{TO}

The threshold voltage is set by fixing the value of V_{TO}. Threshold voltage of a power MOSFET is usually measured in the saturated regime at a low current, typically 1mA. If the PSPICE model is run at 25^{O}C with the gate and drain voltage equal, a voltage will be found to yield 1mA drain current. V_{TO} is this voltage reduced by the measured threshold voltage. The value identified was 0.6 volts.

STEP 3 - R_{SOURCE}

The straight line curve of Figure 20 is modified by a chosen value of R_{SOURCE} in order to better fit the measured data for medium to high currents at 25^{O}C. This is shown in Figure 21, where 2E-3 provided the best fit.

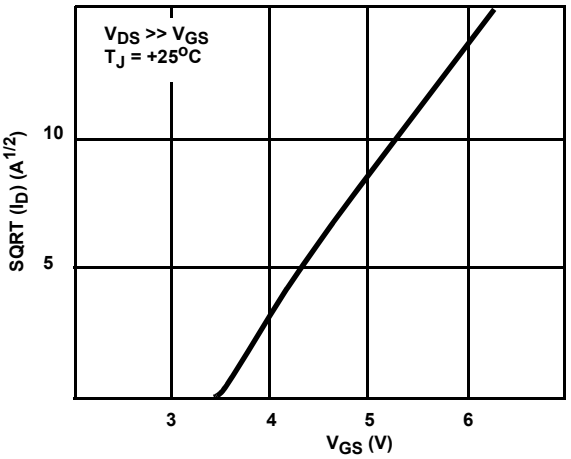

FIGURE 21. SQUARE ROOT OF I_D

STEP 4 - R_{DRAIN}

R_{DRAIN} is chosen to fix the PSPICE calculated $R_{DS(ON)}$ value to the measured value at 25^{O}C when the template is biased to the gate voltage and drain current of the specifications. Do not use the specified maximum of $R_{DS(ON)}$. The value developed was 3.07E-3.

STEP 5 - MODEL RDSMOD (TC1 AND TC2)

R_{SOURCE} and R_{DRAIN} are assumed to have the same temperature coefficients. Although this is not accurate, it is convenient and is deemed to be sufficient for this purpose. If $R_{DS(ON)}$ is measured as a function of temperature, best fit can be obtained by appropriately choosing TC1 and TC2 values of 5.2E-3 and 1.37E-5. $R_{DS(ON)}$ is shown in Figure 22.

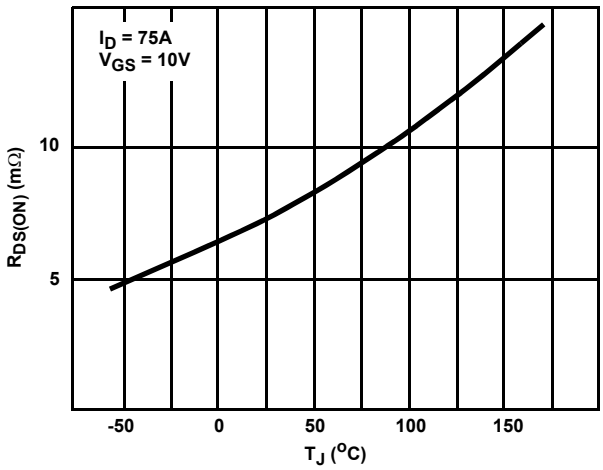

FIGURE 22. $R_{DS(ON)}$ vs TEMPERATURE

STEP 6 - MODEL RVTOMOD (TC1 AND TC2)

The plot of Figure 21 must be modified to add curves at low and high temperature. A temperature sensitive additive or subtractive voltage is placed in series with the gates of Mos1 and Mos2 by use of E_{VTO}. A 1 volt drop equal to It times R_{VTO} is canceled by a 1 volt supply, V_{BAT} and applied to E_{VTO}. By choosing the values of TC1 and TC2 for model RVTOMOD, the voltage of E_{VTO} is made temperature sensitive. The result is shown in Figure 23, where TC1 and TC2 were chosen for best fit at -3.78E-3 and -7.51E-7.

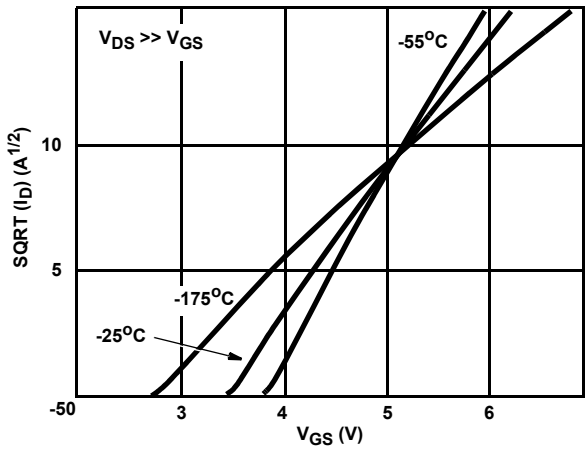

FIGURE 23. TRANSFER CHARACTERISTICS vs TEMPERATURE

STEP 7 - E_{BREAK}

E_{BREAK} derives a thermally variant voltage from the product of I_T and R_{BREAK} equal to 1.00 volt at 25°C. When the drain voltage rises sufficiently, diode D_{BREAK} provides a voltage clamp to E_{BREAK}. The value of the E_{BREAK} multiplier is equal to the low current value of BV_{DSS} less the forward drop of D_{BREAK}. The multiplier was set at 58.4 for the final model.

STEP 8 - MODEL RBKMOD (TC1 AND TC2)

The low current breakdown voltage of the MOSFET may be measured at several temperatures, such that TC1 and TC2 may be determined for model RBKMOD. Figure 24 plots the low current breakdown voltage as a function of temperature as modeled with TC1 and TC2 equal to 9.5E-4 and -1.17E-6.

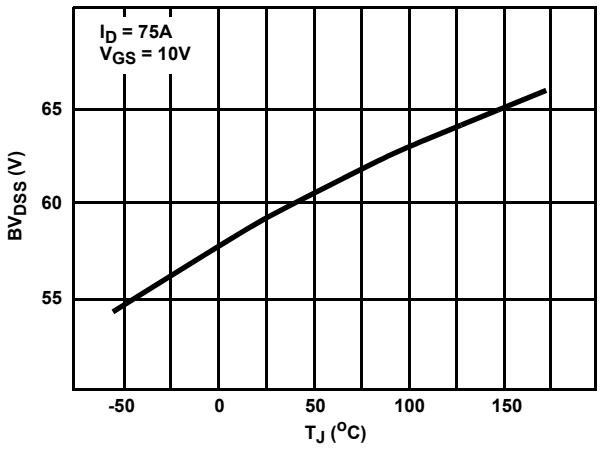

FIGURE 24. BREAKDOWN VOLTAGE vs TEMPERATURE

STEP 9 - MODEL DBKMOD (RS, TRS1 AND TRS2)

Although reliable data is difficult to obtain for the breakdown voltage at many tens of amperes, it can be done with a small inductive flyback circuit of very low duty cycle. RS of the diode D_{BREAK} may be determined at 25°C. TRS1 and TRS2 may be determined with similar measurements at several temperatures. The curves of Figure 25 present the modelled behavior for RS, TRS1 and TRS2 equal to 8E-2, 2.5E-3, and 0.

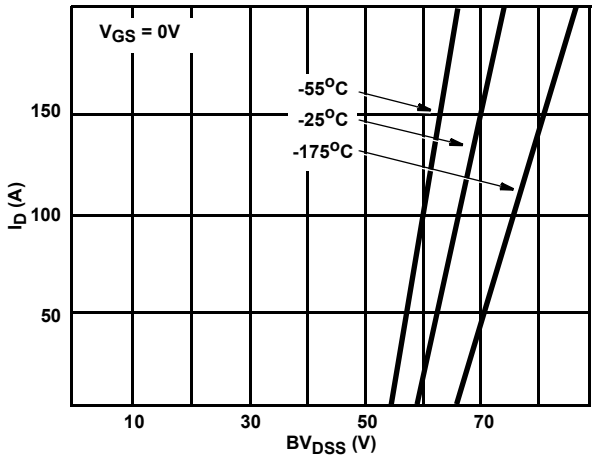

FIGURE 25. BREAKDOWN VOLTAGE vs TEMPERATURE

STEP 10(a) - MODEL DBDMOD (IS, RS, TRS1 and TRS2)

When operating D_{BODY} in the forward mode, one may develop IS and RS at 25°C assuming a diode ideality value of 1.0, the default value. Measurements at elevated current levels and several temperatures will define TRS1 and TRS2. Measurements are taken with V_{GS} equal to zero. Figure 26 presents the body diode forward characteristics for several temperatures where IS, RS, TRS1, and TRS2 are found to equal 2.23E-12, 2.28E-3, 2.98-E3, and 2.22E-12.

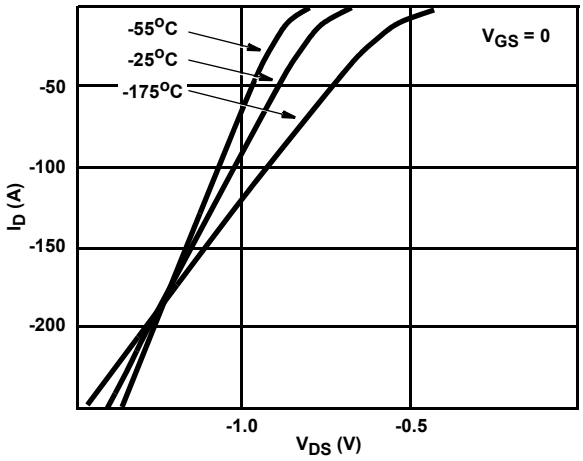

FIGURE 26. BODY DIODE CURVES

STEP 10(b) - MODEL DBDMOD (CJO, TT)

C_{OSS} minus C_{RSS} may be determined at 25 volts and 25°C. Then CJO is this value when adjusted to zero drain volts by the factor of the square root of (25+0.7) or 5.07. For the example this equals 7.55E-9.

In order to determine TT, equipment similar to the Bermar SM30 may be used. This equipment forces a forward body diode current (If) for a sufficiently long period of time, after which a linear amplifier with high current capability ramps the diode current off at a constant rate, di/dt. (Feedback control is used.) The diode current equals zero at time T_F, after the ramp off is initiated. The current continues to ramp, extracting charge from the diode, for an added time T_A. At this time, the constant ramp (di/dt) can no longer be maintained and the reverse current has attained a maximum. TT may be solved [12] and entered using:

$$TT = T_A/(1-\exp(-(T_A+T_F)/TT))$$

The value of TT was determined to equal 4E-8.

STEP 11 - L_{GATE}, L_{DRAIN}, L_{SOURCE}, R_{GATE}

L_{GATE}, L_{DRAIN}, L_{SOURCE}, and R_{GATE} may be measured, estimated or calculated and entered. An approximation for the inductances in nH may be calculated using:

$$L = (5)(length)(\log_e(4(length/diam))) \text{ nH}$$

where wire length and diameter are in inches [13]. Values of Lgate, Ldrain, Lsource, and Rgate were approximated at 5E-9, 1E-9, 3E-9, and 1.2 for the final model.

CAPACITANCES

The capacitances are derived from the measured gate charge curve of Figure 27. They will require some iteration and some judgement calls as will be explained.

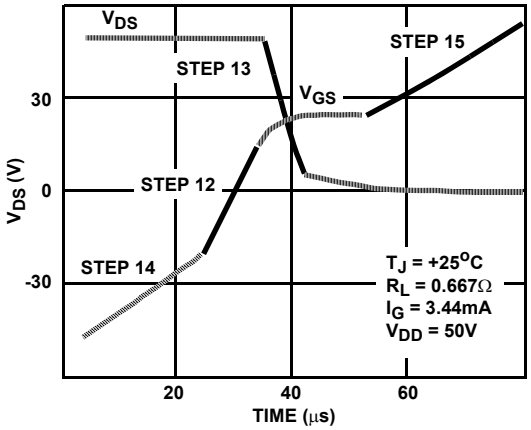

FIGURE 27. GATE CHARGE CURVES

STEP 12 - C_{IN}

The value of C_{IN} should be chosen for best fit to the solid line portion of the V_{GS} curve of Figure 27 labeled step 12. A value of 4.48E-9 was found to provide a good fit.

STEP 13 - MODEL DPLCAPMOD (CJO)

A feedback capacitor is modeled by using the junction capacitance of a reverse biased diode, D_{PLCAP}, as defined by model DPLCAPMOD. IS and N of model DPLCAPMOD were chosen to avoid undesired diode effects. CJO is chosen as 2.14E-9 to best fit the solid line portion of the V_{DS} curve of Figure 27.

STEP 14 - C_A, MODELS S1AMOD and S1BMOD (VON and VOFF)

The value of C_A is chosen to be 8.98E-9 to best parallel the dotted line portion of the V_{GS} curve of Figure 27 labeled step 14.

In order to match the dotted line portion it may be necessary to increment VON and VOFF of both model S1AMOD and model S1BMOD. Note that all four values must be incremented by an identical amount before making a PSPICE run. This incremental change will vertically displace the slope provided by C_A. The transition voltages of S1A and S1B must always be negative values.

The sharpness of transition between the dashed line of step 14 and the solid line of step 12 may be adjusted if necessary by changing the increment between VON and VOFF equally for both S1A and S1B.

STEP 15 - C_B, MODELS S2AMOD and S2BMOD (VON and VOFF)

The value of C_B is chosen to be 8.81E-9 to best parallel the solid line portion of the V_{GS} curve of Figure 27 labeled step 15.

In order to match the solid line portion it may be necessary to increment VON and VOFF of both model S2AMOD and model S2BMOD. Note that all four values must be incremented by an identical amount before making a PSpice run. This increment change will horizontally displace the slope provided by C_B.

The sharpness of transition between the solid line and the low voltage dotted line of the V_{DS} curve may be adjusted if necessary by changing the increment between VON and VOFF equally for both S2A and S2B. It is recommended that this increment be small, of the order of several volts.

STEP 16 - R_{IN}

R_{IN} can be set to a very large value such as 1E15. However it is recommended that it be chosen low enough to cause 10nA to flow at a gate bias of moderately high voltage, typically 1E9 ohms. R_{in} functions to provide an initial gate reference voltage near zero even though the Modeler may choose to drive the MOSFET from a current generator.

EPILOGUE

The final model is completed as shown in Table 3. One may iterate through the steps if desired, but it should not be necessary. Any changes made in the model outside of the above routine should be minimal, if at all.

Anomalies

Some commercially available power MOSFETs exhibit anomalous behavior which is not modelled in this work.

THE VERTICAL JFET PROBLEM

A vertical JFET type of structure exists in the VDMOS device used for the industry standard power MOSFET. Many works describe this portion of the device, including Wheatley, et al [14]. The N^- lightly doped drain region reaches to the surface of the silicon die, which is bounded by the P doped body. This region of N^- is often called the neck of the MOSFET. As the breakdown voltage of the device is designed for increasing

values, the depletion layer extends further within the neck laterally, for relatively low drain voltages. In this manner, the neck or vertical JFET becomes pinched off, causing the $R_{DS(ON)}$ to exhibit excess non-linearity with current. In addition an abrupt limiting of the drain current (at large values of drain voltages) occurs for increasing values of gate voltage. This current limiting has a highly localized thermal assist constrained to the neck with time responses in the microsecond region. This anomaly may be suppressed by increasing the neck width and/or implanting a low dose of N type dopant into the neck, just below the surface.

Devices of this type are not properly modeled.

NON OHMIC CONTACT PROBLEMS

Some commercially available devices exhibit a non-ohmic series contact resistance from the metalization to the silicon. This seldom happens with present day devices, but, when present, it is most likely to occur from source metal to source silicon for N channel devices, and from drain metal to drain silicon for P channel devices. The effect is seen as a low current non-linearity in $R_{DS(ON)}$ vs drain current for the former case and an excessive voltage drop for the body diode for the latter case.

Devices of this type are not properly modeled.

Conclusions

An equivalent circuit model for power MOSFETs that is suitable for use with PSPICE has been demonstrated. The model requires no modifications to the PSPICE algorithms. The model features global temperature representation from -55^{o}C to 175^{o}C for the first time. It addresses static and dynamic behavior over the normal circuit operating range of the device, including 1st and 3rd quadrant MOSFET operation, high current avalanche breakdown operation, body diode stored charge effects, gate charge non-linearities, gate equivalent series resistance (ESR), and package inductances. Gate propagation delay is not modeled [15]. The sub-circuit is empirical in nature and the parameters may be readily extracted by use of terminal measurements. Experimental verification shows excellent agreement between measured and simulated results over the entire thermal, static, and dynamic regimes.

Recommendations For Future Work

A supporting program of algorithms should be written to address the parameter extraction effort.

Accurate testing for characterization of power MOSFETs as a function of temperature is required. Studies should be made to identify and correct methods prone to testing error.

PSPICE algorithms should be modified to refine and incorporate many of the findings of this work into a new MOS level.

If a new MOS level is formed, a modification should be made to the drain current equation in the linear regime to accommodate the non-uniform channel surface concentration of the power MOSFET as described elsewhere. If done, the MOSFET may be more closely modeled in the linear regime of the output characteristic curves and the third quadrant MOSFET regime. (See Figure 9 and Figure 19.) The authors suggest a user defined model value WH to be used in a multiplier which would be applied to Id in the linear regime such that:

$$\text{Multiplier} = (1+WH*(1-V_{DS}/(V_{GS}-V_{TO}))^2)$$

If the multiplier were applied to the MOSFET of Table 3, the 1st and 3rd quadrant characteristics would be approximately as shown in Figure 28 for V_{GS} = 5 volts. Here, WH is shown for values of 0, 1, and 2. The drain and source are interchanged for V_{DS} < 0, as is done in PSPICE.

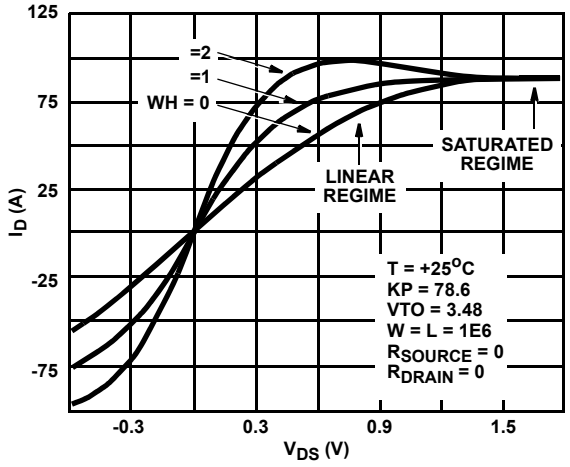

FIGURE 28. THE WH ADJUSTMENT

A value of zero for WH forces the multiplier to equal unity for all values of V_{DS}, thereby retaining the original linear regime equation. Zero should be the default value. Any value of WH greater than 1 results in a negative output resistance and is unacceptable. Therefore WH is bounded by 0 and 1.

If this multiplier option were offered, it would be extracted for the model MOSMOD between steps 3 and 4 of Table 2, probably requiring some iteration between WH and Rdrain.

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