

ISL78840ASxH, ISL78841ASxH, ISL78843ASxH, ISL78845ASxH

Radiation Hardened, High Performance Industry Standard Single-Ended Current Mode PWM Controller

FN7952
Rev 2.00
Feb 23, 2018

The [ISL78840ASEH](#), [ISL78841ASEH](#), [ISL78843ASEH](#), [ISL78845ASEH](#), [ISL78840ASRH](#), [ISL78841ASRH](#), [ISL78843ASRH](#), [ISL78845ASRH](#) are high performance, radiation hardened drop-in replacements for the popular 28C4x and 18C4x PWM controllers suitable for a wide range of power conversion applications including boost, flyback, and isolated output configurations. Fast signal propagation and output switching characteristics make these ideal products for existing and new designs.

Features include up to 13.2V operation, low operating current, 90µA typical start-up current, adjustable operating frequency to 1MHz and high peak current drive capability with 50ns rise and fall times.

Applications

- Current mode switching power supplies
- Isolated buck and flyback regulators
- Boost regulators
- Direction and speed control in motors
- Control of high current FET drivers

Related Literature

For a full list of related documents, visit our website

- [ISL78840ASEH](#), [ISL78841ASEH](#), [ISL78843ASEH](#), [ISL78845ASEH](#), [ISL78840ASRH](#), [ISL78841ASRH](#), [ISL78843ASRH](#), and [ISL78845ASRH](#) product pages

Features

- Electrically screened to DLA SMD #[5962-07249](#)
 - QML qualified per MIL-PRF-38535 requirements
 - 1A MOSFET gate driver
 - 90µA typical start-up current, 125µA maximum
 - 35ns propagation delay current sense to output
 - Fast transient response with peak current-mode control
 - 9V to 13.2V operation
 - Adjustable switching frequency to 1MHz
 - 50ns rise and fall times with 1nF output load
 - Trimmed timing capacitor discharge current for accurate dead time/maximum duty cycle control
 - 1.5MHz bandwidth error amplifier
 - Tight tolerance voltage reference over line, load, and temperature
 - ±3% current limit threshold
 - Pb-free available (RoHS compliant)
 - Radiation environment:
 - High dose rate (50 - 300rad(Si)/s) 100krad(Si)
 - Low dose rate (0.01rad(Si)/s) 100krad(Si)*
- * Product capability established by initial characterization. The "EH" version is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate. (Applies to ISL7884xASEH only)

TABLE 1. KEY DIFFERENCES BETWEEN FAMILY OF PARTS

PART NUMBER	RISING UVLO (V)	MAXIMUM DUTY CYCLE (%)
ISL78840ASxH	7.0	100
ISL78841ASxH	7.0	50
ISL78843ASxH	8.4	100
ISL78845ASxH	8.4	50

Ordering Information

ORDERING NUMBER (Note 1)	PART NUMBER (Note 2)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962R0724905VPC	ISL78840ASEHVD	-55 to +125	8 Ld SBDIP	D8.3
5962R0724906VPC	ISL78841ASEHVD	-55 to +125	8 Ld SBDIP	D8.3
5962R0724907VPC	ISL78843ASEHVD	-55 to +125	8 Ld SBDIP	D8.3
5962R0724908VPC	ISL78845ASEHVD	-55 to +125	8 Ld SBDIP	D8.3
5962R0724905VXC	ISL78840ASEHVF	-55 to +125	8 Ld Flatpack	K8.A
5962R0724906VXC	ISL78841ASEHVF	-55 to +125	8 Ld Flatpack	K8.A
5962R0724907VXC	ISL78843ASEHVF	-55 to +125	8 Ld Flatpack	K8.A
5962R0724908VXC	ISL78845ASEHVF	-55 to +125	8 Ld Flatpack	K8.A
5962R0724905V9A	ISL78840ASEHVX	-55 to +125	Die	
5962R0724906V9A	ISL78841ASEHVX	-55 to +125	Die	
5962R0724907V9A	ISL78843ASEHVX	-55 to +125	Die	
5962R0724908V9A	ISL78845ASEHVX	-55 to +125	Die	
5962R0724901V9A	ISL78840ASRHVX	-55 to +125	Die	
	ISL78840ASRHX/SAMPLE (Note 3)	-55 to +125	Die	
	ISL78840ASRHF/PROTO (Note 3)	-55 to +125	8 Ld Flatpack	K8.A
5962R0724901QXC	ISL78840ASRHQF	-55 to +125	8 Ld Flatpack	K8.A
5962R0724901VXC	ISL78840ASRHVF	-55 to +125	8 Ld Flatpack	K8.A
	ISL78840ASRHD/PROTO (Note 3)	-55 to +125	8 Ld SBDIP	D8.3
5962R0724901QPC	ISL78840ASRHQD	-55 to +125	8 Ld SBDIP	D8.3
5962R0724901VPC	ISL78840ASRHVD	-55 to +125	8 Ld SBDIP	D8.3
5962R0724902V9A	ISL78841ASRHVX	-55 to +125	Die	
	ISL78841ASRHX/SAMPLE (Note 3)	-55 to +125	Die	
	ISL78841ASRHF/PROTO (Note 3)	-55 to +125	8 Ld Flatpack	K8.A
5962R0724902QXC	ISL78841ASRHQF	-55 to +125	8 Ld Flatpack	K8.A
5962R0724902VXC	ISL78841ASRHVF	-55 to +125	8 Ld Flatpack	K8.A
	ISL78841ASRHD/PROTO (Note 3)	-55 to +125	8 Ld SBDIP	D8.3
5962R0724902QPC	ISL78841ASRHQD	-55 to +125	8 Ld SBDIP	D8.3
5962R0724902VPC	ISL78841ASRHVD	-55 to +125	8 Ld SBDIP	D8.3
5962R0724903V9A	ISL78843ASRHVX	-55 to +125	Die	
	ISL78843ASRHX/SAMPLE (Note 3)	-55 to +125	Die	
	ISL78843ASRHF/PROTO (Note 3)	-55 to +125	8 Ld Flatpack	K8.A
5962R0724903QXC	ISL78843ASRHQF	-55 to +125	8 Ld Flatpack	K8.A
5962R0724903VXC	ISL78843ASRHVF	-55 to +125	8 Ld Flatpack	K8.A
	ISL78843ASRHD/PROTO (Note 3)	-55 to +125	8 Ld SBDIP	D8.3
5962R0724903QPC	ISL78843ASRHQD	-55 to +125	8 Ld SBDIP	D8.3
5962R0724903VPC	ISL78843ASRHVD	-55 to +125	8 Ld SBDIP	D8.3
5962R0724904V9A	ISL78845ASRHVX	-55 to +125	Die	
	ISL78845ASRHX/SAMPLE (Note 3)	-55 to +125	Die	
	ISL78845ASRHF/PROTO (Note 3)	-55 to +125	8 Ld Flatpack	K8.A

Ordering Information (Continued)

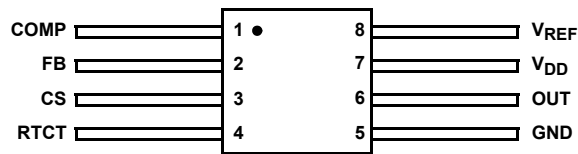
ORDERING NUMBER (Note 1)	PART NUMBER (Note 2)	TEMP. RANGE (°C)	PACKAGE (RoHS Compliant)	PKG. DWG. #
5962R0724904QXC	ISL78845ASRHQF	-55 to +125	8 Ld Flatpack	K8.A
5962R0724904VXC	ISL78845ASRHVF	-55 to +125	8 Ld Flatpack	K8.A
	ISL78845ASRHD/PROTO (Note 3)	-55 to +125	8 Ld SBDIP	D8.3
5962R0724904QPC	ISL78845ASRHQD	-55 to +125	8 Ld SBDIP	D8.3
5962R0724904VPC	ISL78845ASRHVD	-55 to +125	8 Ld SBDIP	D8.3

NOTES:

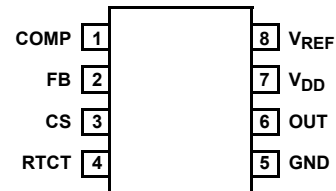
1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the "Ordering Information" table must be used when ordering.
3. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across the temperature range specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE die is capable of meeting the electrical limits and conditions specified in the DLA SMD at +25°C only. The /SAMPLE is a die and does not receive 100% screening across the temperature range to the DLA SMD electrical limits. These part types do not come with a certificate of conformance because there is no radiation assurance testing and they are not DLA qualified devices.

Pin Configurations

ISL78840ASEH, ISL78841ASEH, ISL78843ASEH, ISL78845ASEH
 ISL78840ASRH, ISL78841ASRH, ISL78843ASRH, ISL78845ASRH
 (8 LD FLATPACK)
 TOP VIEW



ISL78840ASEH, ISL78841ASEH, ISL78843ASEH, ISL78845ASEH
 ISL78840ASRH, ISL78841ASRH, ISL78843ASRH, ISL78845ASRH
 (8 LD SBDIP)
 TOP VIEW



Pin Descriptions

PIN NAME	PIN NUMBER	DESCRIPTION
RTCT	4	<p>The oscillator timing control pin. The operational frequency and maximum duty cycle are set by connecting a resistor, RT, between VREF and this pin and a timing capacitor, CT, from this pin to GND. The oscillator produces a sawtooth waveform with a programmable frequency range up to 2.0MHz. The charge time, tC, the discharge time, tD, the RTCT oscillator frequency, f, and the maximum duty cycle, DMAX, can be approximated from Equations 1 through 4:</p> $t_C \approx 0.533 \cdot RT \cdot CT \quad (\text{EQ. 1})$ $t_D \approx -RT \cdot CT \cdot \ln\left(\frac{0.008 \cdot RT - 3.83}{0.008 \cdot RT - 1.71}\right) \quad (\text{EQ. 2})$ $f = 1/(t_C + t_D) \quad (\text{EQ. 3})$ $D = t_C \cdot f \quad (\text{EQ. 4})$ <p>The formulas have increased error at higher frequencies due to propagation delays. Figure 7 may be used as a guideline in selecting the capacitor and resistor values required for a given oscillator frequency for the ISL7884xASxH. The switching frequency for the ISL78841ASxH and ISL78845ASxH will be half the RTCT oscillator frequency.</p>
COMP	1	COMP is the output of the error amplifier and the input of the PWM comparator. The control loop frequency compensation network is connected between the COMP and FB pins.
FB	2	The output voltage feedback is connected to the inverting input of the error amplifier through this pin. The noninverting input of the error amplifier is internally tied to a reference voltage.
CS	3	The current sense input to the PWM comparator. The range of the input signal is nominally 0V to 1.0V and has an internal offset of 100mV.
GND	5	GND is the power and small signal reference ground for all functions.
OUT	6	The drive output to the power switching device. It is a high current output capable of driving the gate of a power MOSFET with peak currents of 1.0A. This GATE output is actively held low when VDD is below the UVLO threshold.
VDD	7	<p>VDD is the power connection for the device. The total supply current will depend on the load applied to OUT. Total IDD current is the sum of the operating current and the average output current. Knowing the operating frequency, f and the MOSFET gate charge, Qg, the average output current can be calculated from Equation 5:</p> $I_{OUT} = Qg \times f \quad (\text{EQ. 5})$ <p>To optimize noise immunity, bypass VDD to GND with a ceramic capacitor as close to the VDD and GND pins as possible.</p>
VREF	8	The 5.00V reference voltage output. +1.0/-1.5% tolerance over line, load and operating temperature. The recommended bypass to GND cap is in the range 0.1µF to 0.22µF. A typical value of 0.15µF can be used.

Functional Block Diagram

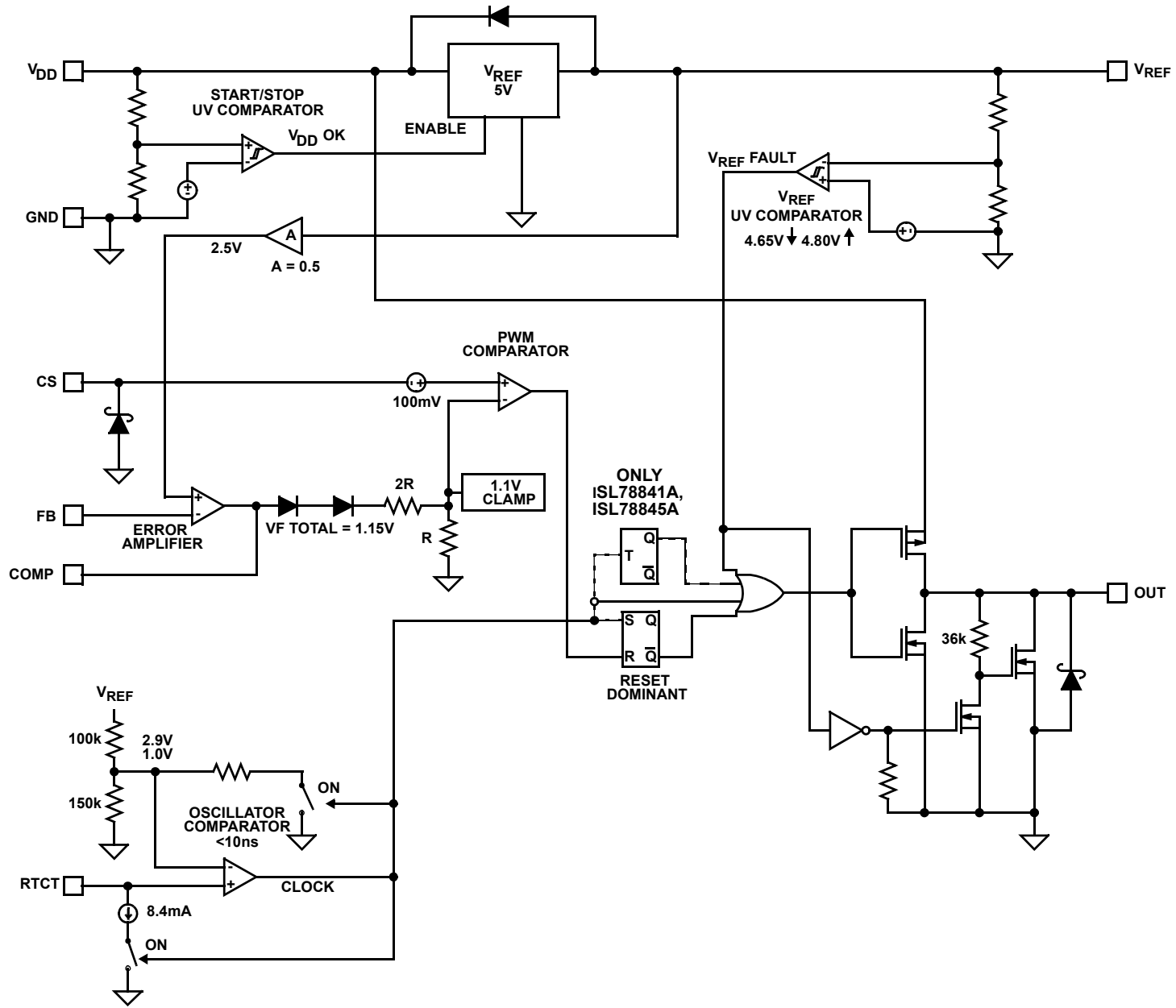


FIGURE 1. BLOCK DIAGRAM

Typical Application - 48V Input Dual Output Flyback

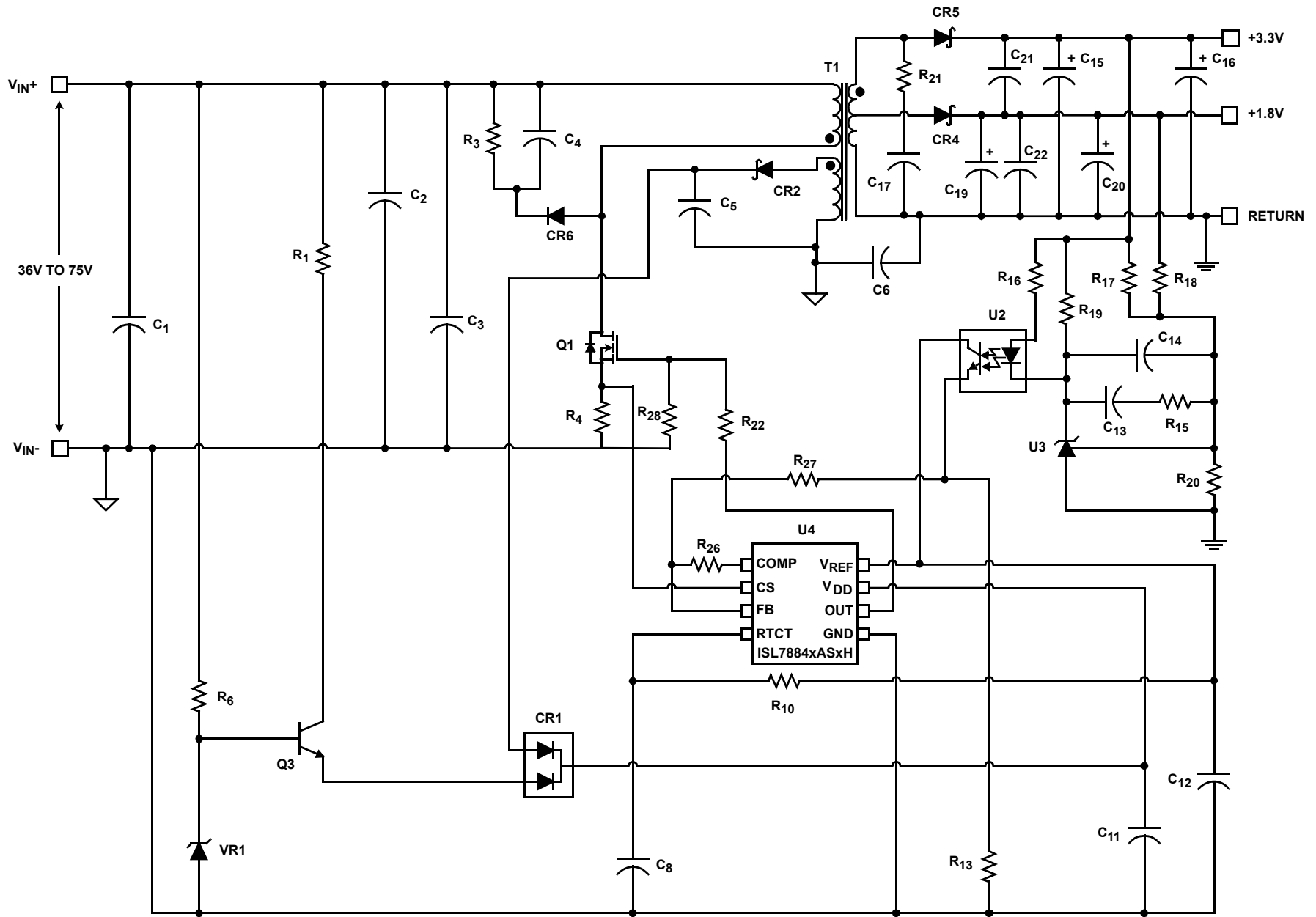


FIGURE 2. TYPICAL APPLICATION - 48V INPUT DUAL OUTPUT FLYBACK

Typical Application - Boost Converter

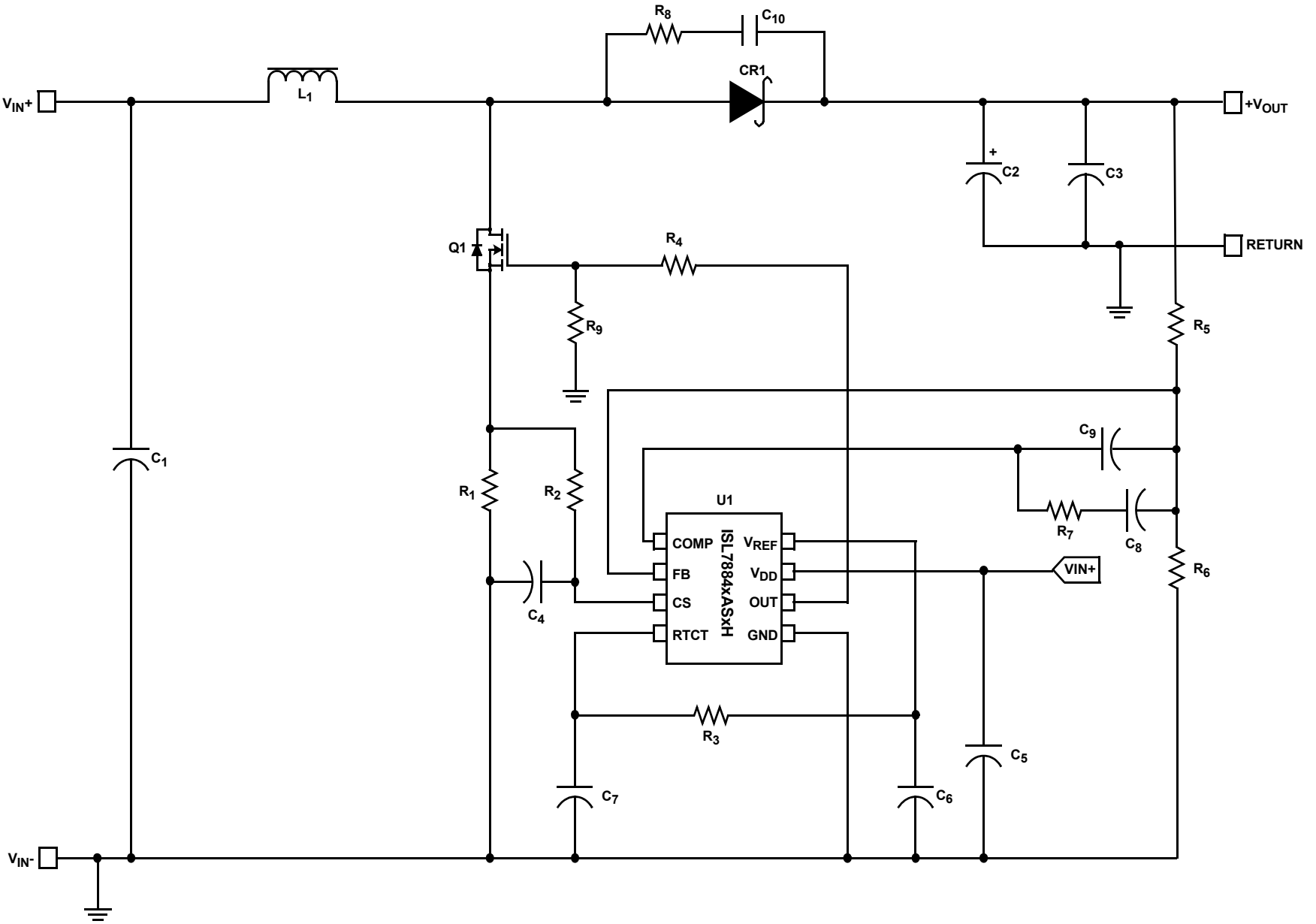


FIGURE 3. TYPICAL APPLICATION - BOOST CONVERTER

Absolute Maximum Ratings

Supply Voltage V_{DD} Without Beam	(GND -0.3V) to +30.0V
Supply Voltage V_{DD} Under Beam	(GND -0.3V) to +14.7V
OUT	(GND -0.3V) to $V_{DD} + 0.3V$
Signal Pins	(GND -0.3V) to 6.0V
Peak GATE Current	1A
ESD Rating	
Human Body Model (Tested per JESD22-A114E)	2kV
Machine Model (Tested per JESD22-A115-A)	200V
Latch-Up (Tested per JESD-78B; Class 2, Level A)	100mA

Recommended Operating Conditions

Temperature Range	-55°C to +125°C
Supply Voltage (Typical Note 6)	9V to 13.2V

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
8 Ld Flatpack Package (Notes 4, 5)	140	15
8 Ld SBDIP Package (Notes 4, 5)	98	15
Maximum Junction Temperature	+150°C	
Storage Temperature Range	-65°C to +150°C	

Radiation Information

Maximum Total Dose	
Dose Rate = 50 - 100radSi/s	100krads (Si)
Dose Rate = 0.01rad(Si)/s (Note 7)	100krad (Si)
SEB (No Burnout) (Note 8)	80Mev/mg/cm ²
SEL (No latch-up) (Note 8)	43Mev/mg/cm ²
SET (Regulated V_{OUT} within ±3%) (Note 8)	40Mev/mg/cm ²

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

- θ_{JA} is measured with the component mounted on a low-effective thermal conductivity test board in free air. See [TB379](#) for details.
- For θ_{JC} , the "case temp" location is the center of the ceramic on the package underside.
- All voltages are with respect to GND.
- Product capability established by initial characterization. The "EH" version is acceptance tested on a wafer-by-wafer basis to 50krad(Si) at low dose rate. (Applied only to ISL7884xASEH.)
- SEE tests performed with V_{REF} bypass capacitor of 0.22µF and $f_{SW} = 200kHz$. SEB/L tests done on a standalone open loop configuration. SET tests done in a closed loop configuration. For LET ≤ 43Mev/mg·cm². The SEL observed requiring a power cycle to recover operation occurred at ≤ 43Mev/mg·cm² < LET ≤ 80Mev/mg·cm². For more information see: [ISL7884xASRH SEE Test Report](#).

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to Block Diagram on [page 5](#) and Typical Application on [page 6](#). $V_{DD} = 13.2V$, $R_T = 10k\Omega$, $C_T = 3.3nF$, $T_A = -55$ to $+125^\circ C$. Typical values are at $T_A = +25^\circ C$. **Boldface limits apply across the operating temperature range, -55 to +125°C.**

PARAMETER	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
UNDERVOLTAGE LOCKOUT					
START Threshold	ISL78840A, ISL78841A	6.5	7.0	7.5	V
	ISL78843A, ISL78845A	8.0	8.4	9.0	V
STOP Threshold	ISL78840A, ISL78841A	6.1	6.6	6.9	V
	ISL78843A, ISL78845A	7.3	7.6	8.0	V
Hysteresis	ISL78840A, ISL78841A	-	0.4	-	V
	ISL78843A, ISL78845A	-	0.8	-	V
Start-Up Current, I_{DD}	$V_{DD} < \text{START Threshold}$	-	90	125	µA
	$V_{DD} < \text{START Threshold}, 100krad$	-	300	500	µA
Operating Current, I_{DD}	(Note 9)	-	2.9	4.0	mA
Operating Supply Current, I_D	Includes 1nF GATE loading	-	4.75	5.50	mA
REFERENCE VOLTAGE					
Overall Accuracy	Over line ($V_{DD} = 9V$ to $13.2V$), load of 1mA and 10mA, temperature	4.925	5.000	5.050	V
Long Term Stability	$T_A = +125^\circ C$, 1000 hours (Note 10)	-	5	-	mV
Current Limit, Sourcing		-20	-	-	mA
Current Limit, Sinking		5	-	-	mA
CURRENT SENSE					
Input Bias Current	$V_{CS} = 1V$	-1.0	-	1.0	µA

Electrical Specifications Recommended operating conditions unless otherwise noted. Refer to Block Diagram on [page 5](#) and Typical Application on [page 6](#). $V_{DD} = 13.2V$, $R_T = 10k\Omega$, $C_T = 3.3nF$, $T_A = -55$ to $+125^\circ C$. Typical values are at $T_A = +25^\circ C$. **Boldface limits apply across the operating temperature range, -55 to +125°C. (Continued)**

PARAMETER	TEST CONDITIONS	MIN (Note 11)	TYP	MAX (Note 11)	UNIT
Input Signal, Maximum		0.97	1.00	1.03	V
Gain, $A_{CS} = \Delta V_{COMP} / \Delta V_{CS}$	$0 < V_{CS} < 910mV$, $V_{FB} = 0V$	2.75	2.82	3.15	V/V
CS to OUT Delay		-	35	55	ns
ERROR AMPLIFIER					
Open Loop Voltage Gain	(Note 10)	-	90	-	dB
Unity Gain Bandwidth	(Note 10)	-	1.5	-	MHz
Reference Voltage, V_{REF}	$V_{FB} = V_{COMP}$	2.475	2.500	2.530	V
FB Input Bias Current, FBI_{IB}	$V_{FB} = 0V$	-1.0	-0.2	1.0	μA
COMP Sink Current	$V_{COMP} = 1.5V$, $V_{FB} = 2.7V$	1.0	-	-	mA
COMP Source Current	$V_{COMP} = 1.5V$, $V_{FB} = 2.3V$	-0.4	-	-	mA
COMP V_{OH}	$V_{FB} = 2.3V$	4.80	-	V_{REF}	V
COMP V_{OL}	$V_{FB} = 2.7V$	0.4	-	1.0	V
PSRR	Frequency = 120Hz, $V_{DD} = 9V$ to $13.2V$ (Note 10)	-	80	-	dB
OSCILLATOR					
Frequency Accuracy	Initial, $T_A = +25^\circ C$	48	51	53	kHz
Frequency Variation with V_{DD}	$T_A = +25^\circ C$, $(f_{13.2V} - f_{9V}) / f_{12V}$	-	0.2	1.0	%
Temperature Stability	(Note 10)	-	5	-	%
Amplitude, Peak-to-Peak	Static Test	-	1.75	-	V
RTCT Discharge Voltage (Valley Voltage)	Static Test	-	1.0	-	V
Discharge Current	RTCT = 2.0V	6.5	7.8	8.5	mA
OUTPUT					
Gate V_{OH}	V_{DD} to OUT, $I_{OUT} = -100mA$	-	1.0	2.0	V
Gate V_{OL}	OUT to GND, $I_{OUT} = 100mA$	-	1.0	2.0	V
Peak Output Current	$C_{OUT} = 1nF$ (Note 10)	-	1.0	-	A
Rise Time	$C_{OUT} = 1nF$	-	35	60	ns
Fall Time	$C_{OUT} = 1nF$	-	20	40	ns
OUTPUT OFF State Leakage	$V_{DD} = 5V$	-	-	50	μA
PWM					
Maximum Duty Cycle (ISL78840A, ISL78843A)	COMP = V_{REF}	94.0	96.0	-	%
Maximum Duty Cycle (ISL78841A, ISL78845A)	COMP = V_{REF}	47.0	48.0	-	%
Minimum Duty Cycle	COMP = GND	-	-	0	%

NOTES:

9. This is the V_{DD} current consumed when the device is active but not switching. Does not include gate drive current.
10. Limits established by characterization and are not production tested.
11. Parameters with MIN and/or MAX limits are 100% tested at $+25^\circ C$, unless otherwise specified. Temperature limits established by characterization and are not production tested.

Typical Performance Curves

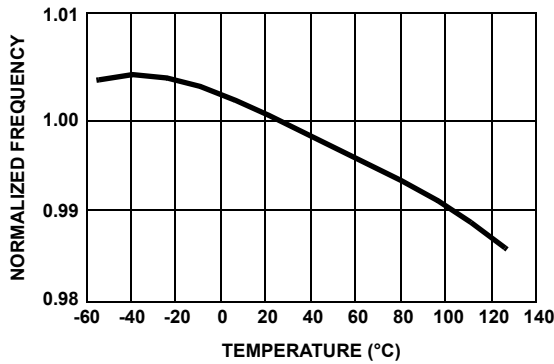


FIGURE 4. FREQUENCY vs TEMPERATURE

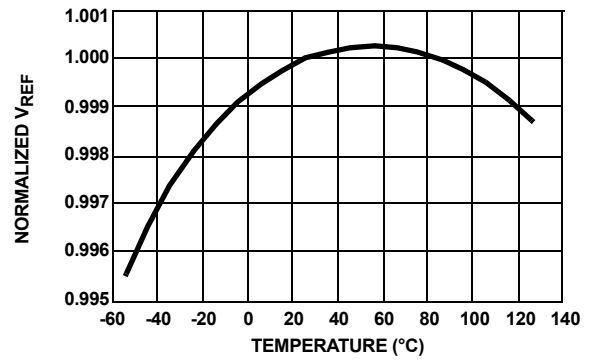


FIGURE 5. REFERENCE VOLTAGE vs TEMPERATURE

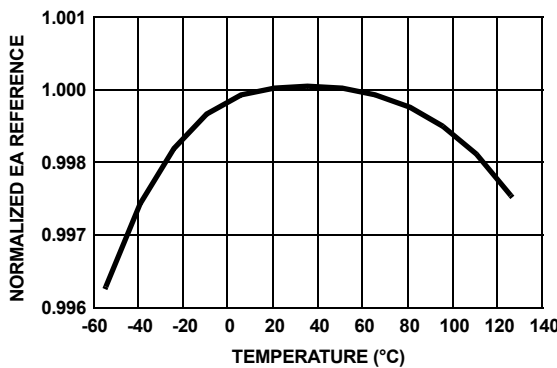


FIGURE 6. EA REFERENCE vs TEMPERATURE

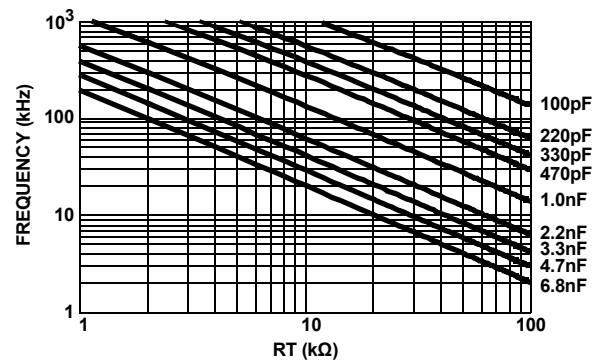


FIGURE 7. RESISTANCE FOR CT CAPACITOR VALUES GIVEN

Functional Description

Features

The ISL7884xASxHs' current mode PWM makes an ideal choice for low-cost flyback and forward topology applications. With their greatly improved performance over industry standard parts, they are the obvious choice for new designs or existing designs, which require updating.

Oscillator

The ISL7884xASxH devices have a sawtooth oscillator with a programmable frequency range to 2MHz, which can be programmed with a resistor from V_{REF} and a capacitor to GND on the RTCT pin. (Please refer to [Figure 7](#) for the resistor and capacitance required for a given frequency.)

Soft-Start Operation

Soft-start must be implemented externally. One method, illustrated below, clamps the voltage on COMP.

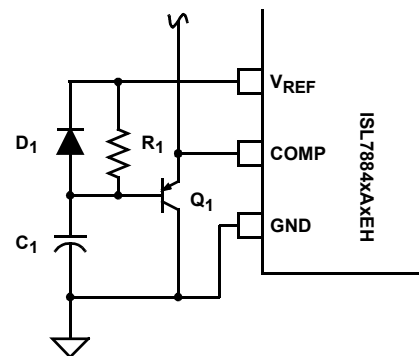


FIGURE 8. SOFT-START

The COMP pin is clamped to the voltage on capacitor C_1 plus a base-emitter junction by transistor Q_1 . C_1 is charged from V_{REF} through resistor R_1 and the base current of Q_1 . At power-up C_1 is fully discharged, COMP is at $\sim 0.7V$, and the duty cycle is zero. As C_1 charges, the voltage on COMP increases and the duty cycle increases in proportion to the voltage on C_1 . When COMP reaches the steady state operating point, the control loop takes over and soft-start is complete. C_1 continues to charge up to V_{REF} and no longer affects COMP. During power-down, diode D_1 quickly discharges C_1 so that the soft-start circuit is properly initialized prior to the next power-on sequence.

Gate Drive

The ISL7884xAxEH devices are capable of sourcing and sinking 1A peak current. To limit the peak current through the IC, an optional external resistor may be placed between the totem-pole output of the IC (OUT pin) and the gate of the MOSFET. This small series resistor also damps any oscillations caused by the resonant tank of the parasitic inductances in the traces of the board and the FETs input capacitance. TID environment of $>50krads$ requires the use of a bleeder resistor of 10k from the OUT pin to GND.

Slope Compensation

For applications where the maximum duty cycle is less than 50%, slope compensation may be used to improve noise immunity, particularly at lighter loads. The amount of slope compensation required for noise immunity is determined empirically, but is generally about 10% of the full scale current feedback signal. For applications where the duty cycle is greater than 50%, slope compensation is required to prevent instability.

Slope compensation may be accomplished by summing an external ramp with the current feedback signal or by subtracting the external ramp from the voltage feedback error signal. Adding the external ramp to the current feedback signal is the more popular method.

From the small signal current-mode model [1] it can be shown that the naturally-sampled modulator gain, F_m , without slope compensation is calculated in Equation 6:

$$F_m = \frac{1}{S_n t_{SW}} \quad (\text{EQ. 6})$$

where S_n is the slope of the sawtooth signal and t_{SW} is the duration of the half-cycle. When an external ramp is added, the modulator gain becomes Equation 7:

$$F_m = \frac{1}{(S_n + S_e) t_{SW}} = \frac{1}{m_c S_n t_{SW}} \quad (\text{EQ. 7})$$

where S_e is slope of the external ramp and becomes Equation 8:

$$m_c = 1 + \frac{S_e}{S_n} \quad (\text{EQ. 8})$$

The criteria for determining the correct amount of external ramp can be determined by appropriately setting the damping factor of the double-pole located at the switching frequency. The double-pole will be critically damped if the Q-factor is set to 1, over-damped for $Q < 1$ and under-damped for $Q > 1$. An under-damped condition may result in current loop instability.

$$Q = \frac{1}{\pi(m_c(1-D) - 0.5)} \quad (\text{EQ. 9})$$

where D is the percent of on-time during a switching cycle. Setting $Q = 1$ and solving for S_e yields Equation 10:

$$S_e = S_n \left(\left(\frac{1}{\pi} + 0.5 \right) \frac{1}{1-D} - 1 \right) \quad (\text{EQ. 10})$$

Because S_n and S_e are the on-time slopes of the current ramp and the external ramp, respectively, they can be multiplied by t_{ON} to obtain the voltage change that occurs during t_{ON} .

$$V_e = V_n \left(\left(\frac{1}{\pi} + 0.5 \right) \frac{1}{1-D} - 1 \right) \quad (\text{EQ. 11})$$

where V_n is the change in the current feedback signal (ΔI) during the on-time and V_e is the voltage that must be added by the external ramp.

For a flyback converter, V_n can be solved in terms of input voltage, current transducer components and primary inductance, yielding Equation 12:

$$V_e = \frac{D \cdot t_{SW} \cdot V_{IN} \cdot R_{CS}}{L_p} \left(\left(\frac{1}{\pi} + 0.5 \right) \frac{1}{1-D} - 1 \right) \quad V \quad (\text{EQ. 12})$$

where R_{CS} is the current sense resistor, t_{SW} is the switching period, L_p is the primary inductance, V_{IN} is the minimum input voltage and D is the maximum duty cycle.

The current sense signal at the end of the ON time for CCM operation is Equation 13:

$$V_{CS} = \frac{N_s \cdot R_{CS}}{N_p} \left(I_O + \frac{(1-D) \cdot V_O \cdot t_{sw}}{2L_s} \right) \quad V \quad (\text{EQ. 13})$$

where V_{CS} is the voltage across the current sense resistor, L_s is the secondary winding inductance and I_O is the output current at current limit. Equation 13 assumes the voltage drop across the output rectifier is negligible.

Because the peak current limit threshold is 1.00V, the total current feedback signal plus the external ramp voltage must sum to this value when the output load is at the current limit threshold as shown in Equation 14:

$$V_e + V_{CS} = 1V \quad (\text{EQ. 14})$$

Substituting Equations 12 and 13 into Equation 14 and solving for R_{CS} yields Equation 15:

$$R_{CS} = \frac{1}{\frac{D \cdot T_{sw} \cdot V_{IN}}{L_p} \cdot \left(\frac{1}{\pi} + 0.5 \right) \frac{1}{1-D} - 1} + \frac{N_s}{N_p} \cdot \left(I_O + \frac{(1-D) \cdot V_O \cdot t_{sw}}{2L_s} \right) \quad (\text{EQ. 15})$$

Adding slope compensation is accomplished in the ISL7884xASxH devices using an external buffer transistor and the RTCT signal. A typical application sums the buffered RTCT signal with the current sense feedback and applies the result to the CS pin as shown in [Figure 9](#).

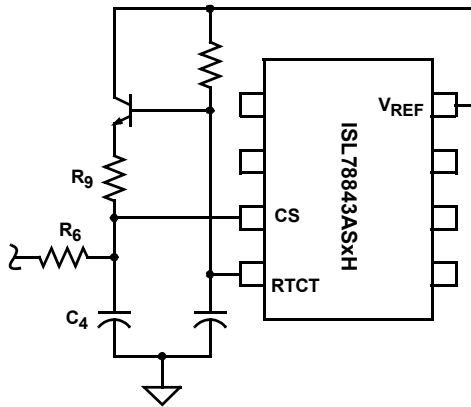


FIGURE 9. SLOPE COMPENSATION

Assuming the designer has selected values for the RC filter (R_6 and C_4) placed on the CS pin, the value of R_9 required to add the appropriate external ramp can be found by superposition.

$$V_e = \frac{2.05D \cdot R_6}{R_6 + R_9} \quad V \quad (\text{EQ. 16})$$

The factor of 2.05 in [Equation 16](#) arises from the peak amplitude of the sawtooth waveform on RTCT minus a base-emitter junction drop. That voltage multiplied by the maximum duty cycle is the voltage source for the slope compensation. Rearranging to solve for R_9 yields [Equation 17](#):

$$R_9 = \frac{(2.05D - V_e) \cdot R_6}{V_e} \quad \Omega \quad (\text{EQ. 17})$$

The value of R_{CS} determined in [Equation 15](#) must be rescaled so that the current sense signal presented at the CS pin is that predicted by [Equation 13](#). The divider created by R_6 and R_9 makes this necessary.

$$R'_{CS} = \frac{R_6 + R_9}{R_9} \cdot R_{CS} \quad (\text{EQ. 18})$$

Example:

$$V_{IN} = 12V$$

$$V_O = 48V$$

$$L_s = 800\mu H$$

$$N_s/N_p = 10$$

$$L_p = 8.0\mu H$$

$$I_O = 200mA$$

$$\text{Switching Frequency, } f_{SW} = 200kHz$$

$$\text{Duty Cycle, } D = 28.6\%$$

$$R_6 = 499\Omega$$

Solve for the current sense resistor, R_{CS} , using [Equation 15](#).

$$R_{CS} = 295m\Omega$$

Determine the amount of voltage, V_e , that must be added to the current feedback signal using [Equation 12](#).

$$V_e = 92.4mV$$

Using [Equation 17](#), solve for the summing resistor, R_9 , from CT to CS.

$$R_9 = 2.67k\Omega$$

Determine the new value of R_{CS} (R'_{CS}) using [Equation 18](#).

$$R'_{CS} = 350m\Omega$$

Additional slope compensation may be considered for design margin. The previous discussion determines the minimum external ramp that is required. The buffer transistor used to create the external ramp from RTCT should have a sufficiently high gain (>200) so as to minimize the required base current. Whatever base current is required reduces the charging current into RTCT and will reduce the oscillator frequency.

Fault Conditions

A Fault condition occurs if V_{REF} falls below 4.65V. When a Fault is detected, OUT is disabled. When V_{REF} exceeds 4.80V, the Fault condition clears and OUT is enabled.

Ground Plane Requirements

Careful layout is essential for satisfactory operation of the device. A good ground plane must be employed. A unique section of the ground plane must be designated for high di/dt currents associated with the output stage. V_{DD} should be bypassed directly to GND with good high frequency capacitors.

References

- [1] Ridley, R., "A New Continuous-Time Model for Current Mode Control", IEEE Transactions on Power Electronics, Vol. 6, No. 2, April 1991.

Package Characteristics

Weight of Packaged Device

8 Ld Mini DIP: 0.7004 Grams
 8 Ld Flatpack: 0.3605 Grams

Die Characteristics

Die Dimensions

2030µm x 2030µm (80 mils x 80 mils)
 Thickness: 482µm ±25.4µm (19.0 mils ±1 mil)

Interface Materials

GLASSIVATION

Type: Silicon Oxide and Silicon Nitride
 Thickness: 0.3µm ±0.03µm to 1.2µm ±0.12µm

TOP METALLIZATION

Type: AlCu (99.5%/0.5%)
 Thickness: 2.7µm ±0.4µm

SUBSTRATE

Silicon

BACKSIDE FINISH

Silicon

PROCESS

0.6µm BiCMOS Junction Isolated

ASSEMBLY RELATED INFORMATION

Substrate Potential

Unbiased

ADDITIONAL INFORMATION

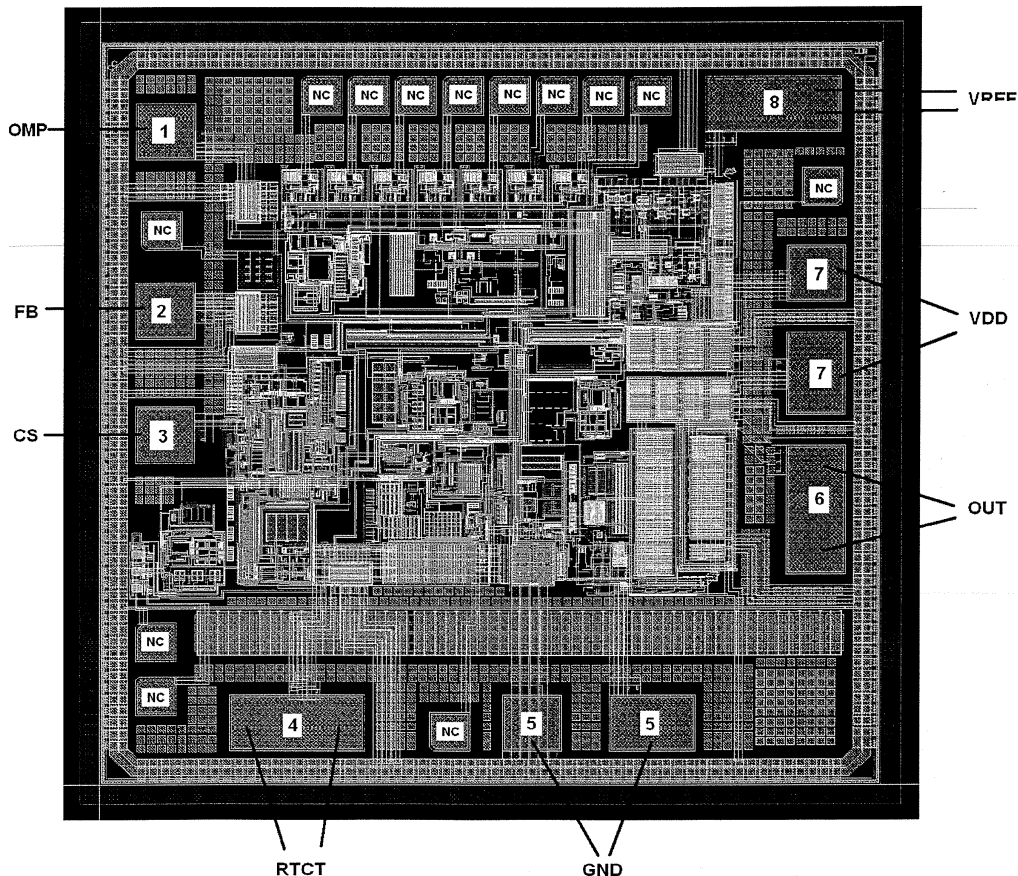
Worst Case Current Density

$< 2 \times 10^5 \text{ A/cm}^2$

Transistor Count

1278

Die Map



Revision History The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest Rev.

DATE	REVISION	CHANGE
Feb 23, 2018	FN7952.2	Updated Related Literature. Updated Ordering Information table. Added Note 3. Removed About Intersil section. Updated disclaimer.
Apr 8, 2016	FN7952.1	Added part numbers "ISL78840ASRH, ISL78841ASRH, ISL78843ASRH, ISL78845ASRH" throughout the datasheet. Added Related Literature section on page 1. Moved Table 1 from page 1 to page 1. Moved and updated the "Pin Descriptions" on page 4. Updated the "Radiation Information" on page 8: Updated SEL (No latch-up) from "80Mev/mg/cm ² " to "43Mev/mg/cm ² ". Moved Note 8 (old Note 9) from page 9 to the end of the Abs max table.
May 4, 2012	FN7952.0	Initial Release.

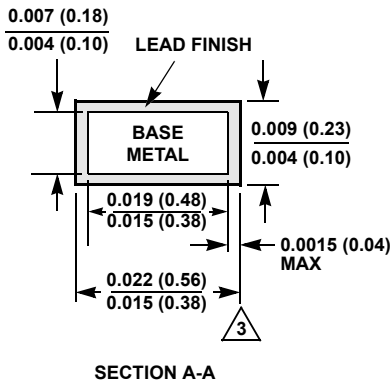
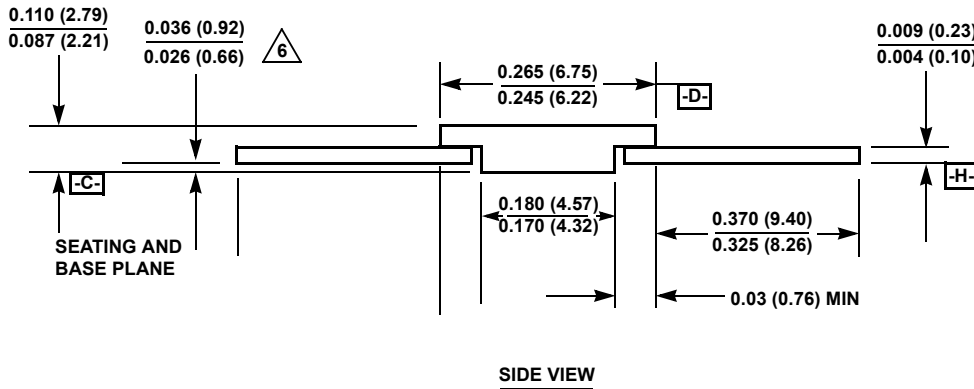
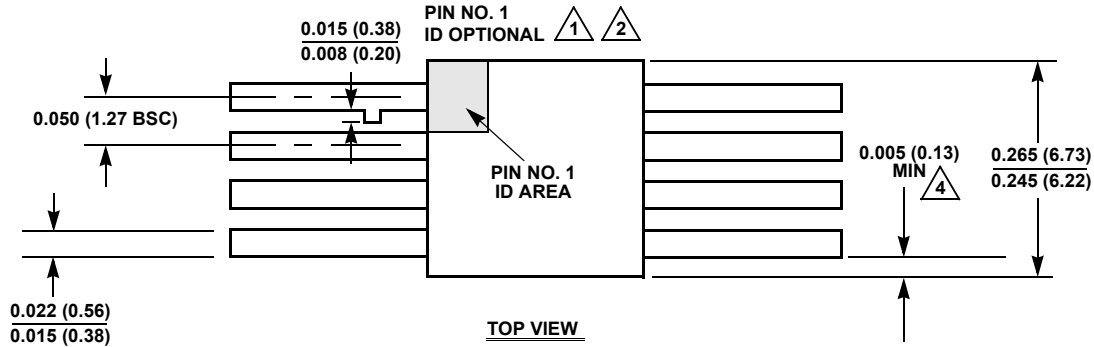
Package Outline Drawing

For the most recent package outline drawing, see [K8.A](#).

K8.A

8 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

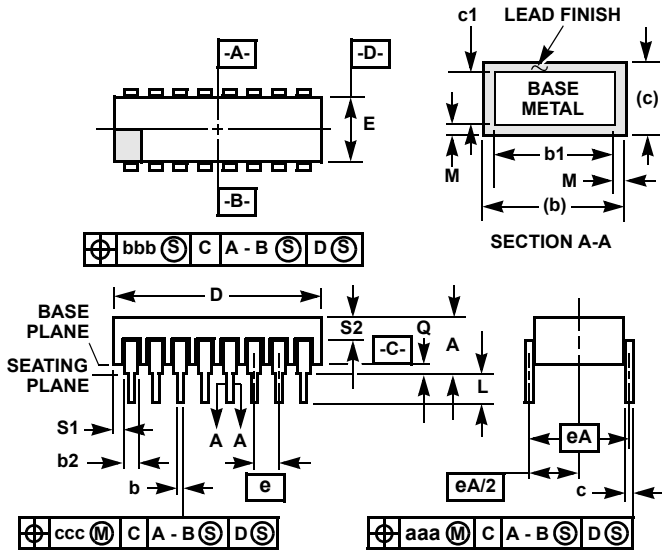
Rev 4, 12/14



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab may be used to identify pin one.
2. If a pin one identification mark is used in addition to or instead of a tab, the limits of the tab dimension do not apply.
3. The maximum limits of lead dimensions (section A-A) shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
4. Measure dimension at all four corners.
5. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
6. Dimension shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
7. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
8. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2 and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.

**D8.3 MIL-STD-1835 CDIP2-T8 (D-4, CONFIGURATION C)
8 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE**

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.405	-	10.29	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
a	90°	105°	90°	105°	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	8		8		8

Rev. 0 4/94

For the most recent package outline drawing, see [D8.3](#).

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