ISL71830SEH

Radiation Tolerant 5V 16-Channel Analog Multiplexer

The ISL71830SEH is a radiation tolerant, 16-channel multiplexer that is fabricated using the proprietary P6 SOI process technology to provide excellent latch-up performance. It operates with a single supply range from 3V to 5.5V and has a 4-bit address line plus an enable that can be driven with adjustable logic thresholds to conveniently select one of 16 available channels. An inactive channel is separated from the active channel by a high impedance, which inhibits any interaction between the channels.

The ISL71830SEH low $r_{DS(ON)}$ allows for improved signal integrity and reduced power losses. The ISL71830SEH is also designed for cold sparing, making it excellent for redundancy in high reliability applications. It is designed to provide a high impedance to the analog source in a powered off condition, making it easy to add additional backup devices without incurring extra power dissipation. The ISL71830SEH also has analog overvoltage protection on the input that disables the switch during an overvoltage event to protect upstream and downstream devices.

The ISL71830SEH is available in a 28 Ld CDFP and operates across the extended temperature range of -55°C to +125°C.

A 32-channel version is also available offered in a 48 Ld CQFP. Refer to the ISL71831SEH datasheet for more information. For a list of differences between the ISL71830SEH and ISL71831SEH, refer to Table 4.

Features

- DLA SMD# 5962-15247
- Fabricated using P6 SOI process technology
- Rail-to-rail operation
- No latch-up
- Low $r_{DS(ON)}$: <120Ω (maximum)
- Single supply operation: 3V to 5.5V
  - Adjustable logic threshold control
- Cold sparing capable: -0.4V to 7V
- Analog overvoltage range: -0.4V to 7V
- Switch input off leakage: 120nA
- Transition times (t_{AHL}): 70ns
- Internally grounded metal lid
- Break-before-make switching
- ESD protection ≥5kV (HBM)
- Operating temperature range: -55°C to +125°C
- Radiation acceptance testing
  - Low dose rate (0.01rad(Si)/s): 75krad(Si)
    Note: All lots were assurance tested to 75krad (0.01rad(Si)/s) wafer-by-wafer.
- SEE hardness (see SEE report for details)
  - SEL/SEB LET_{TH} (V^+ = 6.5V): 60MeV•cm^2/mg

Applications

- Telemetry signal processing
- Harsh environments
- Down-hole drilling

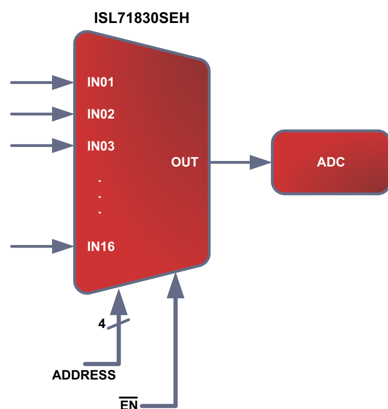

Figure 1. Typical Application

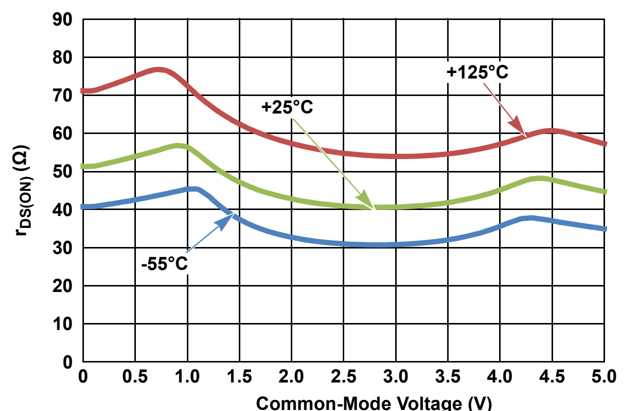

Figure 2. $r_{DS(ON)}$ vs Common-Mode Voltage (V^+ = 5V)

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1. Overview

1.1 Block Diagram

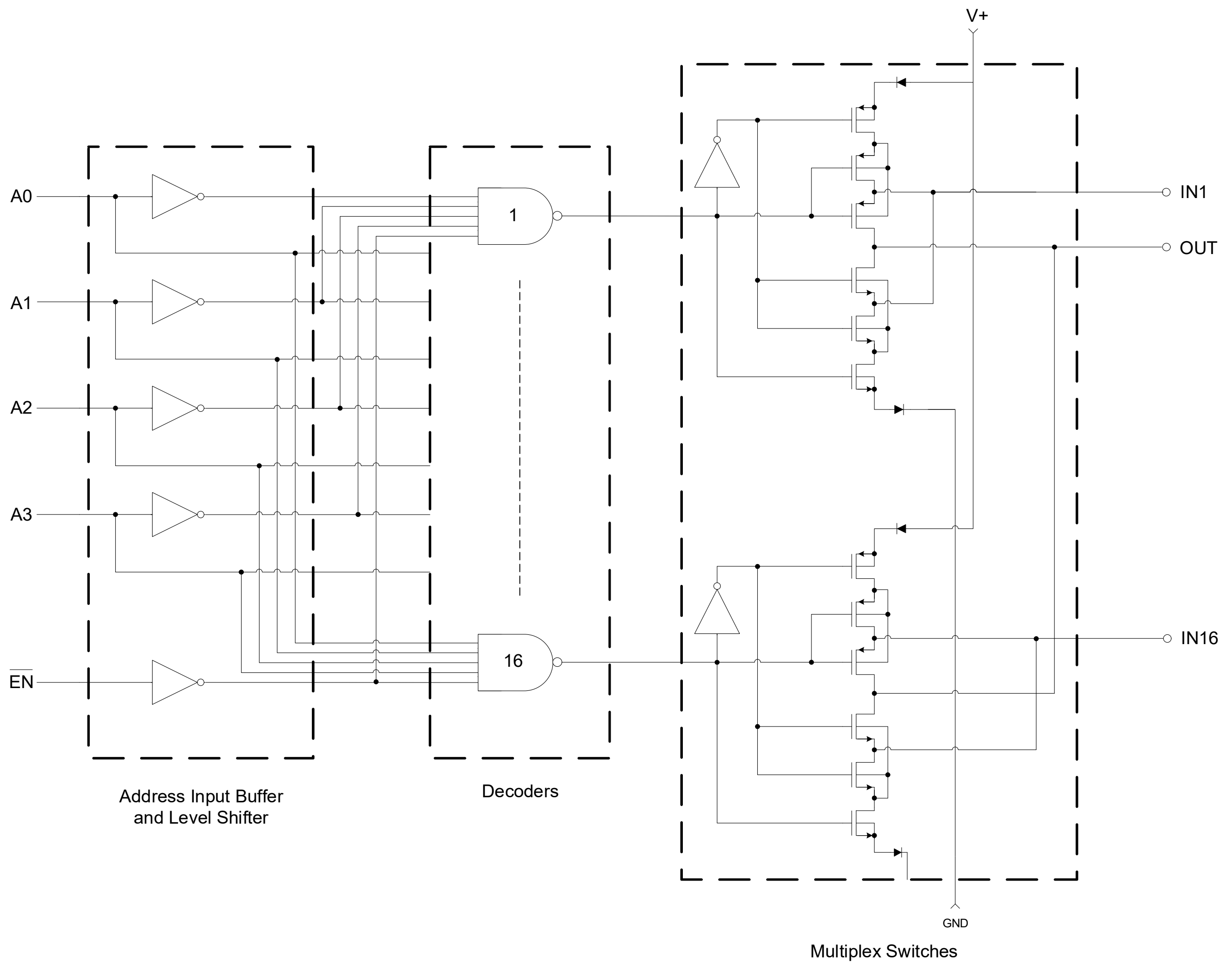


Figure 3. Block Diagram

2. Pin Information

2.1 Pin Assignments

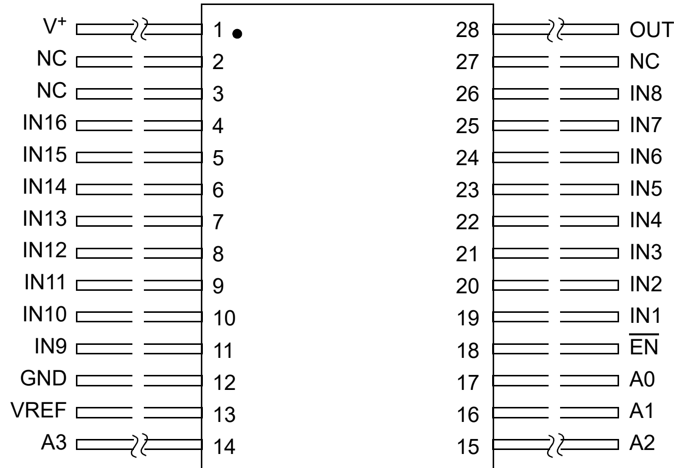
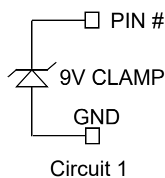
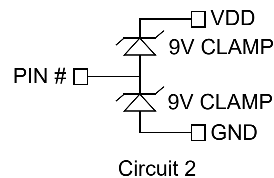


Figure 4. Pin Assignments (28 LD CDFP)-Top View

2.2 Pin Descriptions

Pin Name	Esd Circuit	Pin Number	Description
OUT	2	28	Output for multiplexer.
V+	1	1	Positive power supply.
NC	-	2, 3, 27	Not electrically connected.
INx	1	4, 5, 6, 7, 8, 9, 10, 11, 19, 20, 21, 22, 23, 24, 25, 26	Input for multiplexer.
Ax	1	14, 15, 16, 17	Address lines for multiplexer.
EN	1	18	Enable control for multiplexer (active low).
VREF	1	13	Reference voltage used to set logic thresholds.
GND	-	12	Ground
LID	-	-	Package lid is internally connected to GND (Pin 12).
 Circuit 1		 Circuit 2	

3. Specifications

3.1 Absolute Maximum Ratings

Caution: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Parameter	Minimum	Maximum	Unit
Maximum Supply Voltage (V+ to GND)	-	7	V
Maximum Supply Voltage (V+ to GND)[1]	-	6.5V	V
Analog Input Voltage Range (INx)	-0.4	7	V
Maximum Current Through a Selected Switch	-	10	mA
Peak Current Through a Selected Switch (Pulsed at 1ms, 10% Duty Cycle)	-	40	mA
Digital Input Voltage Range (EN, Ax)	GND - 0.4	V_{REF}	V
VREF to GND	-	7	V
Maximum Junction Temperature	-	+150	°C
Maximum Storage Temperature Range	-65	+150	°C
Human Body Model (Tested per MIL-STD-883 TM 3015)	-	5	kV
Charged Device Model (Tested per JESD22-C101D)	-	250	V
Machine Model (Tested per JESD22-A115-A)	-	250	V

1. Tested in a heavy ion environment at LET = 60MeV•cm2/mg at +125°C.

3.2 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Ambient Temperature	-55	+125	°C
Supply Voltage, V_{CC}	3	5.5	V
V_{REF} to GND	3	5.5	V

3.3 Thermal Specifications

Parameter	Package	Symbol	Conditions	Typical Value	Unit
Thermal Resistance	28 Ld CDFP	θ_{JA}[1]	Junction to ambient	55	°C/W
		θ_{JC}[2]	Junction to case	8.5	°C/W

1. θ_{JA} is measured with the component mounted on a high-effective thermal conductivity test board in free air. See TB379 for details.
2. For θ_{JC}, the case temperature location is the center of the package underside.

3.4 Electrical Specifications

3.4.1 $V^+ = 5V$

GND = 0V, V_{REF} = 3.3V, V_{IH} = 3.3V, V_{IL} = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Analog Input Signal Range	V_{IN}		0		V^+	V
Channel On-Resistance	$r_{DS(ON)}$	V^+ = 4.5V, V_{IN} = 0V to V^+ I_{OUT} = 1mA	-	40	**120**	Ω
$r_{DS(ON)}$ Match Between Channels	$\Delta r_{DS(ON)}$	V^+ = 4.5V, V_{IN} = 0V, 2.25V, 4.5V I_{OUT} = 1mA	-	-	**5**	Ω
On-Resistance Flatness	$r_{FLAT(ON)}$	V^+ = 4.5V, V_{IN} = 0V to V^+	-	-	**40**	Ω
Switch Input Off Leakage	$I_{IN(OFF)}$	V^+ = 5.5V, V_{IN} = 5V, Unused inputs and V_{OUT} = 0.5V	**-30**	-	**30**	nA
		V^+ = 5.5V, V_{IN} = 0.5V, Unused inputs and V_{OUT} = 5V	**-30**	-	**30**	nA
Switch Input Off Overvoltage Leakage	$I_{IN(OFF-OV)}$	V^+ = 5.5V, V_{IN} = 7V, Unused inputs and V_{OUT} = 0V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	-30	-	120	nA
		Post radiation, +25°C	-30	-	30	nA
Switch Input Off Leakage with Supply Voltage Grounded	$I_{IN(POWER-OFF)}$	V_{IN} = 7V, V_{OUT} = 0V V^+ = V_{EN} = V_{REF} = 0V, T_A = +25°C, -55°C	-20	-	20	nA
		T_A = +125°C	-20	-	50	nA
		Post radiation, +25°C	-20	-	20	nA
Switch Input Off Leakage with Supply Voltage Open	$I_{IN(POWER-OFF)}$	V_{IN} = 7V, V_{OUT} = 0V V^+ = V_{EN} = V_{REF} = Open, T_A = +25°C, -55°C	-20	-	20	nA
		T_A = +125°C	-20	-	50	nA
		Post radiation, +25°C	-20	-	20	nA
Switch On Input Leakage with Overvoltage Applied to the Input	$I_{IN(ON-OV)}$	V^+ = 5.5V, V_{IN} = 7V, V_{OUT} = OPEN	**2.75**	-	**5.50**	µA
Switch Output Off Leakage	$I_{OUT(OFF)}$	V^+ = 5.5V, V_{OUT} = 5V, All inputs = 0.5V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	0	-	150	nA
		Post radiation, +25°C	-30	-	30	nA
		V^+ = 5.5V, V_{OUT} = 0.5V, All inputs = 5V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	-60		30	nA
		Post radiation, +25°C	-30	-	30	nA

GND = 0V, V_{REF} = 3.3V, V_{IH} = 3.3V, V_{IL} = 0V, T_A = +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Test Conditions	Min[1]	Typ	Max[1]	Unit
Switch Output Leakage with Switch Enabled	$I_{OUT(ON)}$	V^+ = 5.5V, V_{IN} = V_{OUT} = 5V All unused inputs at 0.5V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	0	-	150	nA
		Post radiation, +25°C	-30	-	30	nA
		V^+ = 5.5V, V_{IN} = V_{OUT} = 0.5V All unused inputs at 5V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	-60	-	30	nA
		Post radiation, +25°C	-30	-	30	nA
Logic Input Voltage High/Low	$V_{IH/L}$	V^+ = 5.5V, V_{REF} = 3.3V	**1.3**	-	**1.6**	V
Input Current with V_{AH}, V_{ENH}	I_{AH}, I_{ENH}	V^+ = 5.5V, V_{EN} = V_A = V_{REF}	**-0.1**	-	**0.1**	µA
Input Current with V_{AL}, V_{ENL}	I_{AL}, I_{ENL}	V^+ = 5.5V, V_{EN} = V_A = 0V	**-0.1**	-	**0.1**	µA
Quiescent Supply Current	I_{SUPPLY}	V^+ = V_{REF} = V_{EN} = 5.5V V_A = 0V, T_A = +25°C, -55°C	-	-	100	nA
		T_A = +125°C	-	-	300	nA
		Post radiation, +25°C	-	-	300	nA
Reference Quiescent Supply Current	I_{REF}	V^+ = V_{REF} = V_{EN} = 5.5V V_A = 0V	-	-	**200**	nA
Dynamic						
Addressing Transition Time	t_{AHL}	V^+ = 4.5V; Figure 5	**10**	-	**70**	ns
Break-Before-Make Delay	t_{BBM}	V^+ = 4.5V; Figure 7	**5**	18	**40**	ns
Enable Turn-On Time	$t_{EN(ON)}$	V^+ = 4.5V; Figure 6	-	-	**40**	ns
Enable Turn-Off Time	$t_{EN(OFF)}$	V^+ = 4.5V; Figure 6	-	-	**40**	ns
Charge Injection	V_{CTE}	C_L = 100pF, V_{IN} = 0V, Figure 8	-	1.4	5	pC
Off Isolation	V_{ISO}	V_{EN} = V_{REF}, R_L = OPEN, f = 1kHz	**60**	-	-	dB
Crosstalk	V_{CT}	V_{EN} = 0V, f = 1kHz, V_{P-P} = 1V, R_L = OPEN	**73**	-	-	dB
Input Capacitance	$C_{IN(OFF)}$	f = 1MHz	-	-	**5**	pF
Output Capacitance	$C_{OUT(OFF)}$	f = 1MHz	-	-	**25**	pF

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

3.4.2 $V^+ = 3.3V$

V_{REF} = 3.3V, V_{IH} = 3.3V, V_{IL} = 0V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C.; over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Conditions	Min[1]	Typ	Max	Unit
Analog Input Signal Range	V_{IN}		0	-	V^+	V
Channel On-Resistance	$r_{DS(ON)}$	V^+ = 3V, V_{IN} = 0V to V^+ I_{OUT} = 1mA	**25**	70	**200**	Ω
$r_{DS(ON)}$ Match Between Channels	$\Delta r_{DS(ON)}$	V^+ = 3V, V_{IN} = 0.5V, 2.5V I_{OUT} = 1mA	-	-	**5**	Ω
On-Resistance Flatness	$r_{FLAT(ON)}$	V^+ = 3V V_{IN} = 0V to V^+	-	-	**50**	Ω
Switch Input Off Leakage	$I_{IN(OFF)}$	V^+ = 3.6V V_{IN} = 3.1V, Unused inputs and V_{OUT} = 0.5V	**-30**	-	**30**	nA
		V^+ = 3.6V V_{IN} = 0.5V, Unused inputs and V_{OUT} = 3.1V	**-30**	-	**30**	nA
Switch Input Off Overvoltage Leakage	$I_{IN(OFF-OV)}$	V^+ = 3.6V V_{IN} = 7V, Unused inputs and V_{OUT} = 0V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	-30	-	100	nA
		Post radiation, +25°C	-30	-	30	
Switch On Input Leakage with Overvoltage Applied to the Input	$I_{IN(ON-OV)}$	V^+ = 3.6V, V_{IN} = 7V, V_{OUT} = OPEN	**1.8**	-	**3.6**	μA
Switch Output Off Leakage	$I_{OUT(OFF)}$	V^+ = 3.6V, V_{OUT} = 3.1V, All inputs = 0.5V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	0	-	60	nA
		Post radiation, +25°C	-30	-	30	nA
		V^+ = 3.6V, V_{OUT} = 0.5V, All inputs = 3.1V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	0	-	30	nA
		Post radiation, +25°C	-30	-	30	nA

V_{REF} = 3.3V, V_{IH} = 3.3V, V_{IL} = 0V, T_A= +25°C, unless otherwise noted. **Boldface limits apply across the operating temperature range, -55°C to +125°C.; over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s. (Cont.)**

Parameter	Symbol	Conditions	Min[1]	Typ	Max	Unit
Switch Output Leakage with Switch Enabled	$I_{OUT(ON)}$	V^+ = 3.6V, V_{IN} = V_{OUT} = 3.1V All unused inputs at 0.5V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	0	-	30	nA
		Post radiation, +25°C	-30	-	30	nA
		V^+ = 3.6V, V_{IN} = V_{OUT} = 0.5V All unused inputs at 3.1V, T_A = +25°C, -55°C	-30	-	30	nA
		T_A = +125°C	0	-	30	nA
		Post radiation, +25°C	-30	-	30	nA
Quiescent Supply Current	I_{SUPPLY}	V^+ = V_{REF} = V_{EN} = 3.6V V_A = 0V, T_A = +25°C, -55°C	-	-	100	nA
		T_A = +125°C	-	-	300	nA
		Post radiation, +25°C	-	-	300	nA
Reference Quiescent Supply Current	I_{REF}	V^+ = V_{REF} = V_{EN} = 3.6V, V_A = 0V	-	-	**200**	nA
DYNAMIC						
Addressing Transition Time	t_{AHL}	V^+ = 3V; Figure 5	**10**	-	**100**	ns
Break-Before-Make Delay	t_{BBM}	V^+ = 3V; Figure 7	**5**	25	**50**	ns
Enable Turn-On Time	$t_{EN(ON)}$	V^+ = 3V; Figure 6	-	-	**50**	ns
Enable Turn-Off Time	$t_{EN(OFF)}$	V^+ = 3V; Figure 6	-	-	**50**	ns

1. Compliance to datasheet limits is assured by one or more methods: production test, characterization, and/or design.

Table 1. Truth Table[1]

A3	A2	A1	A0	EN	"ON" Channel
X	X	X	X	1	None
0	0	0	0	0	1
0	0	0	1	0	2
0	0	1	0	0	3
0	0	1	1	0	4
0	1	0	0	0	5
0	1	0	1	0	6
0	1	1	0	0	7
0	1	1	1	0	8
1	0	0	0	0	9
1	0	0	1	0	10
1	0	1	0	0	11
1	0	1	1	0	12

Table 1. Truth Table[1] (Cont.)

A3	A2	A1	A0	EN	"ON" Channel
1	1	0	0	0	13
1	1	0	1	0	14
1	1	1	0	0	15
1	1	1	1	0	16

1. X = Don't care, 1 = Logic High, 0 = Logic Low.

4. Timing Diagrams

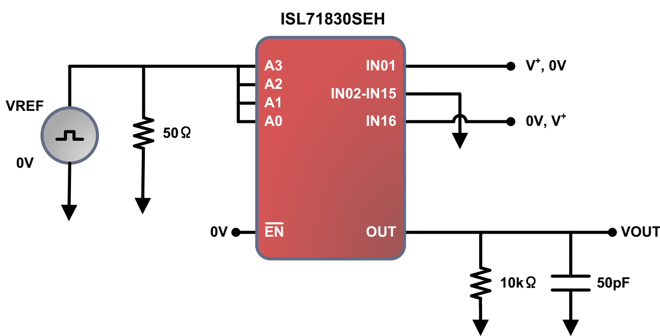


Figure 5. Address Time to Output Test Circuit

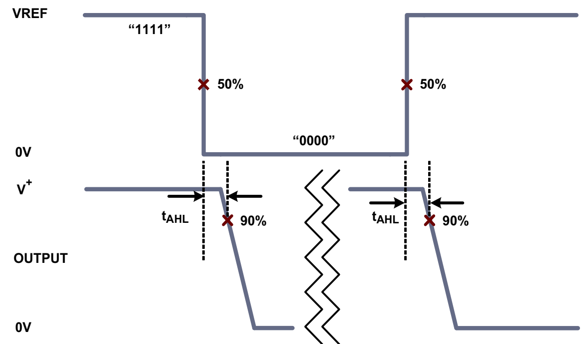


Figure 6. Address Time to Output Diagram

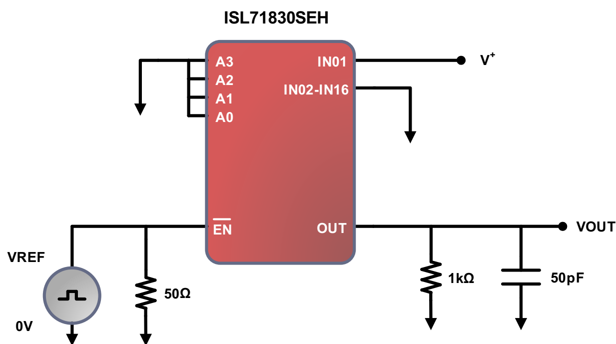


Figure 7. Time to Enable/Disable Output Test Circuit

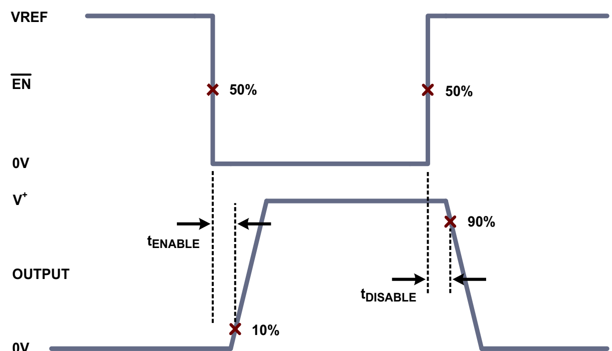


Figure 8. Time to Enable/Disable Output Diagram

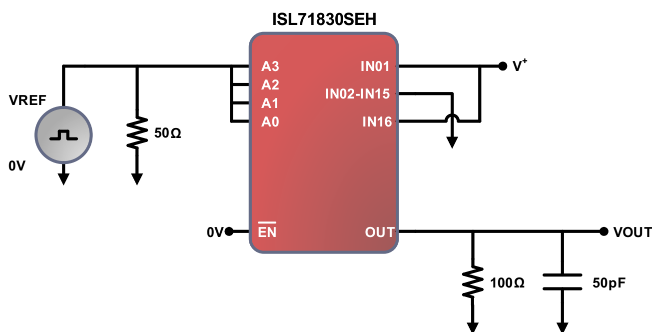


Figure 9. Break-Before-Make Test Circuit

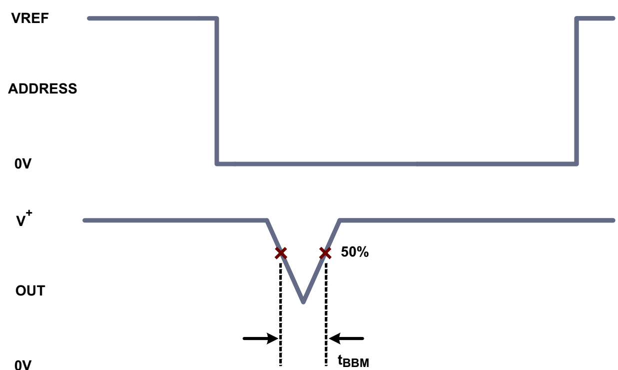


Figure 10. Break-Before-Make Diagram

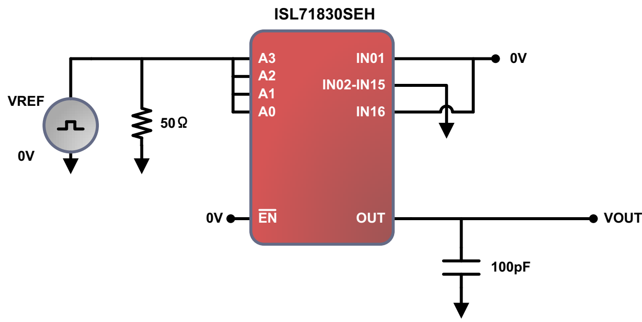


Figure 11. Charge Injection Test Circuit

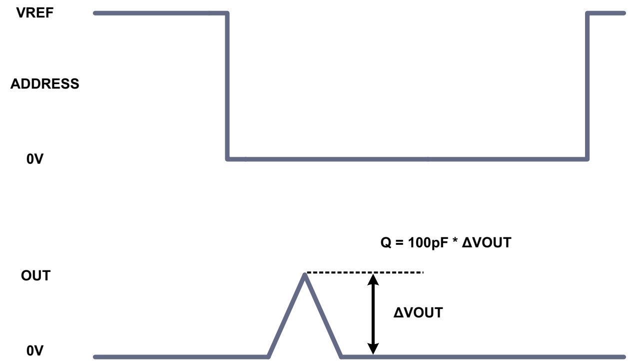


Figure 12. Charge Injection Diagram

5. Typical Performance Curves

V^+ = 5V, V_{REF} = 3.3V, V_{IN} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified.

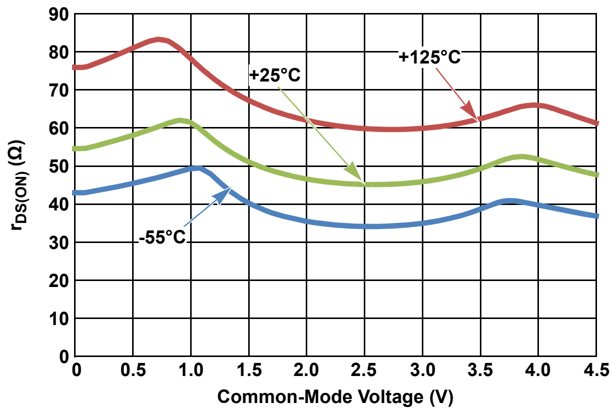


Figure 13. $r_{DS(ON)}$ vs Common-Mode Voltage (V^+ = 4.5V)

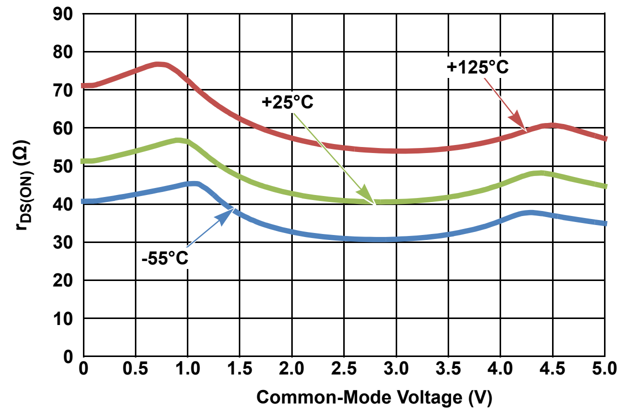


Figure 14. $r_{DS(ON)}$ vs Common-Mode Voltage (V^+ = 5V)

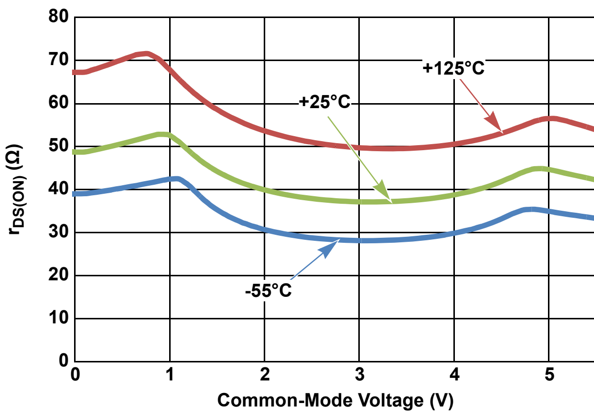


Figure 15. $r_{DS(ON)}$ vs Common-Mode Voltage (V^+ = 5.5V)

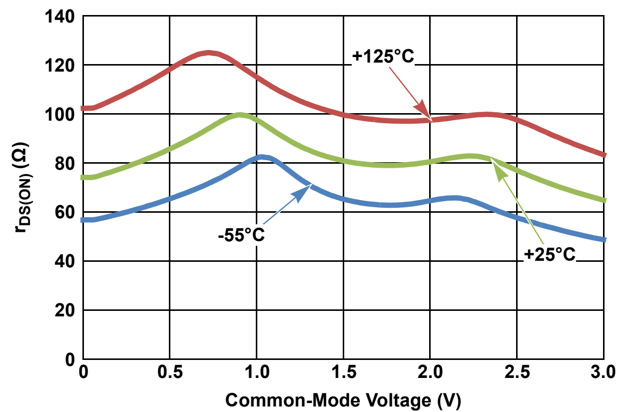


Figure 16. $r_{DS(ON)}$ vs Common-Mode Voltage (V^+ = 3V)

V^+ = 5V, V_{REF} = 3.3V, V_{IN} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. (Cont.)

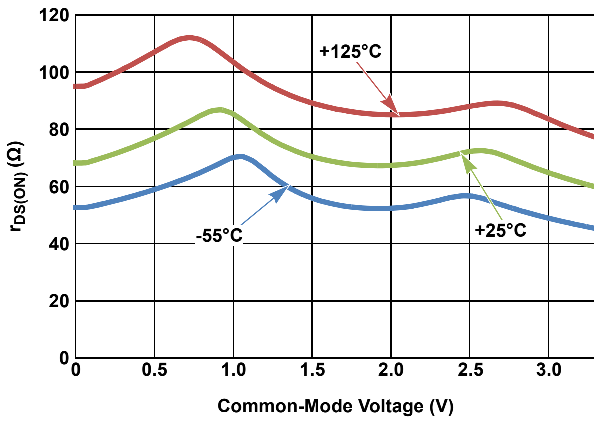


Figure 17. $r_{DS(ON)}$ vs Common-Mode Voltage (V^+ = 3.3V)

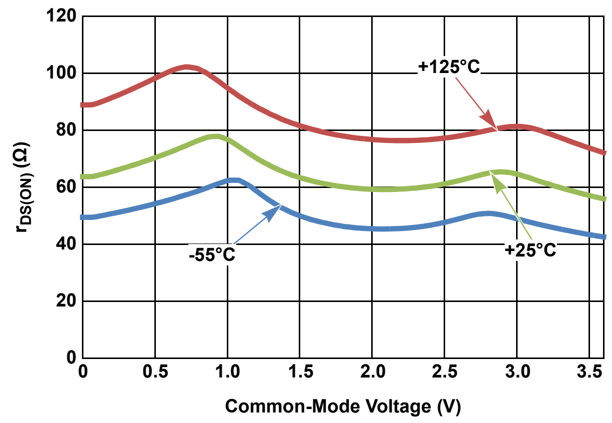


Figure 18. $r_{DS(ON)}$ vs Common-Mode Voltage (V^+ = 3.6V)

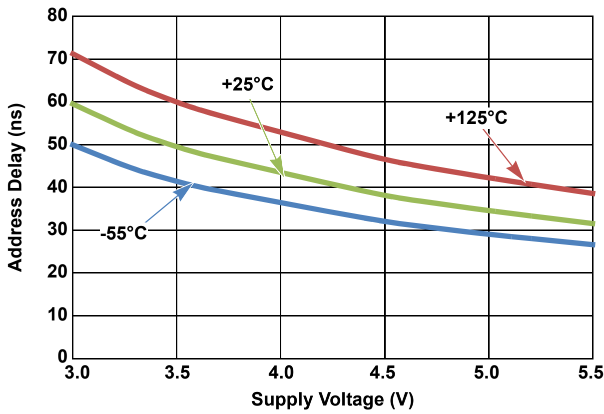


Figure 19. Address Propagation Delay (High to Low)

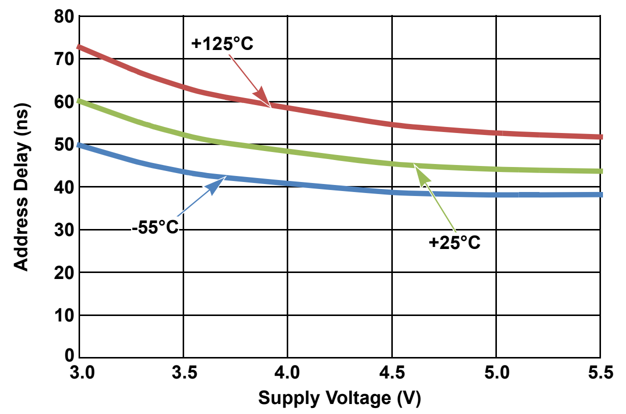


Figure 20. Address Propagation Delay (Low to High)

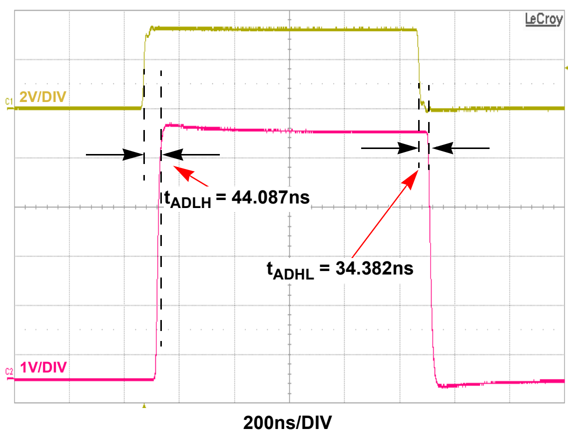


Figure 21. Address Propagation Delay

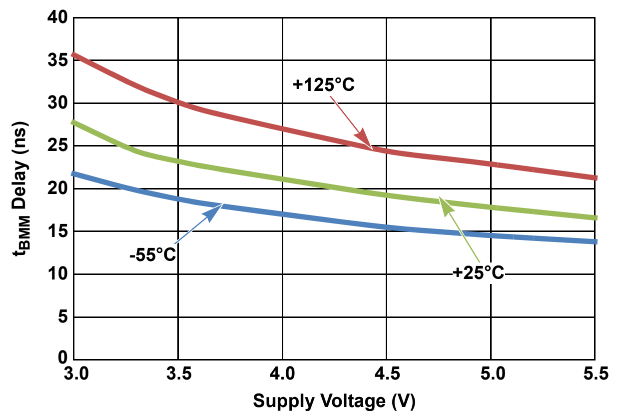


Figure 22. Break-Before-Make Delay

V^+ = 5V, V_{REF} = 3.3V, V_{IN} = 0V, R_L = Open, T_A = +25°C, unless otherwise specified. (Cont.)

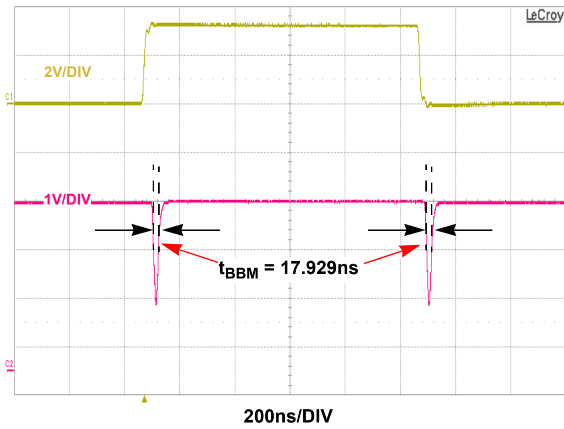


Figure 23. Break-Before-Make Delay

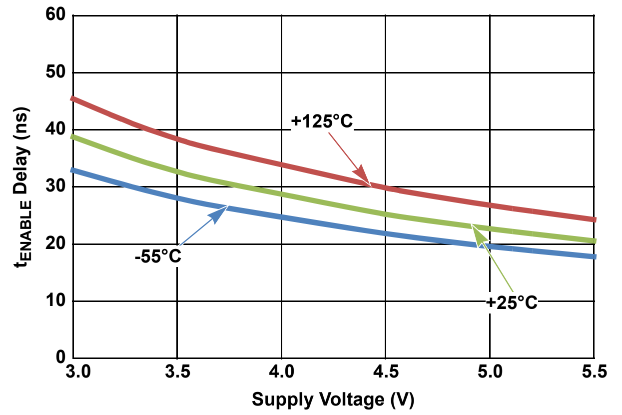


Figure 24. Enable to Output Propagation Delay

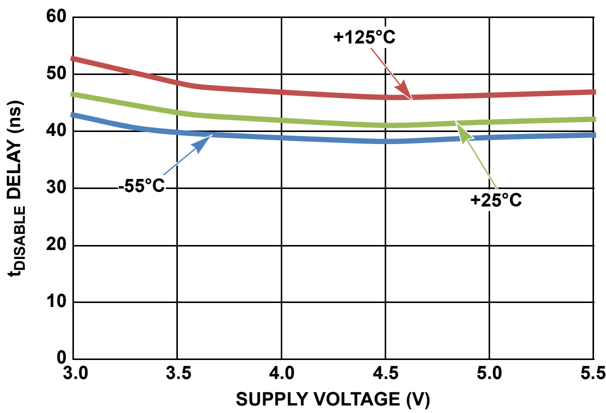


Figure 25. Disable to Output Propagation Delay

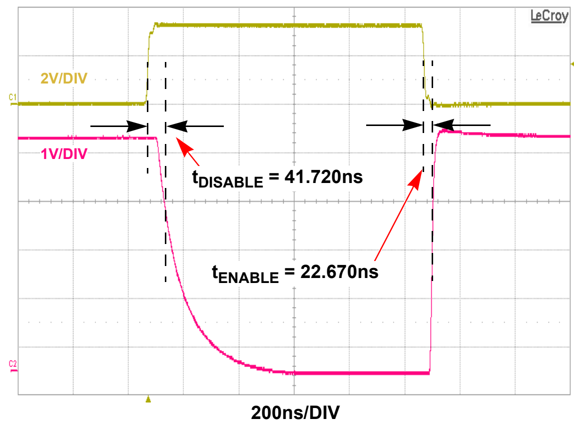


Figure 26. Enable/Disable Propagation Delay

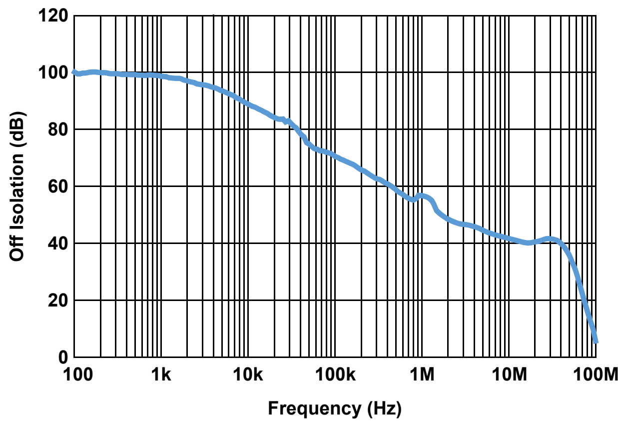


Figure 27. Off Isolation (V^+ = 5V, +25°C, R_L = 511Ω)

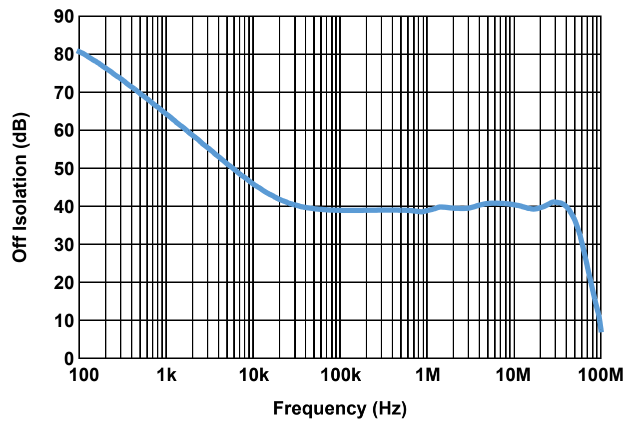


Figure 28. Off Isolation (V^+ = 5V, +25°C, R_L= OPEN)

$V^+ = 5V$, $V_{REF} = 3.3V$, $V_{IN} = 0V$, R_L = Open, $T_A = +25°C$, unless otherwise specified. (Cont.)

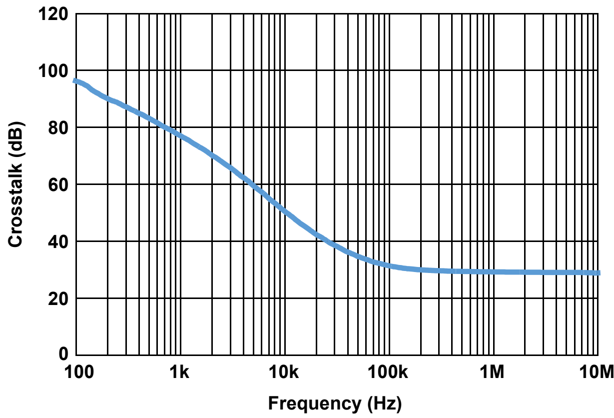


Figure 29. Crosstalk (V^+ = 5V, +25°C, R_L = OPEN)

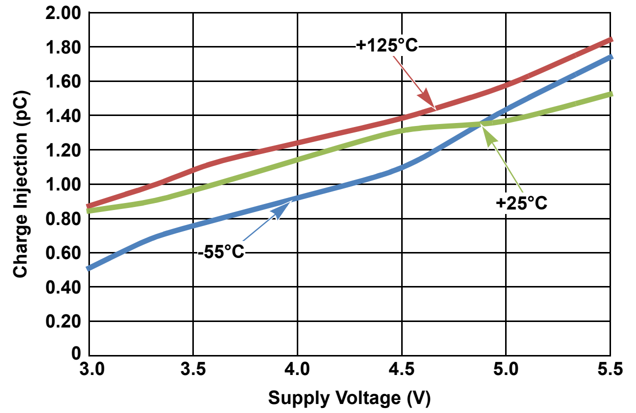


Figure 30. Charge Injection

6. Post Low Dose Rate Radiation Characteristics

6.1 V+ = 5V

Unless otherwise specified, $V^+ = 5V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed.

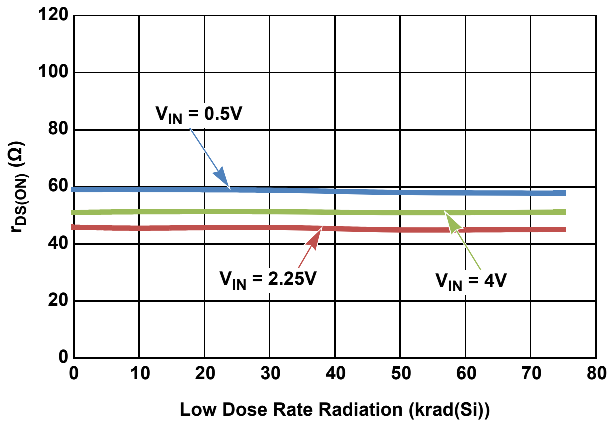


Figure 31. $r_{DS(ON)}$ (V^+ = 4.5V), Biased

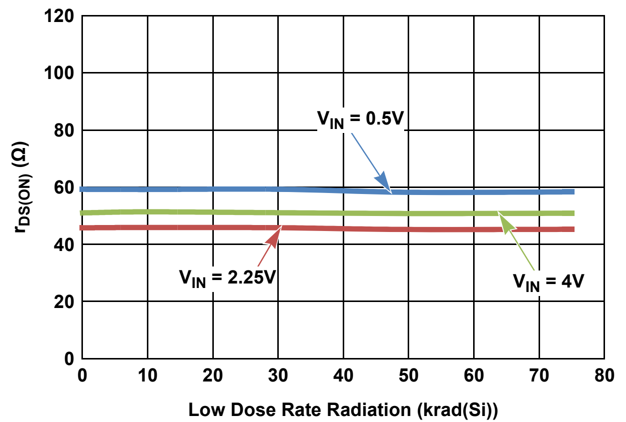


Figure 32. $r_{DS(ON)}$ (V^+ = 4.5V), Grounded

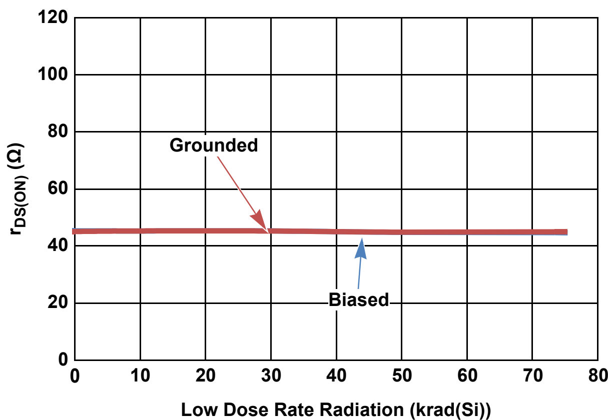


Figure 33. $r_{DS(ON)}$ Minimum (V^+ = 4.5V)

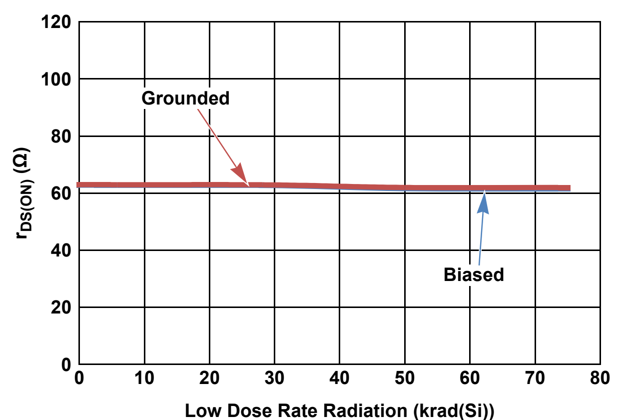


Figure 34. $r_{DS(ON)}$ Maximum (V^+ = 4.5V)

Unless otherwise specified, $V^+ = 5V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed.

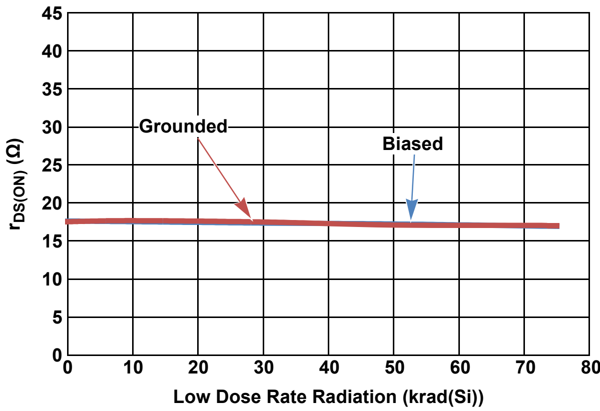


Figure 35. $r_{DS(ON)}$ Flatness ($V^+ = 4.5V$)

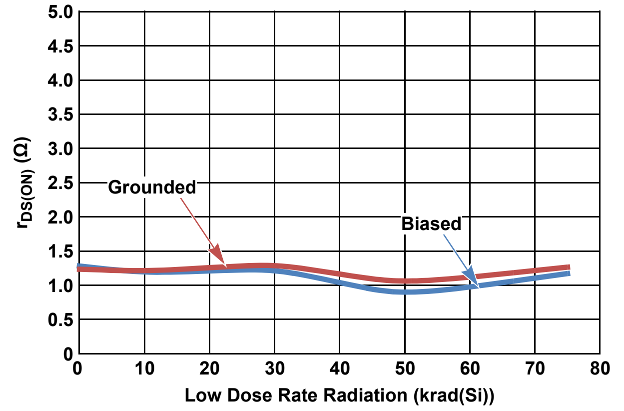


Figure 36. $r_{DS(ON)}$ Match ($V^+ = 4.5V$, $V_{IN} = 0.5V$)

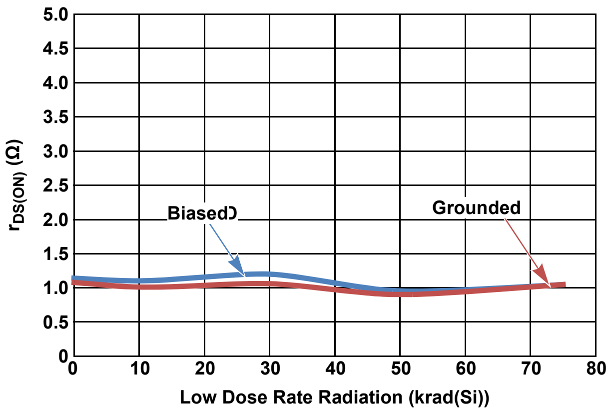


Figure 37. $r_{DS(ON)}$ Match ($V^+ = 4.5V$, $V_{IN} = 4V$)

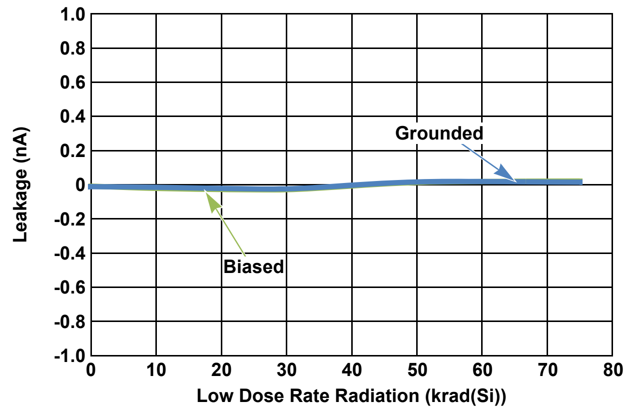


Figure 38. $I_{S(OFF)}$ ($V^+ = 5.5V$, $V_{IN} = 5V$)

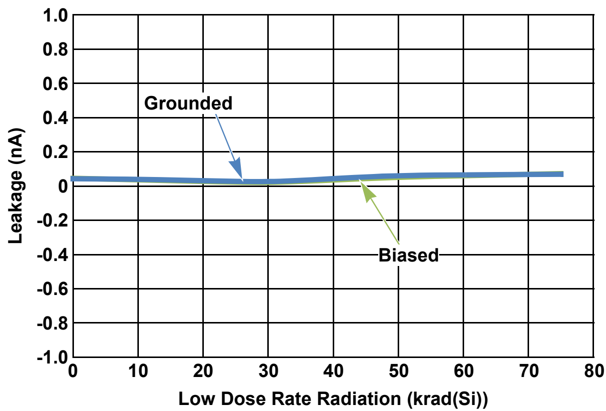


Figure 39. $I_{S(OFF)}$ ($V^+ = 5.5V$, $V_S = 7V$)

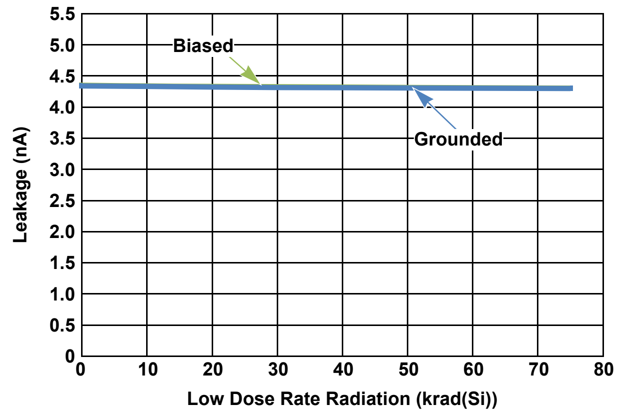


Figure 40. $I_{S(ON)}$ ($V^+ = 5.5V$, $V_{IN} = 5V$)

Unless otherwise specified, $V^+ = 5V$, $V_{CM} = 0$, $V_O = 0V$, $T_A = +25°C$. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed.

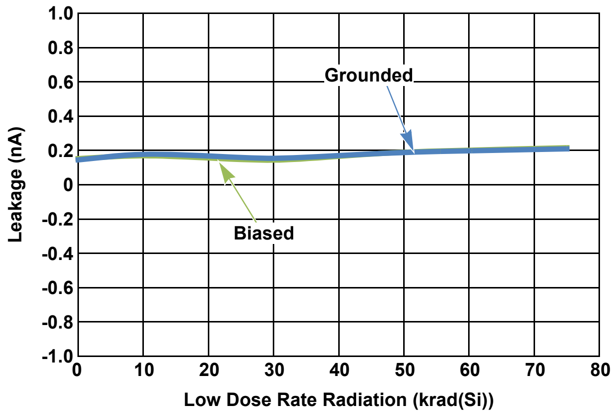


Figure 41. $I_{D(ON)}$ ($V^+ = 5.5V$, $V_{IN} = 5V$)

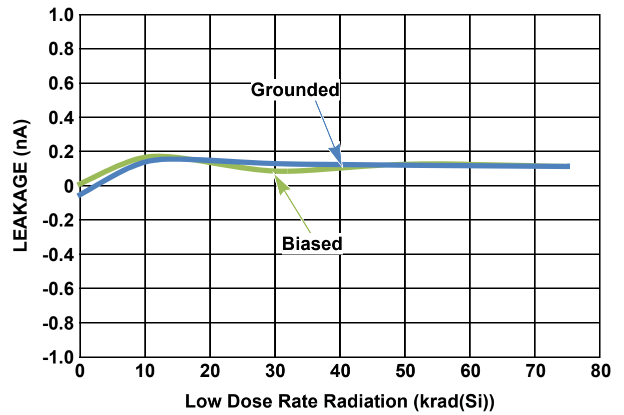


Figure 42. $I_{D(OFF)}$ ($V^+ = 3.6V$, $V_{IN} = 3.1V$)

6.2 $V^+ = 3.3V$

Unless otherwise specified, $V^+ = 3.3V$, $V_{CM} = 0$,$V_O = 0V$, $T_A = +25°C$. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed.

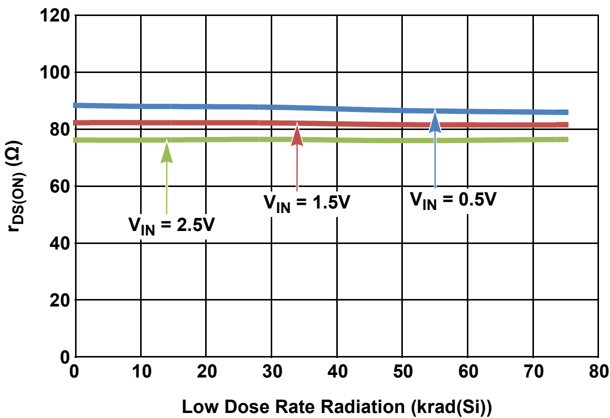


Figure 43. $r_{DS(ON)}$ ($V^+ = 3V$), Biased

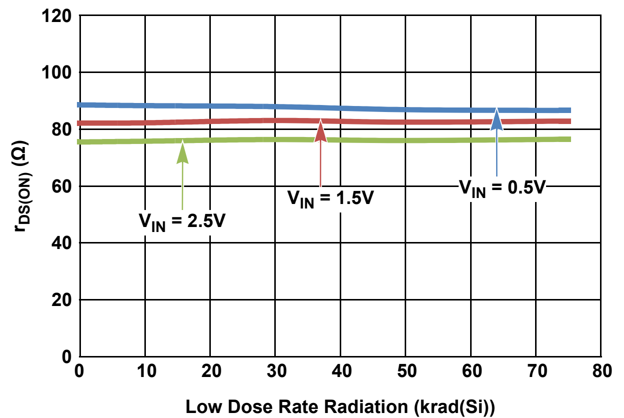


Figure 44. $r_{DS(ON)}$ ($V^+ = 3V$), Grounded

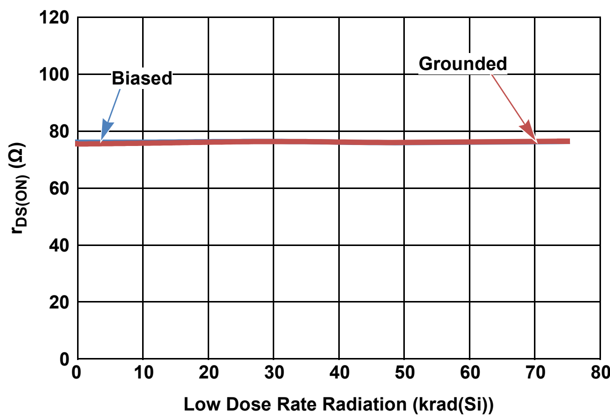


Figure 45. $r_{DS(ON)}$ Minimum ($V^+ = 3V$)

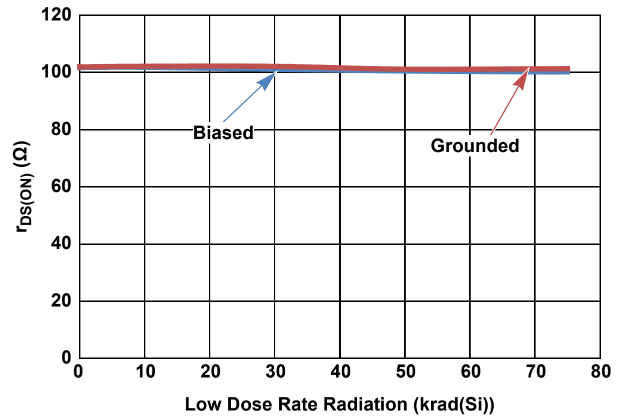


Figure 46. $r_{DS(ON)}$ Maximum ($V^+ = 3V$)

Unless otherwise specified, V^+ = 3.3V, V_{CM} = 0,V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed. (Cont.)

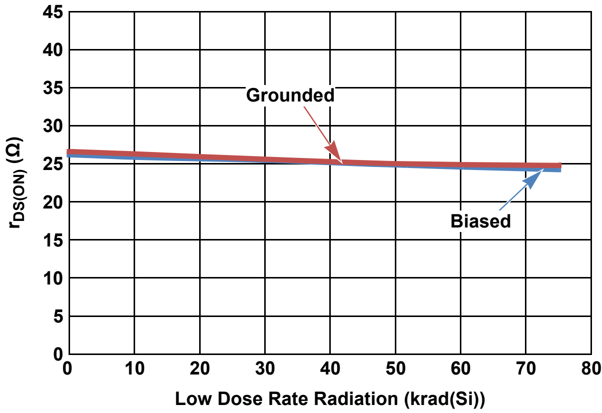


Figure 47. $r_{DS(ON)}$ Flatness (V^+ = 3V)

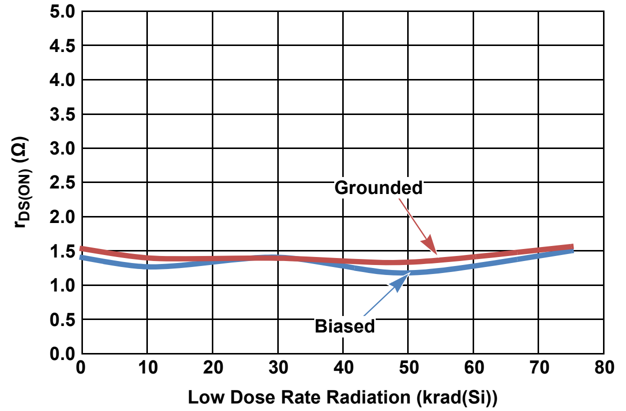


Figure 48. $r_{DS(ON)}$ Match (V^+ = 3V, V_{IN} = 0.5V)

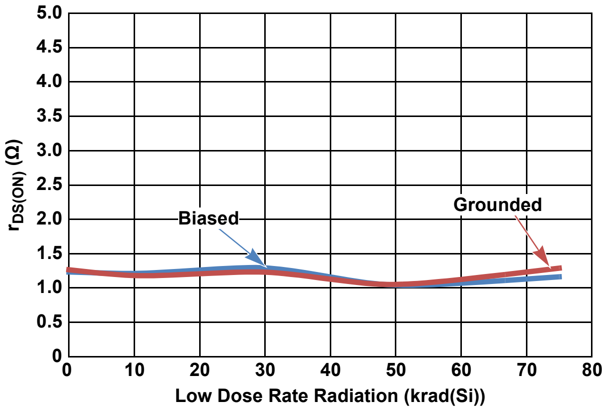


Figure 49. $r_{DS(ON)}$ Match (V^+ = 3V, V_{IN} = 2.5V)

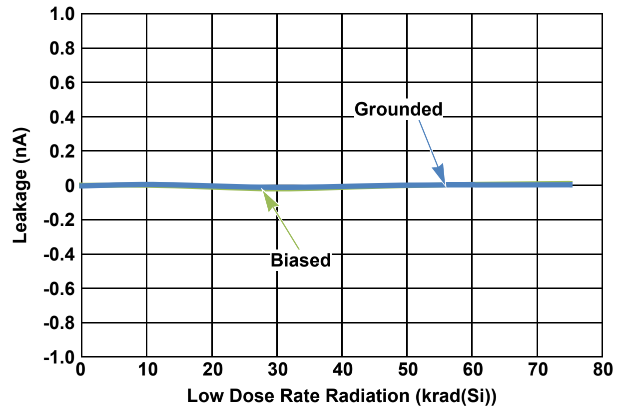


Figure 50. $I_{S(OFF)}$ (V^+ = 3.6V, V_{IN} = 3.1V)

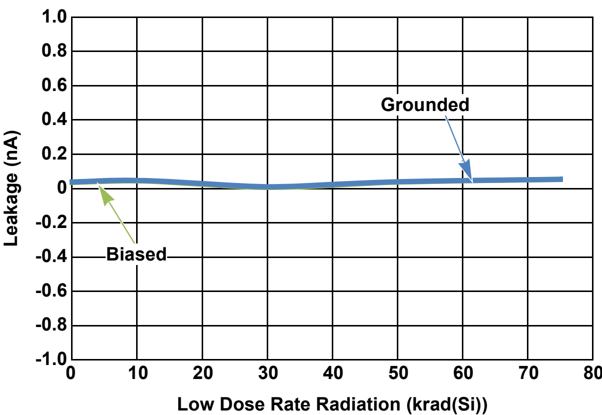


Figure 51. $I_{S(OFF)}$ (V^+ = 3.6V, V_{IN} = 7V)

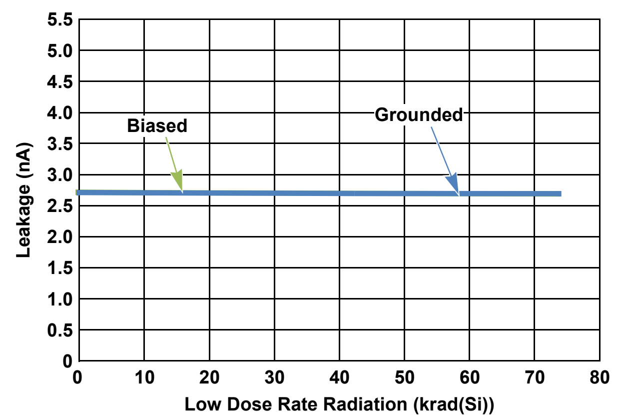


Figure 52. $I_{S(ON)}$ (V^+ = 3.6V, V_{IN} = 7V)

Unless otherwise specified, V^+ = 3.3V, V_{CM} = 0,V_O = 0V, T_A = +25°C. This data is typical mean test data post radiation exposure at a low dose rate of <10mrad(Si)/s. This data is intended to show typical parameter shifts due to low dose rate radiation. These are not limits nor are they guaranteed. (Cont.)

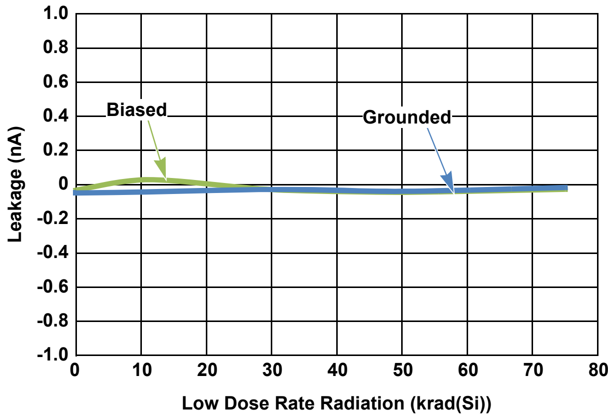


Figure 53. $I_{D(ON)}$ (V^+ = 3.6V, V_{IN} = 3.1V)

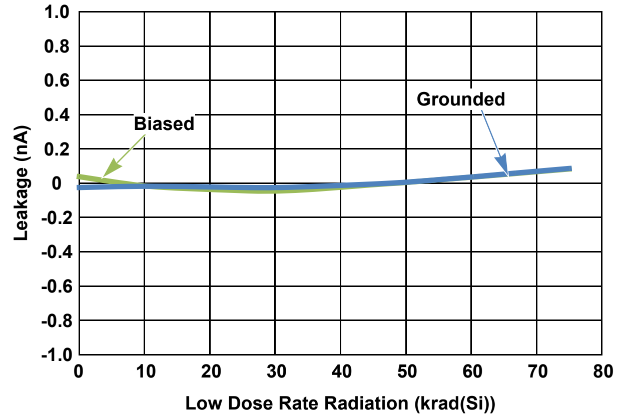


Figure 54. $I_{D(OFF)}$ (V^+ = 3.6V, V_{IN} = 3.1V)

7. Applications Information

7.1 Power-Up Considerations

The circuit is designed to be insensitive to any given power-up sequence between V^+ and VREF; however, it is recommended that all supplies power-up relatively close to each other.

7.2 Overvoltage Protection

The ISL71830SEH has overvoltage protection on both the input and the output. On the output, the voltage is limited to a diode past the rails. Each of the inputs has independent overvoltage protection that works regardless of the switch being selected. If a switch experiences an overvoltage condition, the switch is turned off. As soon as the voltage returns within the rails, the switch returns to normal operation.

7.3 VREF and Logic Functionality

The VREF pin sets the logic threshold for the ISL71830SEH. The range for VREF is between 3V and 5.5V. The switching point is set to around 44% of the voltage presented to VREF. This switching point allows for both 5V and 3.3V logic control.

7.4 Considerations for Redundant Applications

When using the ISL71830SEH in a cold sparing application, it is recommended to keep the ground pin connected to system ground at all times. Both supply pins (V^+ and VREF) should either be grounded or floating together.

If the supply pins are floating, it is recommended to place a high value bleed resistor (~1MΩ) in parallel with the decoupling caps on each supply pin to ensure that the supply voltage is discharged in a predictable manner. Figure 55 and Figure 56 illustrate the recommended cold sparing setup for both shorted and floating supplies.

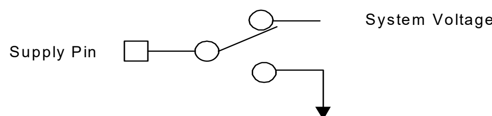


Figure 55. Cold Sparing Setup with Supplies Shorted

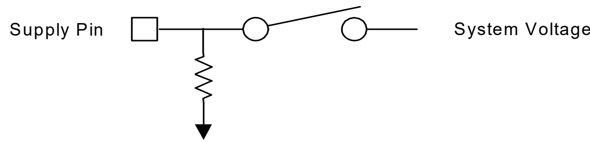


Figure 56. Cold Sparing Setup with Supplies Floating

7.5 ISL71830SEH vs ISL71831SEH

The ISL71831SEH, a 32-channel version of the ISL71830SEH, is available in a 48 Ld CQFP. The parts' performance specifications are very similar. Apart from the apparent increase in channel density, the ISL71831SEH has slightly higher output leakage compared to the ISL71830SEH because it has more channels connected to the output. The supply current for the ISL71831SEH is also slightly higher compared to the ISL71830SEH.

8. Die Characteristics

Table 2. Die and Assembly Related Information

Die Information	
Dimensions	2026µm × 2240µm (79.7638 mils × 88.1890 mils) Thickness: 483µm ±25µm (19 mils ±1 mil)
Interface Materials	
Glassivation	Type: 12kÅ Silicon Nitride on 3kÅ Oxide
Top Metallization	Type: 300Å TiN on 2.8µm AlCu In Bondpads, TiN has been removed.
Backside Finish	Silicon
Process	P6SOI
Assembly Information	
Substrate Potential	Floating
Additional Information	
Worst Case Current Density	1.6×10^5A/cm^2
Transistor Count	3875
Weight of Packaged Device	2.091 grams
Lid Characteristics	Finish: Gold Potential: Grounded, tied to package pin 12

9. Metalization Mask Layout

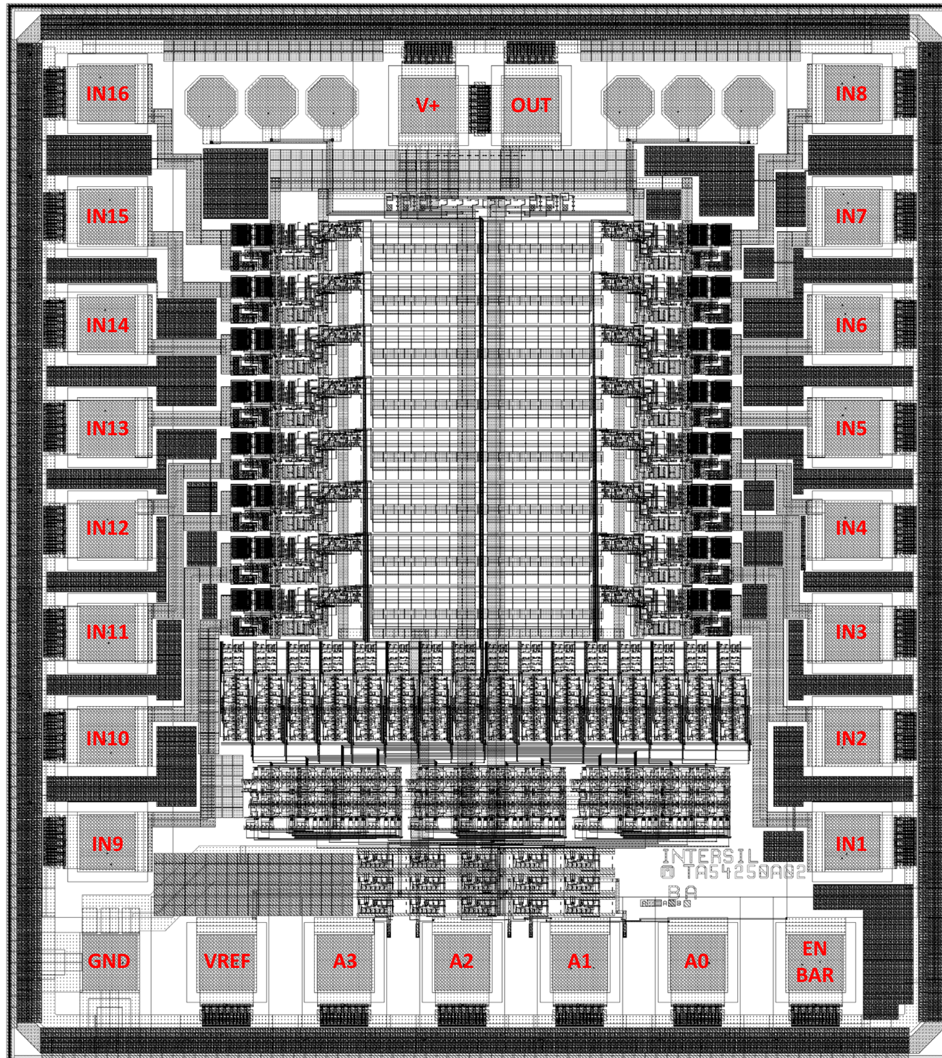


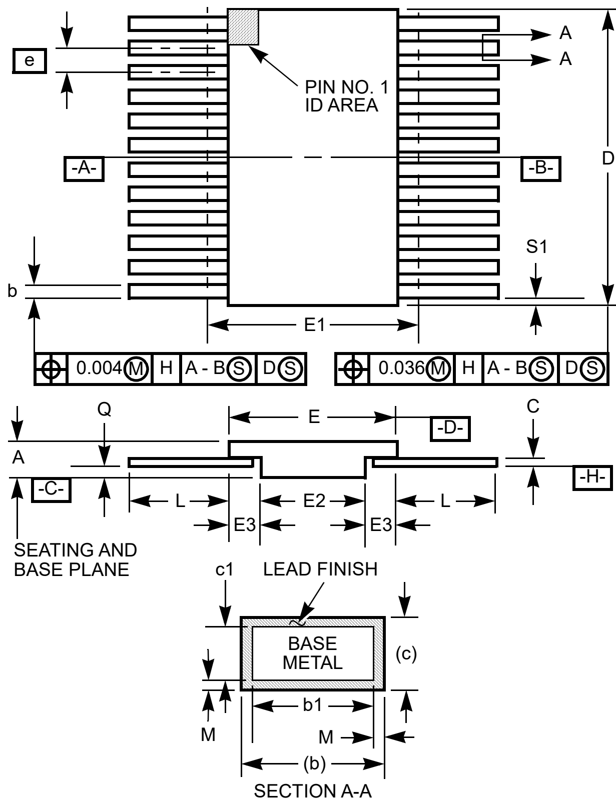
Table 3. ISL71830SEH Die layout X-Y Coordinates[1]

Pad Number	Pad Name	Packaging Pin	ΔX (µm)	ΔY (µm)	X (µm)	Y (µm)
1	IN8	P26	110	110	1693.925	1939.8
5	OUT	P28	110	110	1050.875	1915.8
6	V+	P1	110	110	844.875	1915.8
10	IN16	P4	110	110	201.8	1939.8
11	IN15	P5	110	110	201.8	1693.8
12	IN14	P6	110	110	201.8	1477.8
13	IN13	P7	110	110	201.8	1271.8
14	IN12	P8	110	110	201.8	1065.8
15	IN11	P9	110	110	201.8	859.8
16	IN10	P10	110	110	201.8	653.8
17	IN9	P11	110	110	201.8	442.8
18	GND	P12	110	110	206.225	201.8
19	VREF	P13	110	110	440.35	201.8
20	A3	P14	110	110	676.35	201.8
21	A2	P15	110	110	912.35	201.8
22	A1	P16	110	110	1148.35	201.8
23	A0	P17	110	110	1384.35	201.8
24	EN	P18	110	110	1620.35	201.8
25	IN1	P19	110	110	1693.925	442.8
26	IN2	P20	110	110	1693.925	653.8
27	IN3	P21	110	110	1693.925	859.8
28	IN4	P22	110	110	1693.925	1065.8
29	IN5	P23	110	110	1693.925	1271.8
30	IN6	P24	110	110	1693.925	1477.8
31	IN7	P25	110	110	1693.925	1693.8

1. Origin of coordinates is the bottom left of the die, near Pad 18.

10. Package Outline Drawing

For the most recent package outline drawing, see K28.A.



K28.A MIL-STD-1835 CDFP3-F28 (F-11A, CONFIGURATION B)
28 lead ceramic metal seal flatpack package

Symbol	Inches		Millimeters		Notes
	Min	Max	Min	Max	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.740	-	18.80	3
E	0.460	0.520	11.68	13.21	-
E1	-	0.550	-	13.97	3
E2	0.180	-	4.57	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.250	0.370	6.35	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.00	-	0.00	-	6
M	-	0.0015	-	0.04	-
N	28		28		-

Rev. 0 5/18/94

Notes:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

11. Ordering Information

SMD Ordering[1] Number	Part Number[2]	Radiation Hardness (Total Ionizing Dose)	Package Description (RoHS Compliant)	PKG. DWG. #	Temp. Range
5962L1524701VXC	ISL71830SEHVF	LDR to 75krad(Si)	28 Ld CDFP	K28.A	-55 to +125°C
5962L1524701V9A	ISL71830SEHVX[3]		Die	N/A	
N/A	ISL71830SEHF/PROTO[4]	N/A	28 Ld CDFP	K28.A	
N/A	ISL71830SEHX/SAMPLE[3][4]		Die	N/A	
N/A	ISL71830SEHEV1Z[5]	Evaluation Board			

1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the Ordering Information table must be used when ordering.
2. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
3. Die product tested at T_A = + 25°C. The wafer probe test includes functional and parametric testing sufficient to make the die capable of meeting the electrical performance outlined in V^+ = 5V or V^+ = 3.3V.
4. The /PROTO and /SAMPLE are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO parts meet the electrical limits and conditions across temperature specified in the DLA SMD and are in the same form and fit as the qualified device. The /SAMPLE parts are capable of meeting the electrical limits and conditions specified in the DLA SMD. The /SAMPLE parts do not receive 100% screening across temperature to the DLA SMD electrical limits. These part types do not come with a Certificate of Conformance because they are not DLA qualified devices.
5. The evaluation board uses the /PROTO parts. The /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Table 4. Key Differences Between Family of Parts

Part Number	Number of Channels	Output Leakage	Package
ISL71831SEH	32	120nA	48 Ld CQFP
ISL71830SEH	16	60nA	28 Ld CDFP

12. Revision History

Revision	Date	Change
8.01	Jan 16, 2025	Added Maximum Current Through a Selected Switch and Peak Current Through a Selected Switch specs to abs max section.
8.00	Sep 14, 2023	Added Block Diagram. Applied new template formatting.
7.00	Dec 8, 2022	Updated Switch Output Leakage with Switch Enabled maximum specification from 0 to 30nA for the 125C temperature.
6.00	Nov 11, 2022	Updated Switch Output Off Leakage maximum specification from 0 to 30nA for the 125C temperature.
5.01	Sep 8, 2022	Removed Related Literature section. Updated Ordering Information table formatting. Added Note 3 and updated Note 4. In “VREF and Logic Functionality”, changed the switching point from 50% to 44%.
5.00	Mar 27, 2018	Added Notes 4 and 5 to the Ordering Information table. Added “Considerations for Redundant Applications” section. Removed About Intersil section and added Renesas disclaimer.

Revision	Date	Change
4.00	Feb 6, 2017	Updated the note on Table 3.
3.00	Nov 18, 2016	Added ESD diagrams to the “Pin Descriptions”. Updated Related Literature section.
2.00	Mar 4, 2016	Page 1 Features, changed the following: From: SEL/B immune to LET 60MeV•mg/cm^2 To: SEL/B immune to LET 60MeV•cm^2/mg
1.00	Dec 10, 2015	Changed r_{ON} to $r_{DS(ON)}$ throughout datasheet Changed in Features on page 1 last item under “Radiation tolerance” “V^+ = 5V” to “V^+ = 6.5V” Changed in Description and Features on page 1 supply voltage from “3.3V to 5V” to “3V to 5.5V”. Removed ADDR throughout datasheet from: Pin Configuration from pins 14 through 17 on page 4 “Pin Descriptions”, “Absolute Maximum Ratings”, and Table 3. Abs Max Section, changed: Maximum Supply Voltage (V+ to GND) (Note 5) . . . . . . 7V TO: Maximum Supply Voltage (V+ to GND) (Note 5) . . . . . 6.5V Electrical Spec table: Changed TYP from 60 to 40 t_{BBM} changed TYP from 15 to 18 V_{CTE} changed TYP from 2 to 1.4 Swapped the "VEN = " statements between Off Isolation and Crosstalk. Off Isolation changed: From: 60dB (TYP) To: 60dB (MIN) and Crosstalk changed: From: 73dB (TYP) To: 73dB (MIN) Changed TYP from 60 to 70 tBBM changed TYP from 15 to 25 “Timing Diagrams” Figures 6 and 8 changed 500 to 50Ω Added Truth table. Replaced die plot, changed VDD to V+. X-Y Coordinates table, changed VDD to V+ Figure 8 changed 1000 on bottom right resistor to 100Ω. Y-Axis Changes: Figure 20: from ADDRESS DELAY (ns) to: t_{BMM} DELAY (ns) Figure 22: from ADDRESS DELAY (ns) to: t_{ENABLE} DELAY (ns) Figure 23: from ADDRESS DELAY (ns) to: $t_{DISABLE}$ DELAY (ns)
0.00	Sep 24, 2015	Initial Release

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