White Paper

Radiation Hardened Load Switches Simplify Redundancy and Increase Reliability in Space Grade Power Systems

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Introduction

In space applications there is always a need to prevent against single-point of failures. Elimination of single point of failures is even more critical in power distribution systems where propagation of a failure could lead to loss of functionality, or even worse, complete destruction of the payload or satellite bus.

Figure 1 shows a simplified block diagram of a satellite distribution power architecture (DPA). The basic DPA system consists of an isolated intermediate bus converter (IBC) and two or more non-isolated point of load (POL) voltage regulators that provide the regulated supply voltages to power the various satellite payload modules. The module loads have varying voltage and current requirements. New digital devices (FPGA and ASIC) require lower supply voltages (0.9V, 1V, 1.2V, 1.8V, 1.5V, 2.5V, 3.3V, and 5V) and higher operating currents (5A to 10A or more).

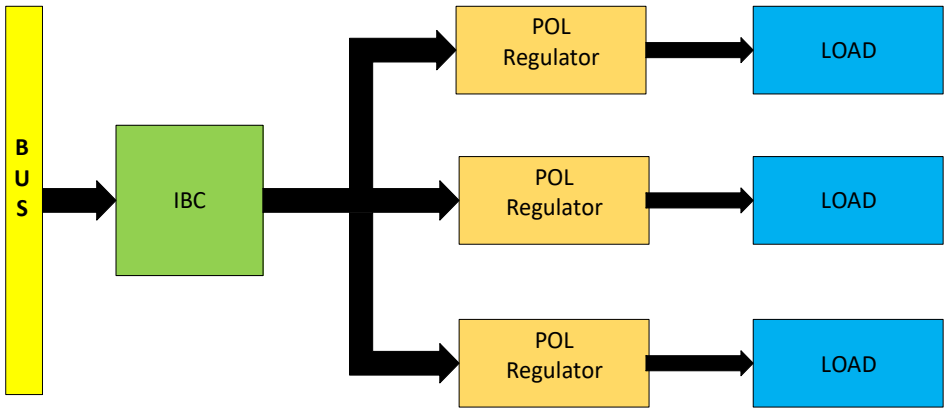

Figure 1. *Block diagram of a satellite distributed power architecture*

The DPA system components must be robust, reliable, and must be able to handle the extreme environment of space. Components need to meet the functional and performance requirements for the life of the mission. For highly critical systems, redundant (backup) is implemented to take over when the primary payload module or its power rail experience a failure. Current satellite power architectures use an external MOSFET or diode to add redundancy and increase the reliability of the power distribution unit; however, using these devices has some drawbacks such as additional complex gate drive circuitry, substantial increase in the size of the power distribution unit, and unnecessary power loss.

This white paper will introduce the new Renesas ISL7x061SEH (PMOS) and ISL7x062SEH (NMOS) radiation hardened load switch ICs, and discuss using the load switches with the ISL70001ASEH radiation hardened 6A synchronous buck POL regulator ICs to implement POL system redundancy. A “Full Redundant Application” and a “Redundant Source Application” will be presented, and we will also discuss the paralleling of two load switches for applications requiring greater than 10A of current or when the IR voltage drop needs to be reduced.

Renesas Load Switches

The new family of Intersil load switch ICs by Renesas were designed for use in satellite power supply POL switching applications to simplify the design of power distribution, sequencing, and redundant (backup) systems. The family consists of the ISL7x061SEH PMOS devices and the ISL7x062SEH NMOS devices.

These load switches are radiation hardened, single channel, unidirectional SPST power switches with ultra-low r_{ON} and high current capability up to 10A. The parts feature a simple ON/OFF digital logic control input that can interface directly to low voltage control signals from FPGA, MCU, or processor. Additional features include reverse current protection (RCP), turn-on slew rate control, selectable MOSFET to discharge the output, and Undervoltage Lockout (UVLO) protection.

Figure 2 shows the block diagrams for the ISL7x061SEH PMOS and the ISL7x062SEH NMOS load switches.

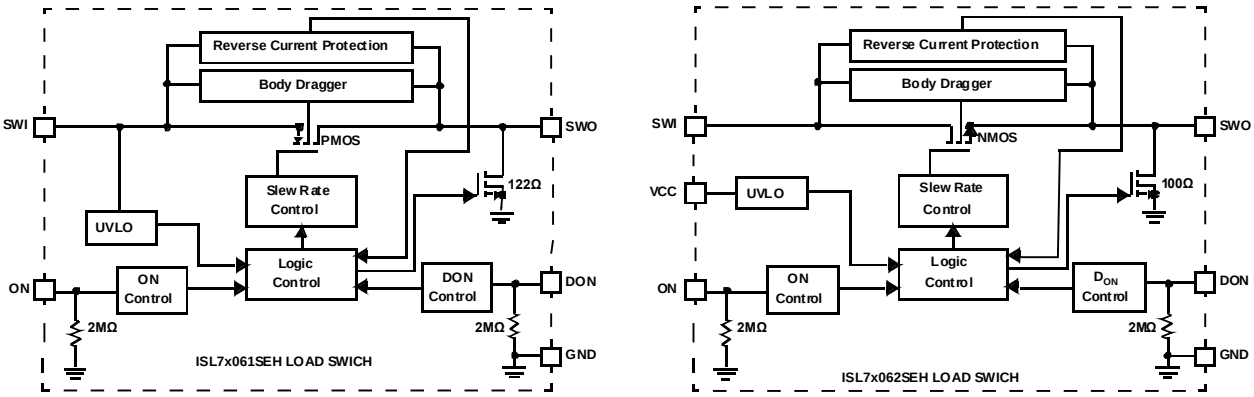

Figure 2. *Renesas load switch block diagrams*

The ISL7x061SEH ICs use a PMOS pass device as the main switch with a simple logic input to turn the pass device on or off. The devices are capable of 10A continuous current with a typical r_{ON} of 14mΩ with V_{SWI} = 5.5V and 16mΩ with V_{SWI} = 3.0V. The input voltage (V_{SWI}) range is 3V to 5.5V and an internal UVLO keeps the devices in an OFF state when the V_{SWI} is < 2.2V (typical). The devices feature internal controlled rise time to reduce inrush current. The ISL7x061SEH incorporate reverse current protection when the output voltage (V_{SWO}) increases above the V_{SWI} voltage. Additionally, there is a selectable 122Ω MOSFET between SWO and GND to discharge the output when the main pass device is OFF. When the DON logic input = High, the discharge FET circuitry is enabled. The ISL70061SEH is radiation acceptance tested on a wafer by wafer basis to 75krad (Si) at LDR and 100krad (Si) at HDR, while the ISL730061SEH is acceptance tested on a wafer by wafer basis to 75krad (Si) at LDR only.

The ISL7x062SEH ICs use a NMOS pass device as the main switch with a simple logic input to turn the pass device on or off. These devices are capable of 10A continuous current with a typical r_{ON} of 25mΩ with V_{CC} = 5.5V and V_{SWI} = 3.5V, and a typical r_{ON} of 16mΩ with V_{CC} = 5.5V and V_{SWI} = 1.0V. The devices have a VCC pin to power the logic and drivers of the device, allowing the switching of low voltage levels. VCC voltage range is 3V to 5.5V, and an internal UVLO keeps the device OFF when V_{CC} < 2.3V (typical). The recommended input voltage (V_{SWI}) range of the devices is 0V to (VCC - 2V). The devices feature internal controlled rise time to reduce inrush current. The ISL7x062SEH incorporate reverse current protection when the output voltage (V_{SWO}) increases above the V_{SWI} voltage. Additionally, there is a selectable 100Ω MOSFET between SWO and GND to discharge the output when the main pass device is OFF. When the DON logic input = High, the discharge FET circuitry is enabled. The ISL70062SEH is radiation acceptance tested on a wafer by wafer basis to 75krad (Si) at LDR and 100krad (Si) at HDR while the ISL730062SEH is acceptance tested on a wafer by wafer basis to 75krad (Si) at LDR only.

Full Redundancy Application

Figure 3 shows a block diagram of a full redundant configuration using two ISL70061SEH load switches with two ISL7001ASEH 6A synchronous buck POL regulators. This configuration can accept a 3V to 5.5V voltage rail at its input and the buck regulators can be set to apply a voltage to the loads in the range of 0.8V to 0.85% of the input supply. The diagram shows an example of the input rail at 5V, with the load rails set at 2.5V.

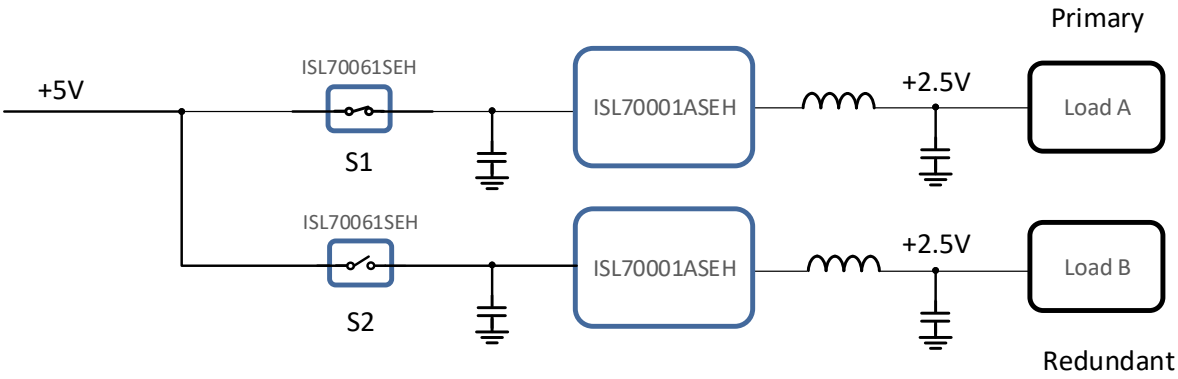

Figure 3. *Block diagram of a full redundant configuration*

Load A and Load B are identical and the power supply circuit feeding each of them are identical. Load A is designated as the primary load and load B is designated as the redundant (backup) load. Power is supplied to the primary load (A) when the load switch (S1) in the primary branch is turned ON, as shown in the diagram. Power to the redundant load (B) is applied when the load switch (S2) in the redundant branch is turned ON.

During normal operation, the primary circuit will be active (S1 → ON) and the redundant (backup) circuit will be inactive (S2 → OFF). If for any reason the primary load malfunctions or its supply regulator enters a fault condition, the power to the primary load can be disconnected by turning the S1 load switch OFF. Cutting the input voltage at the primary POL regulator will shut down the supply voltage at the primary load (A). Then the redundant (backup) load (B) can be brought online by providing power through turning the S2 load switch ON.

Figure 4 shows a picture of a lab setup using two ISL70061SEH load switch evaluation boards and two ISL70001ASEH buck regulator evaluation boards connected in a full redundant load configuration. A power supply (not shown) of +5V is connected to the input of the load switches. Each regulator output is tied to a 1Ω load resistor to ground and their output voltage is set at 2.5V. A break-before-make SPDT switch (not shown) is being used to drive the ON logic control pins of the load switches to switch between the two redundant loads. The SPDT switch in the lab setup mimics the monitoring and control function of the power distribution unit. In many applications this function is realized by using a microcontroller or a field programmable gate array (FPGA).

The oscilloscope plots in Figure 4 show the voltage and current waveforms when switching between the two redundant loads. The red trace (VPOL_Primary) and green trace (IPOL_Primary) are the voltage and current into the primary 1Ω load. The blue trace (VPOL_Redundant) and cyan trace (IPOL_Redundant) are the voltage and current into the backup 1Ω load.

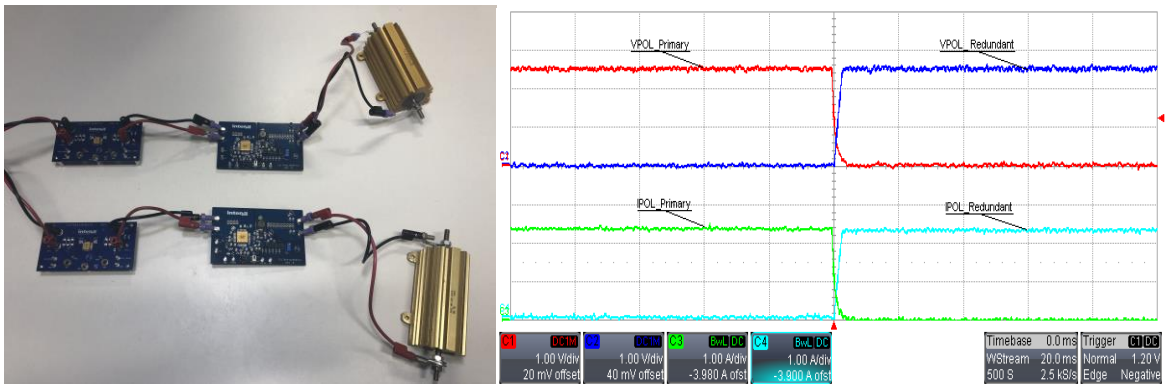

Figure 4. *Full Redundancy setup using evaluation boards, oscilloscope voltage, and current waveforms*

Figure 5 shows the oscilloscope plots of the voltage and current waveforms with the primary output shorted to ground. As can be seen, the regulator goes into hiccup mode. Then the logic to the load switches are toggled to turn the power OFF to the shorted load and to turn the power ON to the backup load.

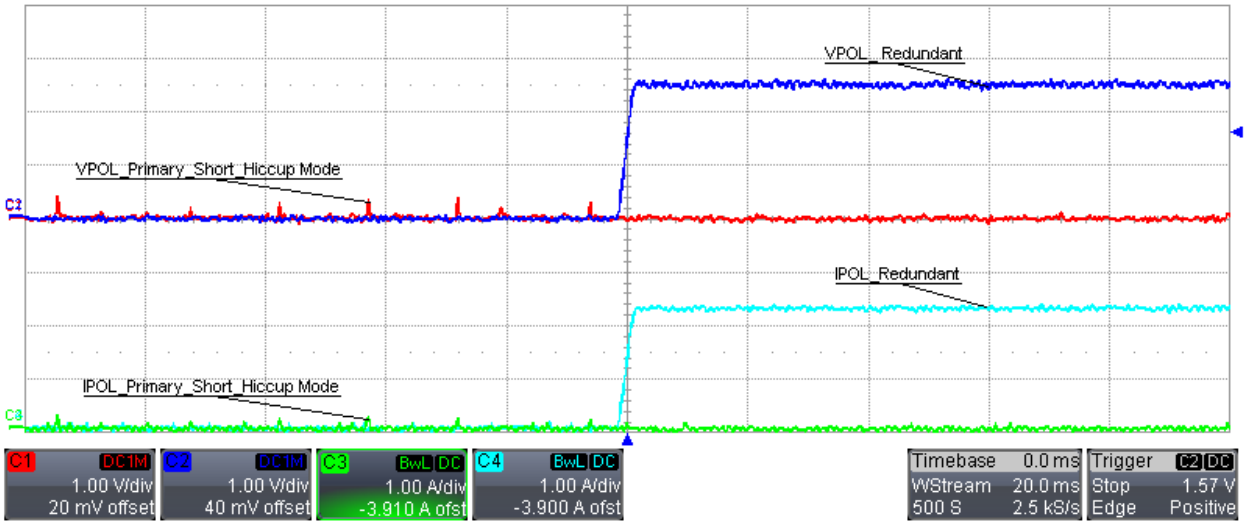

Figure 5. *Oscilloscope plot showing the switching to the redundant load caused by a short at the primary load*

Redundant Source Application

Figure 6 shows a block diagram of a redundant source configuration using two ISL7001ASEH 6A synchronous POL buck regulators and two ISL70062SEH load switches. This configuration is used when systems can't afford to implement full redundancy due to size or cost constraints. The main bus can accept a 3V to 5.5V voltage at its inputs and the POL regulators can be set to output a voltage in the range of 0.8V to 3.3V. For higher output voltage (3.3V to 4.67V) the ISL70062SEH load switches can be changed out with ISL70061SEH load switches. The diagram shows an example with the input voltages (V1 and V2) at +5V and the load rails set at +1.0V.

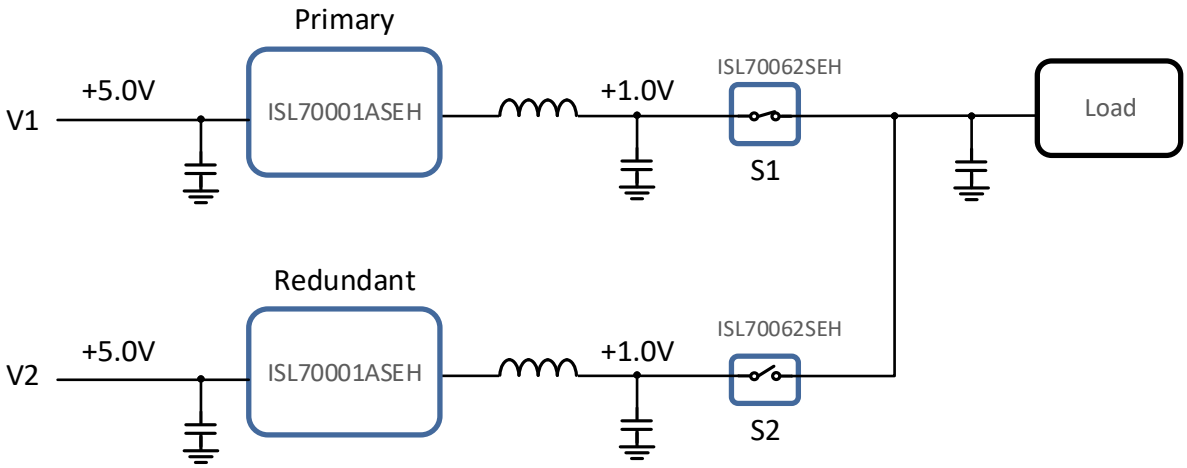

Figure 6. *Block diagram of redundant source application*

The redundant source configuration has one branch designated as the primary source and the other branch designated as the redundant (backup) source. The primary source voltage gets connected to the common load when the load switch (S1) in that branch is turned ON as shown in the diagram. The redundant source gets connected to the common load when the load switch (S2) in that branch is turned ON. If for some reason the primary source (V1) +5V rail goes down or the primary POL regulator malfunctions, that branch can be shut down by turning the S1 load switch OFF. The load can then be powered by the redundant (backup) source (V2) by turning the S2 load switch ON.

Figure 7 shows a picture of a lab setup using two ISL70001ASEH buck POL regulator evaluation boards and two ISL70062SEH load switch evaluation boards connected in a redundant source configuration. Separate power supplies (not shown) are connected to the inputs of the buck regulators. The supplies have their voltage set at +5V. Each regulator output is configured to have an output voltage of +1V and the output of each regulator is connected to the input of a load switch. The outputs of the load switches are tied together and connected to a load that draws 6A. A break-before-make SPDT switch (not shown) is being used to drive the ON control logic pins of the load switches, to switch between the two redundant sources. The SPDT switch in the lab setup mimics the monitoring and control function of the power distribution unit. In many applications, this function is realized by using a microcontroller or a field programmable gate array (FPGA).

The oscilloscope plots in Figure 7 show the voltage and current waveforms at the output of the POL regulators while switching the 6A load from the primary source to the redundant (backup) source. The red trace (VPOL_Primary) is the voltage at the output of the primary POL regulator and the green trace (I POL_Primary) is the current out of the primary POL regulator. The blue trace (VPOL_Redundant) is the voltage at the output of the redundant (backup) POL regulator and cyan trace (I POL_Redundant) is the current out of the redundant (backup) POL regulator.

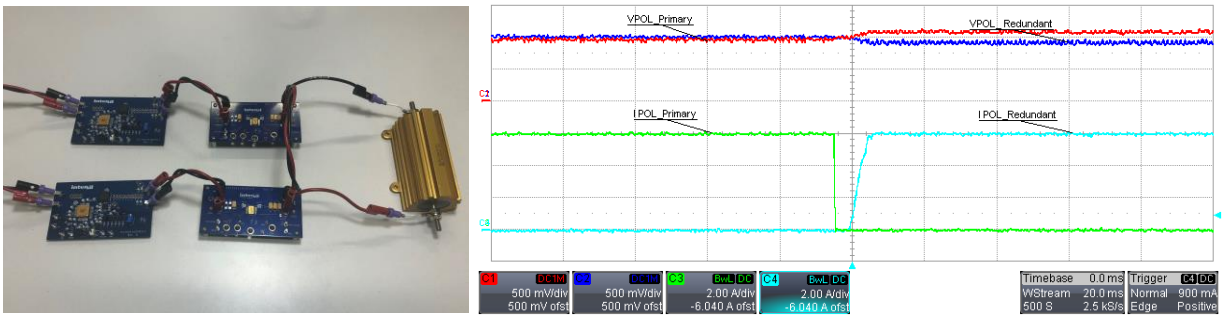

Figure 7. *Redundant source setup using evaluation boards, oscilloscope voltage, and current waveforms*

Figure 8 shows the oscilloscope plots of the voltage and current waveforms with the primary +5V supply voltage turned OFF. During the period when the primary load switch is ON (redundant load switch is off) the primary POL

regulator output is at 0V because there is no voltage at the input of the regulator. If the primary +5V input voltage is off or disconnected, the supply voltage at the load will be at 0V and the load current drops to 0A. When the load switches are toggled to turn the primary load switch OFF and turn the redundant load switch ON, the +1V from the redundant POL regulator gets connected to the load, and the load now draws the 6A of current.

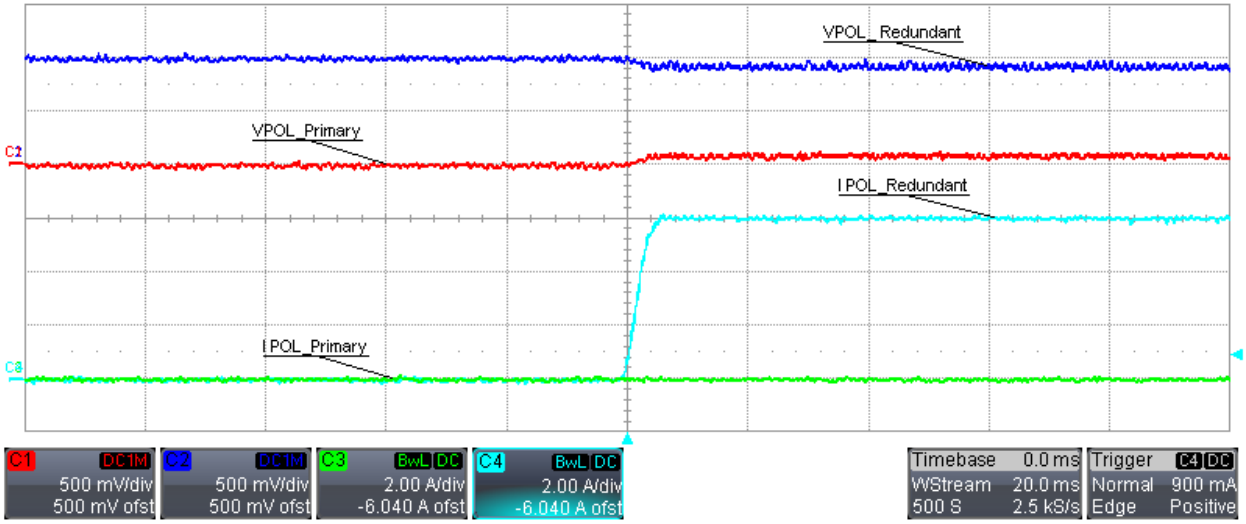

Figure 8. *Oscilloscope plot showing the switching to the redundant source with the primary supply turned off*

Figure 9 shows the oscilloscope plots of the voltage and current waveforms with the output of the primary regulator shorted to ground. The primary regulator responds to the short by collapsing its +1V rail to ground and enters the short circuit hiccup mode. As long as the short remains, the supply voltage at the load is at 0V and the load current drops to 0A. When the load switches are toggled to turn the primary load switch OFF and turn the redundant load switch ON, the +1V from the redundant POL regulator gets connected to the load and draws the 6A of current.

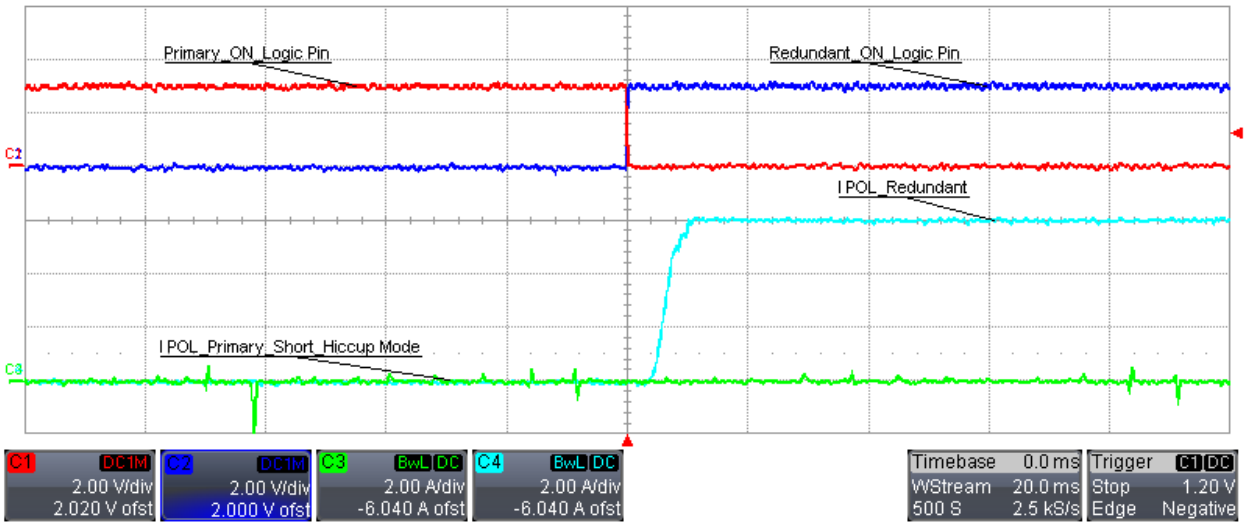

Figure 9. *Oscilloscope plots primary regulator output shorted to ground and switching to the redundant source*

Two Load Switches Connected in Parallel

Figure 10 shows two load switches connected in a parallel configuration. Switches connected in parallel can be used when an application needs to switch > 10A of current, or to reduce the voltage drop across the switch path by reducing the switch path ON resistance.

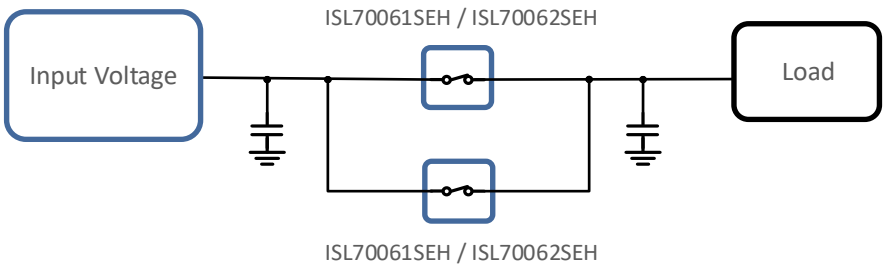

Figure 10. *Load switch parallel configuration*

The parallel configuration reduces the overall switch path ON resistance by half versus the ON resistance of a single switch as shown in Figure 11. The lower ON resistance means less switch path voltage drop for applications that need to meet the voltage headroom requirements of low supply voltage payload modules.

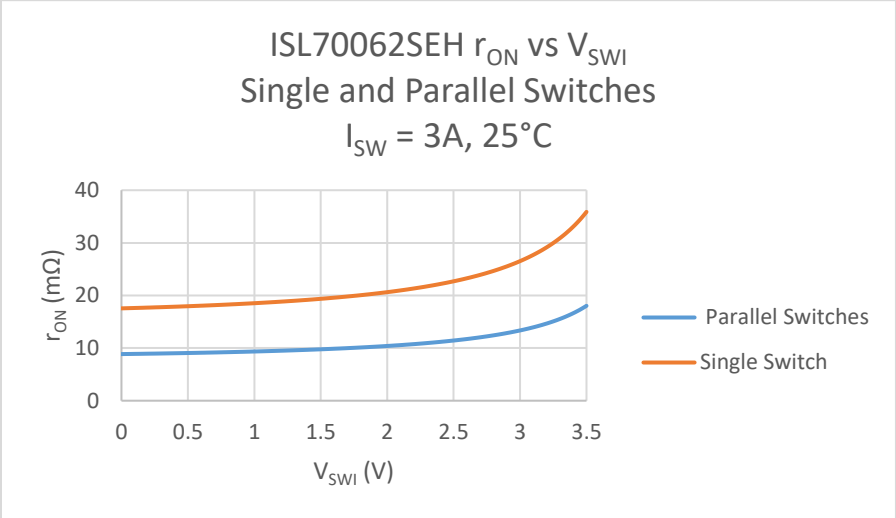

Figure 11. *R_{ON} of two load switches in parallel vs R_{ON} of a single load switch*

A single load switch can handle up to 10A of continuous DC current. For applications that need > 10A, two load switches in parallel can be used to increase the current up to 20A.

Figure 12 oscilloscope plots show the current sharing of two ISL70062SEH switches connected in parallel. The supply voltage at the input is +2V and the output is connected to an electronic load set at 16A. As you can see from the plots, each load switch shares 8A of the current equally. When the parallel combination is switched ON and OFF, each of the switch currents transition smoothly to 8A during turn-on, and to 0A during turn-off.

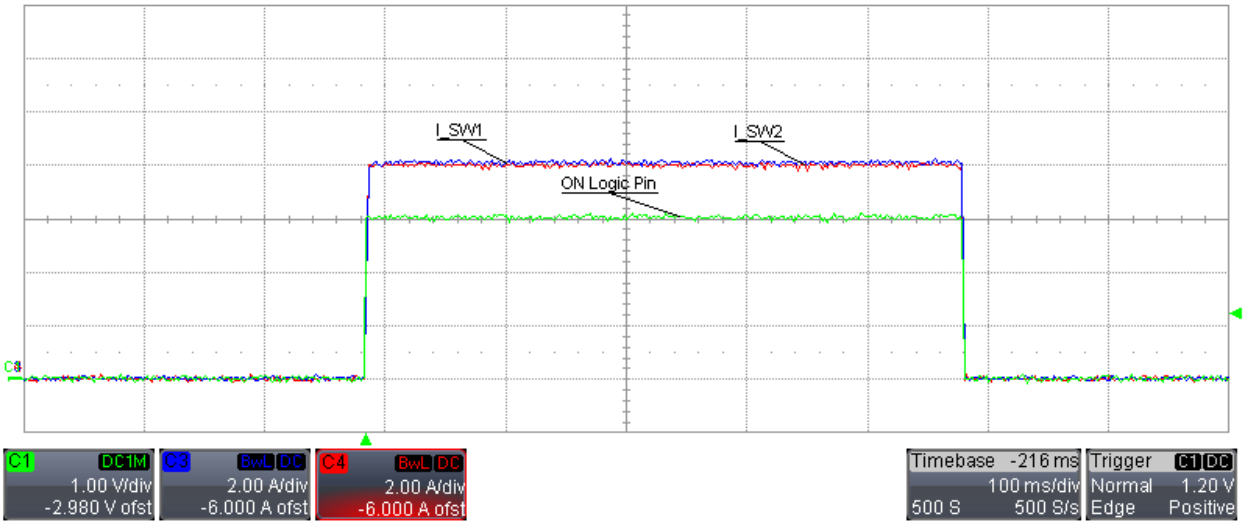

Figure 12. *Isw1 & Isw2 as parallel circuit is turned ON and OFF, V_{SWI} = +2V, I_{LOAD} = 16A*

Conclusion

With the arrival of the Intersil QML-V qualified ISL7x0061SEH (PMOS) and ISL7x0062SEH (NMOS) radiation hardened load switch ICs by Renesas, Space Power Engineers will be able to quickly implement DPA POL redundancy when using the load switches with Intersil state-of-the-art POL regulators by Renesas, i.e. ISL70001A, ISL70003A, etc.

The integrated load switches will allow Engineers to replace older, more complex redundancy systems that use discrete components to implement the switching between the primary to redundant system. Reducing the number of discrete components saves space, weight, and power resulting in major cost savings for spacecraft manufacturers.

Next Steps

- **Learn more about the ISL7x061SEH**
- **Learn more about the ISL7x062SEH**
- **Learn more about the ISL70001ASEH**