PCI Express® Clocks

PCIe Reference Clock Jitter Measurements for Gen5 and Beyond

Ron Wade, System Architect, Data Center Business Division
John Hsu, Senior Manager, Electrical Design Engineering
Joe Tajnai, Manager, Product Engineering

Introduction

Peripheral Component Interconnect (PCI) was a parallel address/data bus specified with time-domain electrical parameters such as set-up/hold times and cycle-to-cycle jitter. The ideal measurement instrument for these time-domain parameters was (and is) a digital sampling oscilloscope (DSO), sometimes referred to as a real-time oscilloscope. PCI used 3.3V LVCMOS signaling, and used spread-spectrum clocking (SSC) techniques to minimize EMI.

PCI Express (PCIe) superseded PCI by introducing serial communication links in place of the parallel address/data buses. *Frequency-domain* parameters such as phase jitter became very important, although PCIe Gen1 did not initially recognize this. PCIe also introduced ±0.7V differential HCSL signaling levels. HCSL helped reduce EMI from the clock, and SSC remained the default for most PCIe systems. The PCIe ecosystem developed procedures for gathering time-domain information (clock period files) with DSOs and calculating clock phase jitter.

This methodology is unique to PCIe, as is the use of SSC with serial communication links. Other serial communication interfaces use Phase Noise Analyzers (PNAs) to measure phase noise; that is, other protocols use a frequency domain instrument to measure frequency domain parameters. Other serial protocols do not use SSC. Until recently, PNAs could not measure spread-spectrum clocks – that is no longer the case. PNAs are now available that can measure spread-spectrum clocks and provide dBc/Hz CSV files for post processing.

Unfortunately, as PCIe data rates increase and reference clock (Refclk) jitter budgets shrink, we can no longer ignore the intrinsic jitter of our measurement setup. We define “intrinsic jitter” as jitter originating or due to causes or factors wholly within a system. In theory, we may obtain the intrinsic jitter of a measurement setup by measuring a “noiseless” device. The results are the intrinsic jitter of the measurement setup. Ideally, we can then remove the intrinsic jitter from our measurements.

Note: We use the term “noiseless” to mean “noiseless” *with respect to* PCIe Gen5 (and Gen6).

This white paper:

1. Identifies two “noiseless” PCIe Refclk sources and calculates their theoretical PCIe Gen5 jitter limits
2. Measures a noiseless PCIe Refclk source with a PNA and a DSO, and compares the results
3. Measures a noiseless PCIe Refclk source at various slew rates with a PNA and a DSO, and compares the results
4. Measures a fan-out buffer and attempts to remove DSO intrinsic jitter from the results
5. Measures a clock generator and attempts to remove DSO intrinsic jitter from the results

Note: In the interest of brevity, this document focuses exclusively on the 32GT/s Gen5 Common Clocked (CC) specifications. The document applies to all current and future PCIe data rates.

Contents

1. Noiseless" Sources

No source is truly "noiseless." However, we can consider several clock sources to be noiseless *with respect to* PCIe. These sources have theoretical phase jitter limits of less than 5fs RMS against the PCIe Gen5 CC limit of 150fs RMS. One such source is an ultra-low noise crystal oscillator, such as the Wenzel® VHF ULN series. A second noiseless source is a programmable RF and Microwave Signal Generator, such as the Rhode and Schwarz® SMA100B. Each has advantages and disadvantages, and both are suitable for our purposes. First, we convert the phase jitter specifications into piece-wise-linear plots. From the plots, we generate dBc/Hz CSV files, and calculate the theoretical best-case PCIe Gen5 CC jitter for each.

1.1 Noiseless Ultra-Low Noise Crystal Oscillators (ULNXO)

ULNXOs are very low noise, relatively inexpensive and easy to use. The highest performance versions provide a single-ended LVCMOS sine wave output. This makes these devices easiest to measure with a PNA since the single output connects directly to the PNA input via a coaxial cable.

Measuring a UNLXO with an oscilloscope presents a few challenges. The major challenge is the very slow slew rate of the UNLXO sine wave output. We need an external device to "sharpen the edges". (We will dive into this issue in more detail later in this document.) The other major challenge is the single-ended nature of the output. We need another device to convert the UNLXO output to the differential type used by PCIe. Luckily, we can use a single device, referred to as a balun, to resolve both issues.

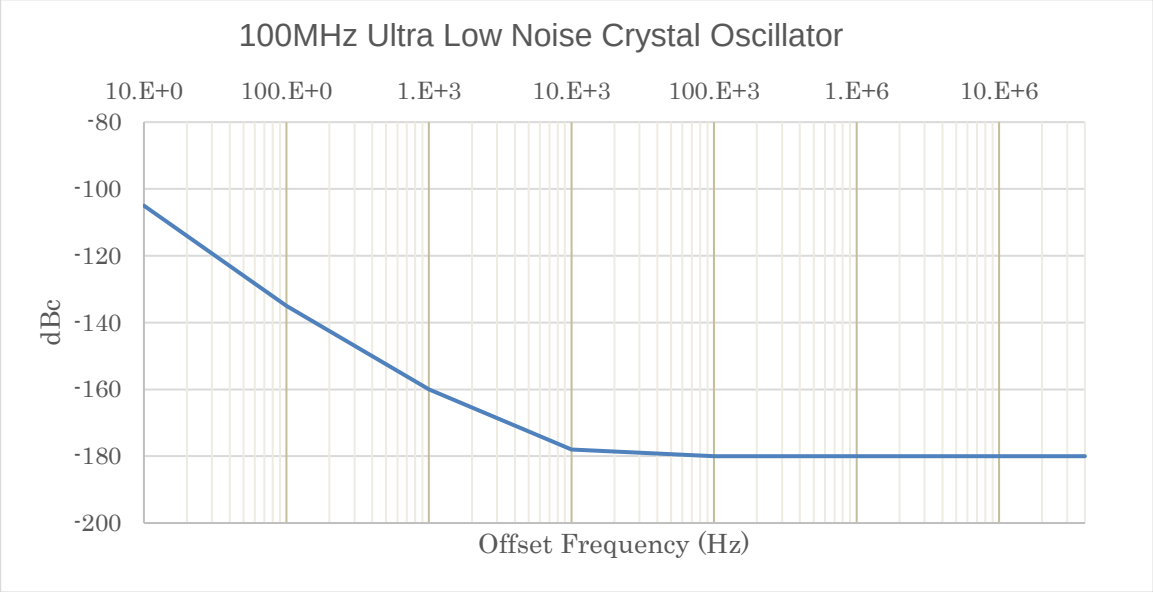

Figure 1. Phase Noise of UNLXO (Piece-wise Linear Model from Datasheet)

The theoretical limit in Figure 1 is 10.07fs RMS (12kHz to 20MHz) and 1.84fs RMS (PCIe Gen5 CC).

1.2 Noiseless Programmable RF and Microwave Signal Generators (RFSG)

RFSGs are also very low noise, and easy to use. An RFSG can generate a wide range of frequencies (8kHz to 67GHz for an SMA100B) making it much more flexible than ULNXOs. (A single ULNXO is required for each desired output frequency.) An RFSG, such as the SMA100B, offers both single-ended and differential square wave and single-ended sine wave outputs, making it ideal for use with both PNAs and DSOs.

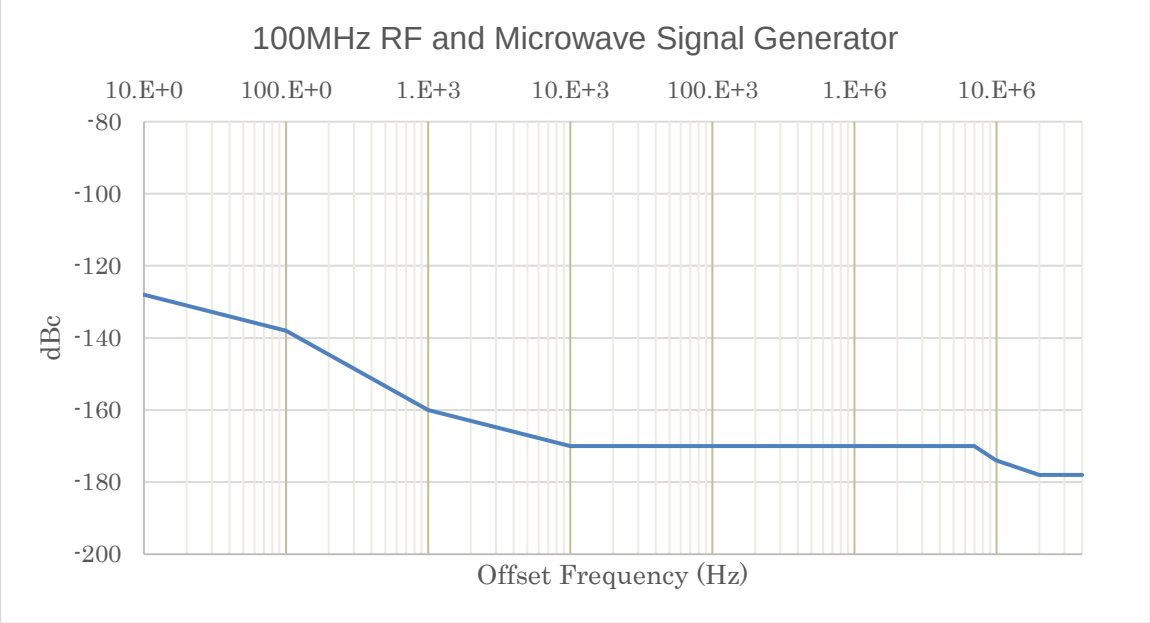

Figure 2. Phase Noise of SMA100B (Piece-wise Linear Model from Datasheet)

The theoretical limit in Figure 2 is 23.96 RMS (12 kHz to 20 MHz) and 2.48fs RMS (PCIe Gen5 CC).

We note that the SMA100B is *slightly* higher jitter than a UNLXO. However, with respect to the 150fs RMS limit for PCIe Gen5 we still have $\mathrm{SQRT}(150^2 - 2.48^2) = 149.98$fs RMS of jitter budget. The SMA100B and the UNLXO are essentially noiseless with respect to PCIe Gen5.

Table 1 summarizes the theoretical limits of our noiseless PCIe sources. If our measurement setup added no noise to the results, these values are the best that we could expect. Note that we round the values.

Table 1. Theoretical Phase Jitter Limits of Noiseless PCIe Sources

Source	Phase Jitter (12kHz – 20MHz)	PCIe Gen5 CC Phase Jitter
ULNXO	10 fs RMS	1.8 fs RMS
RFSG	24 fs RMS	2.5 fs RMS

2. Measuring the Noiseless Refclk Source

Table 2 lists the equipment used for our intrinsic jitter measurements.

Table 2. Equipment Used for Intrinsic Jitter Measurements

Noiseless Source	PNA	DSO	Balun
R&S® SMA100B	R&S® FSWP	Keysight® S404	Mini-Circuits® ZFSCJ Series

2.1 Measurement Setup

We will use the SMA100B as our noiseless source and measure it two ways. We will obtain phase noise files with the PNA and clock period files with the DSO. We will then post-process the files to obtain the PCIe Gen5 CC results. Figure 3 shows the measurement setups. While the SMA100B offers a single-ended output, we use the differential outputs for three reasons:

1. We want to use the same SMA100B internal signal source for both PNA and DSO measurements.
2. The SMA100B differential outputs allow a direct connection to the DSO.
3. The SMA100B specifies its differential outputs to drive 50-ohm terminations, which is the input impedance of the PNA and the DSO.

We use a balun to combine the differential outputs of the noiseless source into a single output to drive the PNA. This balun has a minimum bandwidth of 2GHz to minimize any impact on the results.

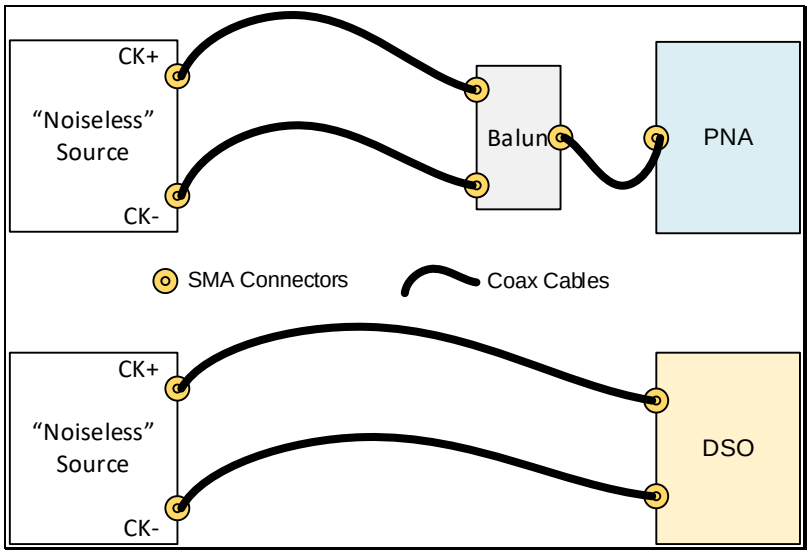

Figure 3. Setup for Baseline Intrinsic Jitter Measurements

2.2 PNA Measurement Results

Figure 4 is the phase noise plot of the SMA100B obtained by the PNA. The 12kHz to 20MHz phase jitter measures 23.793fs RMS. These results are 0.2fs RMS lower than the theoretical best case. This is possible because we derived the theoretical limit from a piece-wise-linear approximation of the phase noise plot in the SMA100B datasheet. The approximation was intentionally conservative; therefore, we round to 24fs RMS and can state that this measurement setup is essentially noiseless.

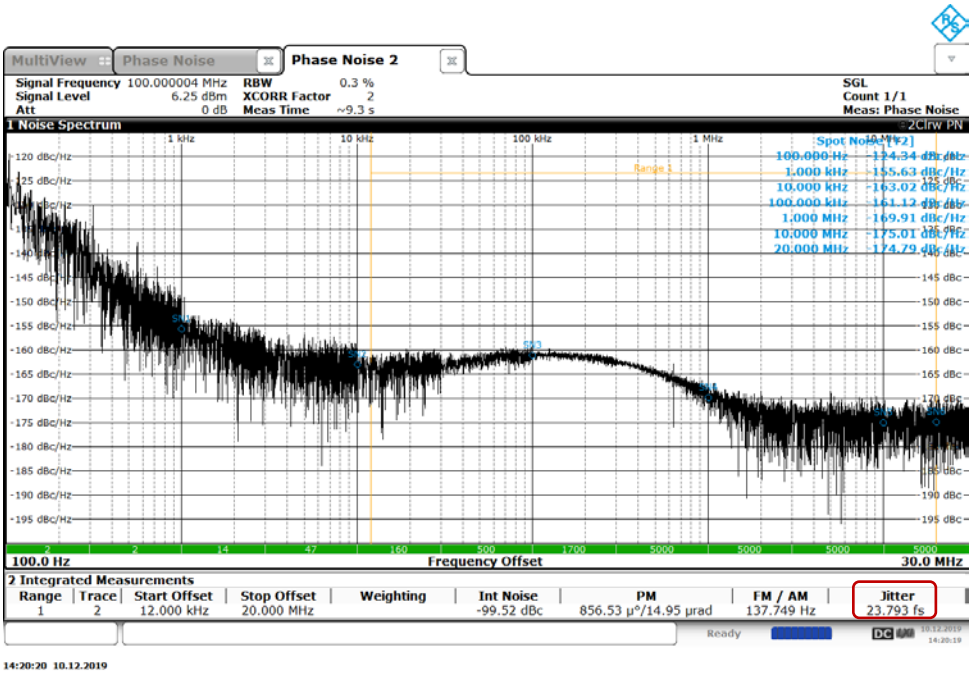

Figure 4. Phase Noise of SMA100B (Measured)

Next, we take the CSV file saved from Figure 4 and post-process it with the Renesas PNA2PCIe tool.

In Figure 5 we see that the FSWP PNA measured the SMA100B at 3.28fs RMS against the PCIe Gen5 CC filter. We round this to 3.3fs RMS. As a cross check, the tool can also calculate the 12kHz – 20MHz single-side band phase noise, which is 23.75fs RMS. This agrees very closely with the 23.793 fs RMS value given by the PNA itself, and we round to 24fs RMS.

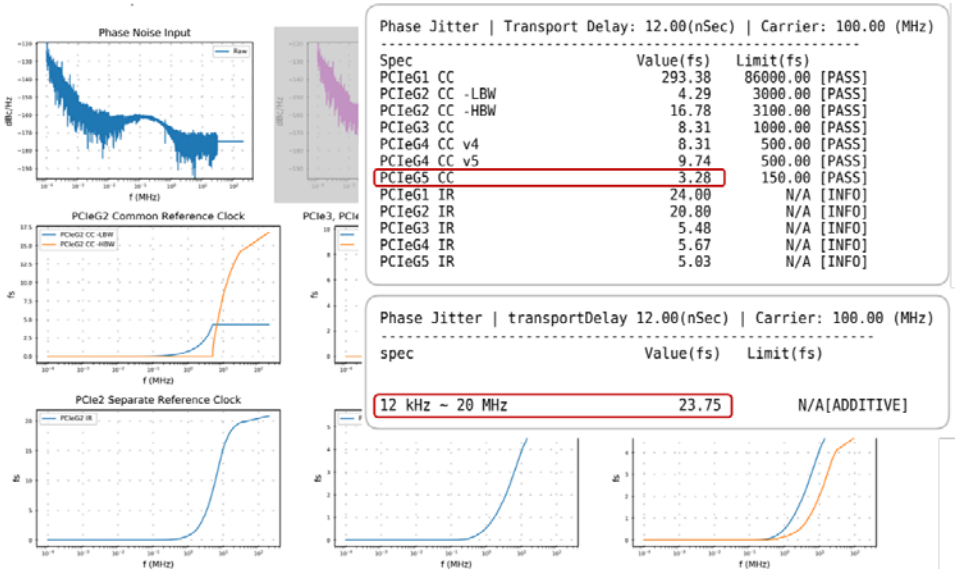

Figure 5. PCIe Gen5 CC Results from PNA

Table 3 summarizes the PCIe Gen5 results measured with a PNA. The PNA measurement setup adds 2.2fs RMS to the theoretical PCIe Gen5 CC results, leaving us with a margin of:

$$\sqrt{(150)^2 - (2.2^2)} = 149.98fs\ RMS$$

Table 3. Summary SMA100B PCIe Gen5 Results Measured by PNA

Specification	PCIe Gen5 Result (fs RMS)	Theoretical Limit (fs RMS)	PNA Gen5 Additive Jitter (fs RMS)	
PCIe Gen5 CC	3.3	2.5	$\sqrt{(3.3)^2 - (2.5^2)}$	= 2.2

These results show that SMA100B is a noiseless source with respect to the PCIe Gen5 CC 150fs RMS jitter limit.

2.3 DSO Measurement Results

Figure 6 shows the SMA100B differential output from which the DSO generates the clock period files for analysis. The Renesas DSO2PCIe tool post-processes these files to calculate the PCIe Gen5 jitter.

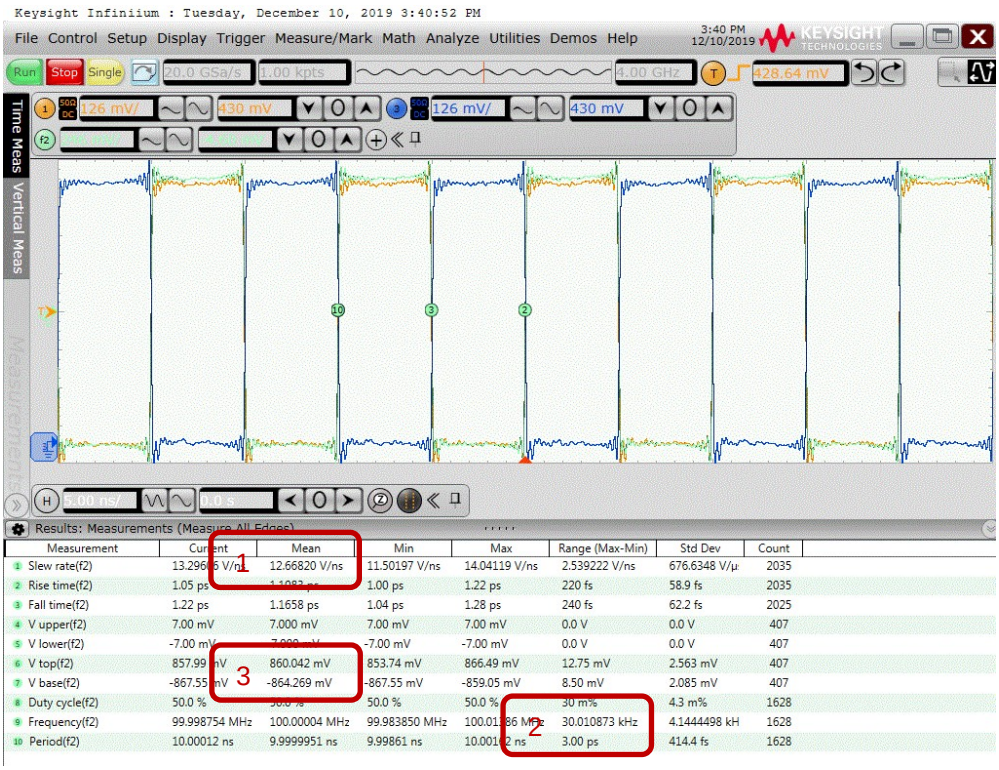

Figure 6. SMA100B Clock Sampled by DSO

There are several things to note about the SMA100B waveform before we proceed. First, the mean value of the clock slew rate is >12V/ns! The PCIe specification indicates a maximum slew rate of 4V/ns. We will return to this item in the next section.

Second, the frequency range (Max – Min) is ~30kHz, with a corresponding period jitter of 3ps. The SMA100B frequency accuracy is <<<30 kHz, and therefore, its period jitter is <<< 3ps.

Third, the single-ended amplitude is ~860mV, because the SMA100B outputs are specified into a 50ohm load, which matches the input impedance of the DSO.

Now, let us look at the PCIe results from the clock period file. Figure 7 illustrates the results obtained by post processing the clock period file from the waveform in Figure 6. According to the post-processed clock period file, the SMA100B is 28fs RMS when filtered for PCIe Gen5 CC.

This is a significantly higher than the 3.3fs RMS calculated from the PNA CSV file.

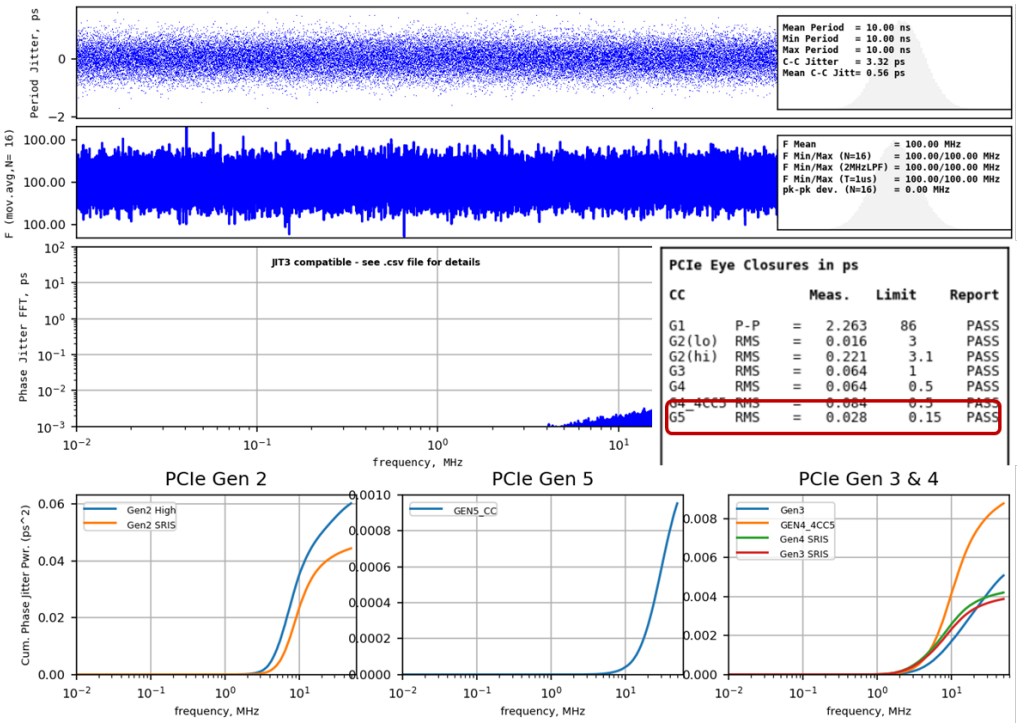

Figure 7. PCIe Gen5 CC Results from DSO

Due to the wonders of RMS math, we still have a significant margin to the PCIe Gen5 CC specification. Table 4 summarizes the PCIe Gen5 results for the noiseless source measured with a DSO. The DSO measurement setup adds 27.9fs RMS to the PCIe Gen5 CC results, leaving us with a margin of:

$$\sqrt{(150)^2 - (27.9^2)} = 147.4fs\ RMS$$

Therefore, we may still consider the SMA100B to be a noiseless source, even when calculated from time domain measurements obtained with a DSO. Note that Figure 7 presents results in picoseconds, which we convert to femtoseconds for use in this document.

Table 4. Summary SMA100B Results Measured by DSO

Specification	PCIe Gen5 Result (fs RMS)	Theoretical Limit (fs RMS)	PNA Gen5 Additive Jitter (fs RMS)	
PCIe Gen5 CC	28	2.5	$\sqrt{(28)^2 - (2.5^2)}$	= 27.9

Another way of looking at Table 4 is that we can never measure a PCIe Gen5 CC result < 28fs RMS for a clock with similar electrical characteristics (amplitude, slew rate and phase noise). This means that for this DSO and this clock source, 27.9fs RMS is the lowest value that we can measure for PCIe Gen5 CC. We round this value to 28fs RMS.

So far, we can consider the SMA100B as noiseless source whether using a PNA or a DSO *for PCIe Gen5 CC.*

3. Measuring the Noiseless Refclk for Various Slew Rates

Recall from Figure 6 that the SMA100B output slew rate is > 12V/ns; also recall that the maximum PCIe Refclk slew rate is specified as 4V/ns. Our next task it to measure the noiseless source at various slew rates with both the PNA and the DSO, to ensure that the intrinsic jitter of our measurement setup remains negligible.

3.1 Measurement Setup for Various Slew Rates

The SMA100B does not have a programmable output slew rate. Therefore, we must find a way to slow down the output slew rate. We must also find a way to do so while maintaining the 860mV output amplitude of the signal generator. The solution chosen for this white paper is a simple circuit board with SMA inputs and outputs and a position to mount load capacitors of different values. A purely capacitive load does not attenuate signal amplitude and we may adjust the clock slew rate by changing the capacitor values.

Table 5 shows the capacitor values used to adjust the slew rate of the SMA100B outputs, while Figure 8 illustrates the revised test setup. It is very similar to the baseline setup in Figure 4 with the addition of the load board. In fact, the baseline measurements (0pf) use the setup in Figure 4 without the load board.

Table 5. Load Capacitance vs. Slew Rate

C_L (pF)	22	20	16.9	12.7	10.7	8.7	6.7	4.7	2	0
Slew Rate (V/ns)	0.7	0.9	1.5	2.2	3.1	3.8	3.9	4.2	7	12.7

Key Takeaway

The *key takeaway* of Table 5 is the slew rate and not the capacitor values.

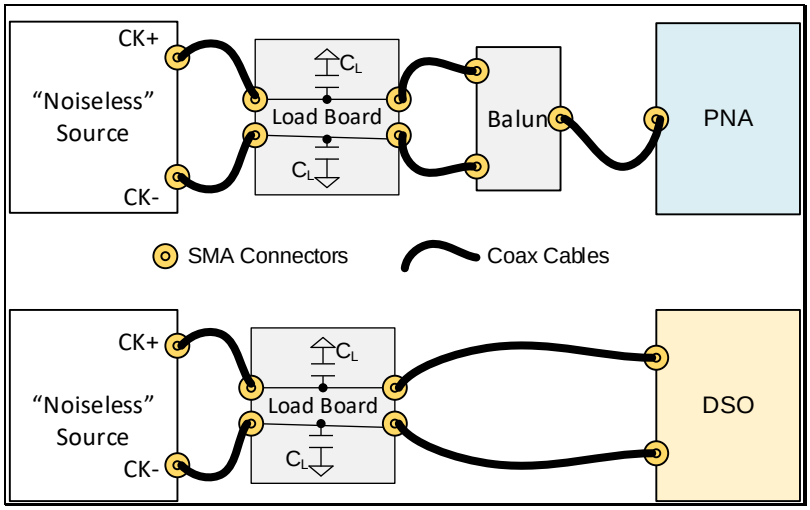

Figure 8. Setups for Variable Slew Rate Intrinsic Jitter Measurements

We can see that the measurement setup for variable slew rate is identical to the baseline setup, except for the insertion of the load board between the noiseless source and the balun for PNA measurements, and between the noiseless source and the DSO for the DSO measurements.

3.2 PNA Measurement Results for Various Slew Rates

Figure 9 and Figure 10 show the PCIe Gen5 CC results from the PNA measurements taken at various slew rates. The first figure shows the results against the 150fs RMS limit for Gen5 CC. The second figure shows the same results with the vertical axis zoomed from 150fs RMS full scale to 8fs RMS full scale.

We see that the PNA results are virtually independent of slew rate and are virtually noiseless with respect to PCIe Gen5 CC. Recall that the amplitude for these measurements is relatively constant at ~860mV. Zooming in on the vertical axis, Figure 10 shows that the measured PCIe Gen5 CC results range from 3.0 to 3.5 fs RMS across all slew rates. The dashed line is a best-fit trend line, which is linear, and is virtually flat.

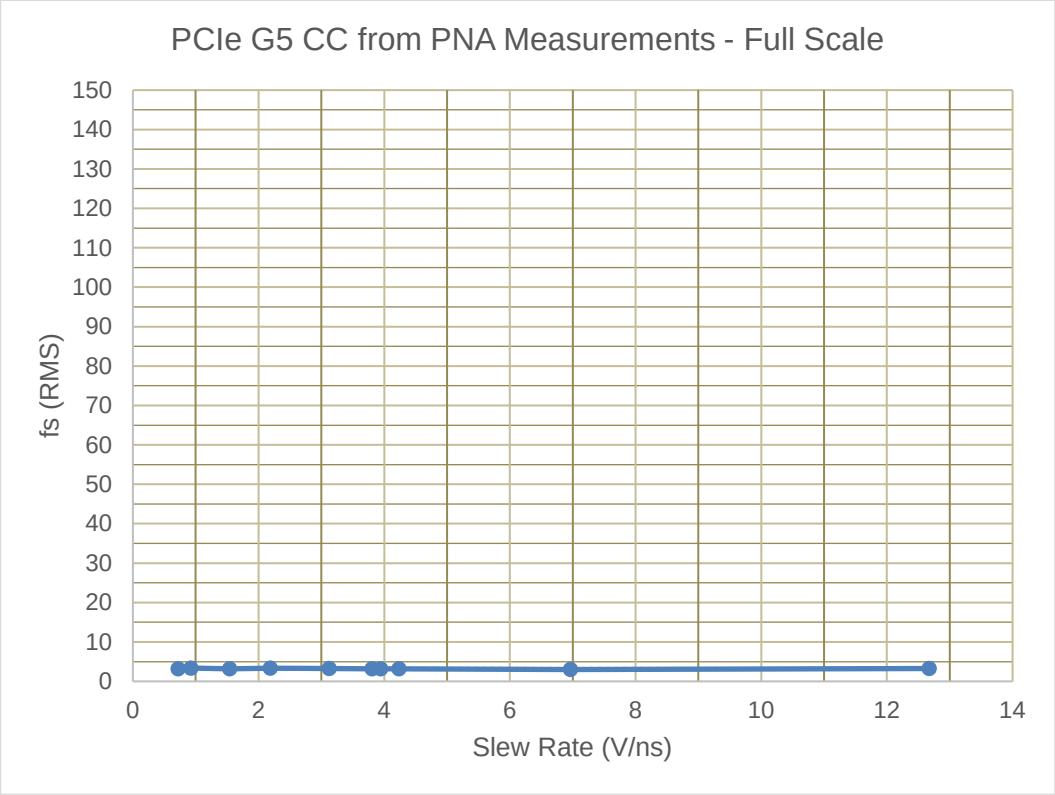

Figure 9. PCIe Gen5 CC Results vs. Slew Rate for PNA – Noiseless Source

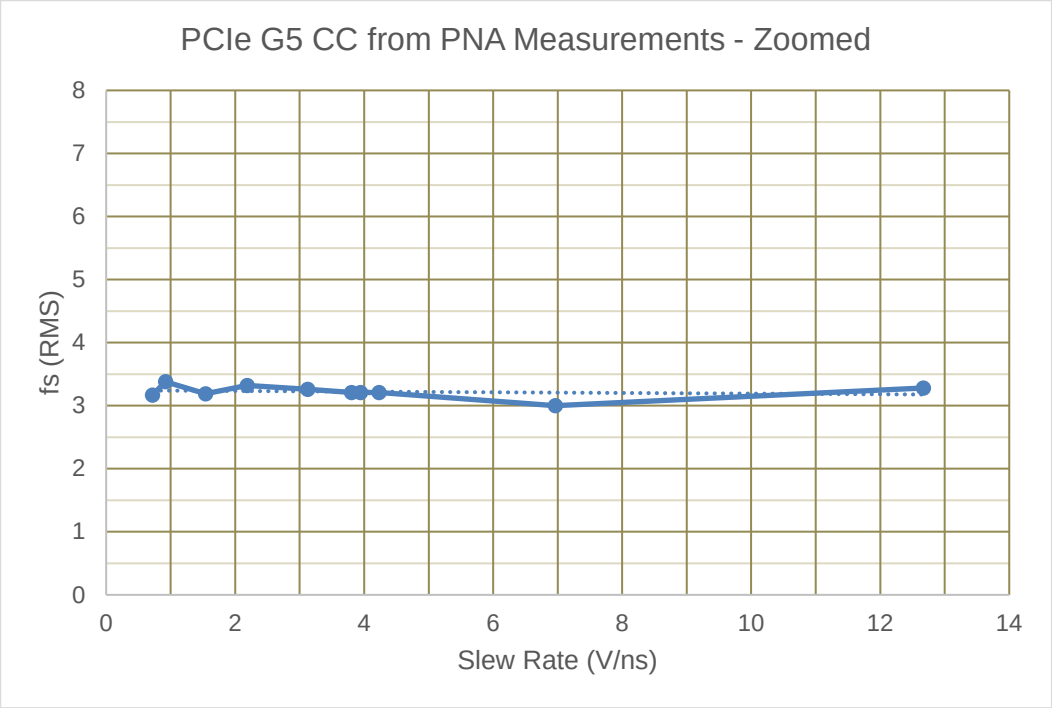

Figure 10. PCIe Gen5 CC Results vs. Slew Rate for PNA – Noiseless Source - Zoomed Vertical Axis

3.3 DSO Measurement Results for Various Slew Rates

We use the same test set up shown in Figure 8 to adjust the output slew rate of the SMA100B for DSO measurements. The slew rates are as indicated in Table 5.

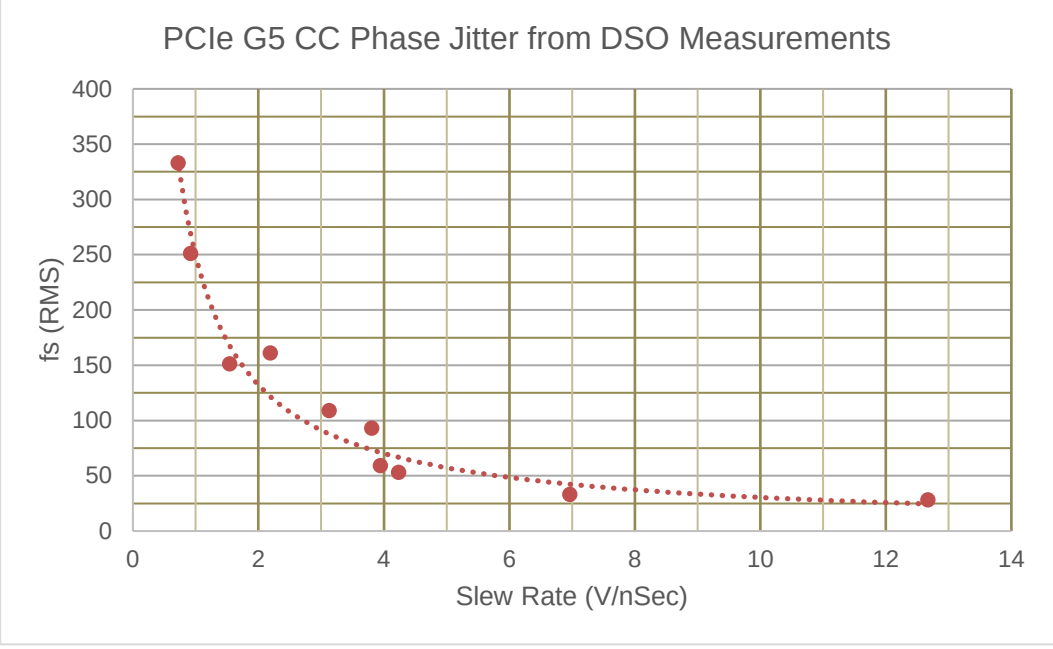

Figure 11. PCIe Gen5 CC Results vs. Slew Rate for DSO

Figure 11 shows the PCIe Gen5 CC results obtained by post processing DSO clock period files obtained at different slew rates. The red dots are the measured data and the dashed line is the best-fit trend line. Clearly, this is different from the PNA results. The DSO results show dramatically increasing jitter as slew rates decrease. These results seem to indicate that the SMA100B violates the PCIe Gen5 CC jitter limit as slew rates decline to < ~1.5V/ns!

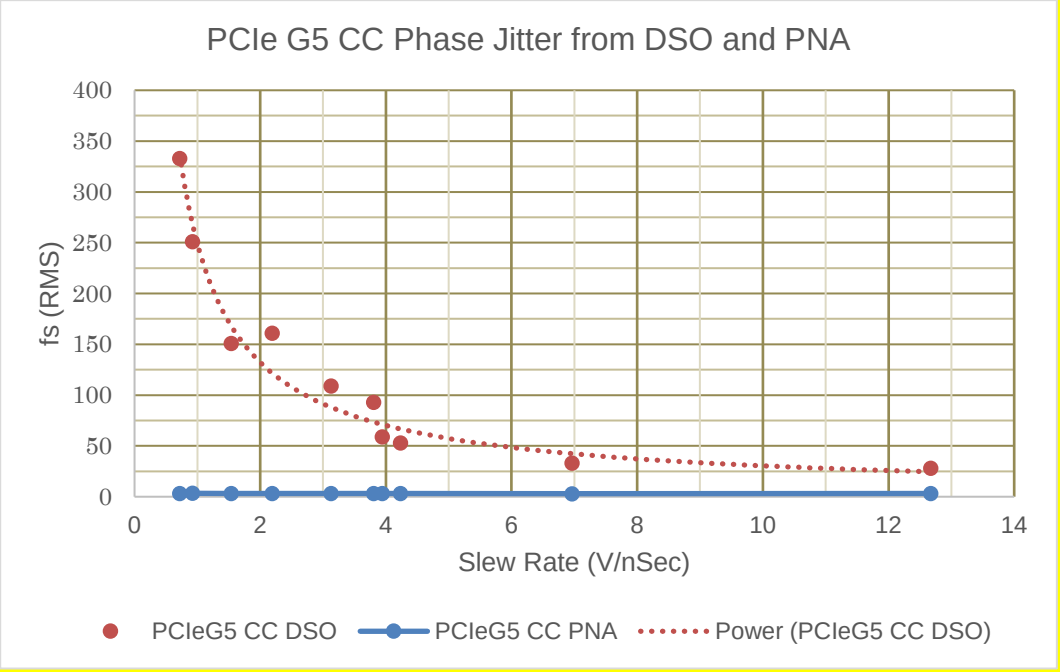

Figure 12. Comparison of DSO and PNA Results

Figure 12 plots the DSO and PNA on the same scale to illustrate this difference. The PNA results are consistent and noiseless. The DSO results are varying and range from ~noiseless at 12.7V/ns to violating the 150fs RMS spec limit at 1.5V/ns. Remember, we mean noiseless with respect to PCIe Gen5.

The SMA100B is a virtually noiseless noise source for all these measurements. The only thing changed is the use of a DSO instead of a PNA. What is going on? Why the dramatic difference in results between the PNA and the DSO? We will return to these questions later.

4. Removing DSO Intrinsic Noise Using an RFSG as a Noiseless Source

This section uses the RFSG noiseless source to drive a Fan-out Buffer. We will measure additive jitter and attempt to remove the DSO intrinsic noise from the results.

4.1 Measuring Additive Jitter of a Fan-out Buffer Using a PNA

Now, we calculate additive jitter of a fan-out buffer. Figure 13 illustrates the setups for measuring additive jitter. The setup is identical to the variable slew rate setup of Figure 8 with the load boards replaced with the DUT board containing the buffer. The buffer's additive RMS jitter is:

$c = \sqrt{a^2 - b^2}$, where c = additive jitter, a = output jitter, and b = input jitter

The fan-out buffer has two selectable output slew rates, fast and slow. We will calculate the additive jitter for both settings using the PNA and DSO setups. We discuss actual slew rates in the DSO section, since, as we have seen, they have minimal impact on PNA results.

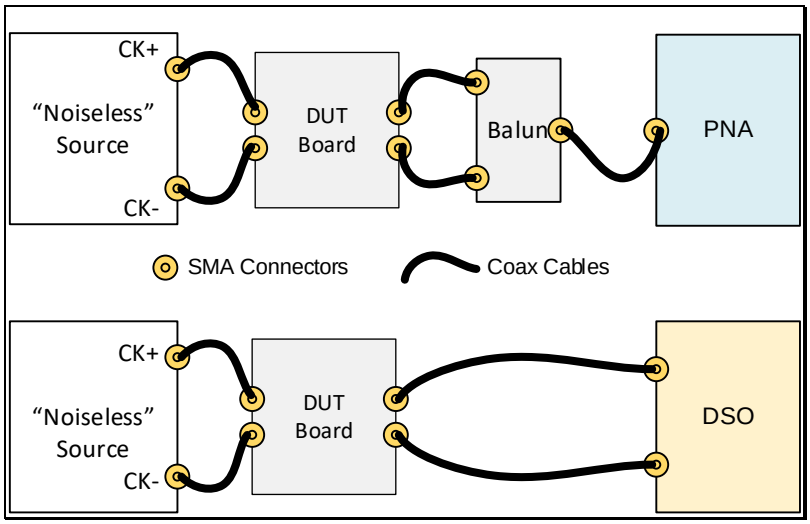

Figure 13. Setups for Measuring Additive Jitter of a Fan-out Buffer

Additive jitter results from the PNA measurements are show in Table 6. We can see very little slew rate impact on the results. For PCIe Gen5 CC, the buffer under test has additive phase jitter of 14 to 16 fs RMS. 12kHz to 20MHz data is provided as a cross check.

Table 6. Calculating the Additive Jitter of a Fan-out Buffer - PNA Results

Units are fs RMS Input is SMA100B	Input Jitter (Noiseless Source)	Output Jitter (Fast Slew Rate)	Additive Jitter (Fast Slew Rate)	Output Jitter (Slow Slew Rate)	Additive Jitter (Slow Slew Rate)
PCIe Gen5 CC	5	15	14	17	16
12 kHz ~ 20MHz	31	109	105	112	108

We see the results are very consistent, as expected. Next, we will repeat the same procedures with the DSO and look for the same consistency.

4.2 Measuring Additive Jitter of a Fan-out Buffer using a DSO

Using the DSO setup from Figure 13, we obtain additive jitter results in Table 7. There are two things to note. First, the additive jitter values are much higher than those obtained using the PNA. Second, the results are, again, extremely sensitive to the DUT slew rate. At the slow slew rate setting, the DSO measurement setup provides an additive jitter result that is higher than the 150fs RMS PCIe Gen5 CC specification limit. Clearly, we must consider DUT slew rate for any attempt at removing intrinsic jitter. We will attempt this in the next section. Remember that the PNA results do not require this extra step.

Table 7. Calculating the Additive Jitter of a Fan-out Buffer - DSO Results

All jitter units are fs RMS	Input Jitter (Noiseless Source)	Output Jitter (Fast Slew Rate)	Additive Jitter (Fast Slew Rate)	Output Jitter (Slow Slew Rate)	Additive Jitter (Slow Slew Rate)
PCIe Gen5 CC	28	81	76	159	156
Slew rate (V/ns)	12.6	2	'-	1.3	'-

4.3 A Formula to Remove DSO Intrinsic Noise Due to Slew Rate

If signal slew rate is the only variable affecting DSO results, then we should now be able to remove DSO intrinsic noise from our results. In an earlier version of this white paper, we developed a formula to correct for intrinsic DSO jitter due to slew rate. We list the summary equations below.

1. $Tj_m = \sqrt{(Tj_{DUT})^2 - (Tj_{add})^2}$
2. $Tj_{add} = \sqrt{\frac{SR_{NS}}{SR_{DUT}}} Tj_{NS}.$

Substituting equation 2 into equation 1 give us:

3. $Tj_m = \sqrt{(Tj_{DUT})^2 - \left(\frac{SR_{NS}}{SR_{DUT}} Tj_{NS}\right)^2}$

The parameters in the above equations are:

$Tj_m = The\ rms\ jitter\ of\ the\ DUT\ with\ scope\ intrinsic\ jitter\ removed.$

$Tj_{add} = The\ intrinsic\ jitter\ of\ the\ DSO$

$Tj_{DUT} = The\ total\ rms\ jitter\ measured\ at\ the\ output\ of\ the\ DUT.$

$Tj_{NS} = The\ measured\ rms\ jitter\ of\ a\ "noiseless\ source".$

$SR_{NS} =$ The $slew\ rate\ of\ the\ "noiseless\ source".$

$SR_{DUT} = The\ slew\ rate\ of\ the\ DUT.$

4.3.1 Applying the Noise Removal Formula to the Additive Jitter of a Fan-out Buffer

Studying equation 3 carefully, we can see that Tjm must be ≥ 0 or the equation will attempt the square root of a negative number. We can determine the conditions where equation 3 is valid, and find from Appendix B. Removing DSO Intrinsic Noise Due to Slew Rate, that it is valid when:

$$\left(\frac{SR_{NS}}{SR_{DUT}}\right) \leq \left(\frac{Tj_{DUT}}{Tj_{NS}}\right)$$

Using this equation, we now test the results in Table 7 to see if we can use the slew-rate correction formula. Let us test the fast slew rate results first. We ask ourselves, “Is the following true?”

$$\left(\frac{12.6}{2}\right) \leq \left(\frac{81}{28}\right)$$

No, 6.3 is not < 2.9. Therefore, the formula does not hold and we cannot use it to remove intrinsic noise due to slew rate.

For completeness, let us try the DUT slow slew rate. We ask ourselves, “Is the following true?”

$$\left(\frac{12.6}{1.3}\right) \leq \left(\frac{159}{28}\right)$$

No, 9.7 is not < 5.7. Therefore, the formula does not hold and we cannot use it to remove intrinsic noise due to slew rate. Substituting other slew rate/jitter combinations from the equation in Figure 11 does not change the results. The equation does not hold.

Perhaps there is an additional factor beyond slew rate. DSOs have an Analog-to-Digital-Converter (ADC) on the input channels, so signal amplitude is also a variable that we need to consider. Both the DSO and the PNA terminate inputs with 50 ohms to ground. The SMA100B outputs specify a 50ohm load. They drive ~850mV into this load. On the other hand, driving a 50ohm load results in double terminating the DUT HCSL outputs. Therefore, their output amplitude is only ~425mV. Does input amplitude (ADC resolution) also have an impact on DSO results?

Before we address this question, let us look at a different set of measurements.

5. Removing DSO Intrinsic Jitter with a UNLXO as a Noiseless Source

Recall that we identified two noiseless clock sources. The examples discussed to this point have used the RFSG as the source. We have not used the UNLXO in any of the discussions – the original white paper used a UNLXO as the noiseless reference source. Let us look at another example using the same UNLXO. For this example, *the amplitude of the UNLXO and DUT into the DSO are identical*.

If we take Figure 3, replace the noiseless source with a clock generator DUT and then obtain DSO results for the DUT and the ULNXO, we can attempt to correct for DSO intrinsic noise. The UNLXO drives a balun into the two DSO inputs. For DSO measurements, we also note the slew rates of the measured waveforms. Table 8 contains these measurement results.

Table 8. Clock Generator and UNLXO DSO Results

All jitter units are fs RMS	UNLXO Jitter (Noiseless Source)	Measured DUT Jitter (Fast Slew Rate)	Formula 3 Corrected Jitter (Fast Slew Rate)	Measured DUT Jitter (Slow Slew Rate)	Formula 3 Corrected Jitter (Slow Slew Rate)
PCIe Gen5 CC	58	89	65	237	150
Slew rate (V/ns)	2.8	2.7	'-	0.9	'-

Recalling the conditions for which the correction formula is valid:

$$\left(\frac{SR_{NS}}{SR_{DUT}}\right) \leq \left(\frac{Tj_{DUT}}{Tj_{NS}}\right)$$

For the fast slew rate, we have:

$$\left(\frac{2.8}{2.7}\right) \leq \left(\frac{89}{58}\right)$$

We can see that 1.037 is $\leq$ 1.53 and Formula 3 is valid.

For the slow slew rate, we have:

$$\left(\frac{2.8}{2.7}\right) \leq \left(\frac{237}{58}\right)$$

We can see that 1.037 is < 4.09 and Formula 3 is valid.

How do the corrected DSO results compare to the PNA results?

Using the PNA, we measure **64fs** RMS PCIe Gen5 CC phase jitter of the clock generator DUT at the fast slew rate setting. This compares very favorably with 65fs RMS result obtained after removing the intrinsic noise of the DSO. Unfortunately, PNA results for the slow slew rate are not available.

6. Conclusions

- PCIe Gen5 CC results from a DSO are highly dependent on the DUT slew rate.
- PCIe Gen5 CC measurements from a DSO require removal of its intrinsic noise. This implies a requirement for a two-pass measurement, access to a noiseless clock source, and additional calculations.
- Correcting for slew rate is not sufficient to remove the intrinsic noise of the DSO measurement setup.
- PCIe Gen5 CC measurements from a PNA are highly consistent across DUT slew rates, and do not require two-pass measurements.
- Intrinsic noise is not an issue when using a PNA for PCIe Gen5 Refclk jitter measurements.
- We note a 2:1 amplitude difference in our measurements when using the RFSG as the noiseless reference. The SMA100B drives ~850mV into 50ohm loads. The DUT drives ~425mV into 50ohm loads. We must also take into account signal amplitude in our attempts to remove intrinsic noise.
- We note very good results for intrinsic DSO noise removal when using the ULNXO noiseless source. The ULNXO and DUT amplitudes were matched for the measurements made for this white paper.

Several efforts are underway to develop a consistent method for intrinsic jitter removal from DSO measurements. All require taking multiple measurements to obtain one result.

A PNA provides the simplest way to measure PCI Gen5 (and Gen6) Refclk jitter. Newer PNAs support spread-spectrum clocking, removing one of the biggest objections to use of a PNA.

Appendix A. Mathematical Discussion of Phase Noise Measurements on the PNA and DSO

Appendix A, of National Bureau of Standards Technical Note 632, and updated in the IEEE Std. 1139-1999 defines the notation used in the following discussion. It is augmented with text book conventions (e.g., the Fourier transform of h(t) is denoted as H(f)).

A square wave with average frequency of v_0, and phase jitter of φ(t) has overall phase of

$$\Theta(t) = 2\pi v_0 t + \varphi(t)$$

in radians. Its average period is

$$\overline{\tau} = 1/v_0.$$

Phase jitter is normally measured in units of time. It is defined as

$$x(t) = \varphi(t)/2\pi v_0.$$

Therefore

$$\Theta(t) = 2\pi v_0 t + \varphi(t) = 2\pi v_0 (t + x(t)).$$

Its phase is approximately expressed as

$$\Theta(n\overline{\tau}) = 2\pi v_0 n\overline{\tau} + \varphi(n\overline{\tau}) = 2\pi v_0 (n\overline{\tau} + x(n\overline{\tau})).$$

That is, the phase of the square wave is measured at the zero cross over of each period. The rest of the discussion will use t for notation, where

$$t = n\overline{\tau}.$$

φ(t) and its Fourier transform, Φ(f) form a transform pair. Where f denotes Fourier frequency. Φ(f) cannot be readily measured. A signal's power spectral density (PSD) is measureable. PSD of a band limited signal is defined as

$$S_\Phi(f) = \Phi(f)\,\Phi^*(f)/BW$$

where $\Phi^*(f)$ is the complex conjugate of Φ(f) and BW is the measurement bandwidth. In the Fourier spectrum of the signal under test, SΦ(f) is the two-sided noise spectrum about the carrier.

Phase Noise Analyzers demodulate and measure the single-sided phase noise spectrum, L(f), of the signals under test. Where

$$L(f) \equiv S_\Phi(f)/2$$

and they display

$$PN = 10\log_{10}(L(f))$$

in dBc/Hz. For a phase noise spectrum multiplied by a transfer function H(f), such as PCIe phase noise, PN can be calculated from the display with

$$PN = 10\log_{10}(L(f)) + 20\log(|H(f)|)$$

The above equation allows the calculation of RMS jitter.

$$Tj = \frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2} 10^{PN/10} df}$$

Alternatively, DSOs can be used to either measure phase jitter, Θ(n), of the signal under test (DUT) by recording the time of zero cross over

$\Theta(n) = (t_{0x}(n) - t_{0x}(n-1))/2\pi v_0$, [rad]

tox(n) = time of nth zero crossing

or p(n) of the DUT, the period jitter of the signal under test. Period jitter, which is basically phase jitter in seconds, p(n) can be calculated with

$p(n) = (t_{0x}(n) - t_{0x}(n-1)) - \bar{\tau}$, $n \geq 0 \cap n \epsilon I$

$x(j) = \sum_{n=n_0}^{j} p(n)$ is the accumulated phase jitter

The Fourier transform of the accumulated phase jitter is calculated by

$X(f)$ = DFT(x(j)). (1)

The maximum measureable modulation frequency of a DUT with frequency v_0 is its Nyquist rate

$f_N = v_0/2$

This represents bimodal jitter in the time domain. For an FFT result with N bins, the bandwidth of each bin is

$\Delta f = f_N/N$

This is the measurement bandwidth of the phase noise spectrum. At this point, the phase noise spectrum of DUT is calculated by the equation

$PN = 10log_{10}(L(f)) = 10log_{10}(S_\Phi(f)/2) = 20log_{10}(2\pi v_0 \sqrt{\frac{X(f)X^*(f)}{\Delta f}})$

Appendix B. Removing DSO Intrinsic Noise Due to Slew Rate

DSOs have intrinsic voltage and other noises introduced by their component parts and architecture. DSO intrinsic noise adds to clock period measurements resulting in additional phase noise. We must measure the noise, and subtract the noise from the overall measurement for a valid result. We can measure and record voltage noise with a null input, but other intrinsic noise sources such as time base noise and quantization noise are hard to measure. Therefore, we must measure the overall jitter of the test setup with a noiseless source (NS) at the input. Only then can we remove the intrinsic jitter of the test setup from our results.

To calibrate with a noiseless source, obtain $X_{NS}(f)$ (Fourier transform of the phase jitter of a noiseless source) as in (1) and measure the signal slew rate seen by the test setup of both the noiseless source, SR_{NS}, and the signal under test, SR_{DUT}. The phase noise power spectrum measured by the noiseless source is

$$|X_{NS}(f)| = \sqrt{X_{NS}(f)X_{NS}{}^{*}(f)}$$

The additive phase noise from the measurement setup is (see section 3.2 for variable definitions):

$$|X_e(f)| = \frac{SR_{NS}}{SR_{DUT}}\sqrt{X_{NS}(f)X_{NS}{}^{*}(f)} = \frac{SR_{NS}}{SR_{DUT}}|X_{NS}(f)|.$$

The above equation corrects for the DSO intrinsic noise sensitivity to input slew rate. Phase noise filtered with a transfer function H(f), is given by $PN_f(f)$ where

$$PN_f(f) = 10log_{10}\left[(2\pi v_0 \frac{|X(f)||H(f)|}{\sqrt{\Delta f}})^2\right].$$

Filtering the phase noise of the DUT and the noiseless source (NS) as shown above yields:

$$PN_{DUT}(f) = 10log_{10}\left[(2\pi v_0 \frac{|X_{DUT}(f)||H(f)|}{\sqrt{\Delta f}})^2\right]$$

$$PN_{add}(f) = 10log_{10}\left[(2\pi v_0 \frac{SR_{NS}}{SR_{DUT}}\frac{|X_{NS}(f)||H(f)|}{\sqrt{\Delta f}})^2\right]$$

We can calculate the RMS jitter as

$$Tj_{DUT} = \frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2} 10^{PN_{DUT}(f)/10}df}$$

$$= \frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2}(2\pi v_0 \frac{|X_{DUT}(f)||H(f)|}{\sqrt{\Delta f}})^2 df}$$

$$Tj_{add} = \frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2} 10^{PN_{add}(f)/10}df}$$

$$= \frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2}\left(2\pi v_0 \frac{SR_{NS}}{SR_{DUT}}\frac{|X_{NS}(f)||H(f)|}{\sqrt{\Delta f}}\right)^2 df}$$

$$= \sqrt{\frac{SR_{NS}}{SR_{DUT}}}\frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2}(2\pi v_0 \frac{|X_{NS}(f)||H(f)|}{\sqrt{\Delta f}})^2 df} = \sqrt{\frac{SR_{NS}}{SR_{DUT}}}Tj_{NS}$$

The calibrated phase noise measurement (after removal of intrinsic noise), PN_m is then:

$$PN_m(f) = 10log_{10}\left[(2\pi v_0 \frac{|X_{DUT}(f)||H(f)|}{\sqrt{\Delta f}})^2 - (2\pi v_0 \frac{SR_{NS}}{SR_{SUT}}\frac{|X_{DUT}(f)||H(f)|}{\sqrt{\Delta f}})^2\right]$$

RMS jitter from the measurement is then

$$Tj_m = \frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2} 10^{PN_m(f)/10} df}$$

$$= \frac{1}{2\pi v_0}\sqrt{2\int_{f_1}^{f_2}\left[\left(2\pi v_0 \frac{|X_{DUT}(f)||H(f)|}{\sqrt{\Delta f}}\right)^2 - \left(2\pi v_0 \frac{SR_{NS}}{SR_{DUT}} \frac{|X_{DUT}(f)||H(f)|}{\sqrt{\Delta f}}\right)^2\right] df}$$

$$= \sqrt{\left(\frac{1}{2\pi v_0}^2\right) 2\int_{f_1}^{f_2}\left(2\pi v_0 \frac{|X_{DUT}(f)||H(f)|}{\sqrt{\Delta f}}\right)^2 df - \left(\frac{1}{2\pi v_0}^2\right) 2\int_{f1}^{f2}\left(2\pi v_0 \frac{SR_{NS}}{SR_{DUT}} \frac{|X_{DUT}(f)||H(f)|}{\sqrt{\Delta f}}\right)^2 df}$$

$$= \sqrt{(Tj_{DUT})^2 - (Tj_{add})^2}$$

$$= \sqrt{(Tj_{DUT})^2 - \left(\frac{SR_{NS}}{SR_{DUT}} Tj_{NS}\right)^2}$$

This equation must be ≥ 0. Therefore, we can determine the conditions where this equation is valid by solving the following equation

$$0 \le \sqrt{(Tj_{DUT})^2 - \left(\frac{SR_{NS}}{SR_{DUT}} Tj_{NS}\right)^2}$$

$$0 \le (Tj_{DUT})^2 - \left(\frac{SR_{NS}}{SR_{DUT}} Tj_{NS}\right)^2$$

$$\left(\frac{SR_{NS}}{SR_{DUT}} Tj_{NS}\right)^2 \le (Tj_{DUT})^2$$

$$\left(\frac{SR_{NS}}{SR_{DUT}}\right) \le \left(\frac{Tj_{DUT}}{Tj_{NS}}\right)$$

References

1. Schwartz; *Information Transmission, Modulation and Noise*, 3rd ed.; McGraw Hill; 1980
2. Papoulis; *Probability, Random Variables, and Stochastic Processes*; McGraw Hill; 1965
3. Papoulis; *Signal Analysis*; McGraw Hill; 1977
4. Clementi; *Reference Clock Measurement Limits for PCIe Gen2*; IDT; 2006
5. IEEE; *IEEE Standard Definitions of Physical Quantities for Fundamental Frequency and Time Metrology—Random Instabilities*; IEEE; 1999
6. Lance, Seal, Labaar, *Phase Noise and AM Noise Measurements in the Frequency Domain, Infrared and Millimeter Waves, Vol. II*, 1984
7. Weigandt, Kim, Gray. *Analysis of Timing Jitter in Ring Oscillators*. IEEE ISCAS 1994
8. *PCIe SIG Measurement Specification*
9. Ron Wade, John Hsu, Jagdeep Bal; *PCIe Reference Clock Measurement Methods for PCIe and Their Limits*; PCIe SIG presentation, September, 2017
10. Ron Wade, John Hsu, Jagdeep Bal, Joe Tajnai; *Appendix - PCIe Reference Clock Measurement Methods for PCIe & Their Limits*; September, 2017

Revision History

Revision Date	Description
August 5, 2020	Initial release.

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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