The Evolution of SAR ADCs for High Sampling Rate Applications

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Abstract

The appetite for quick-access mobile content has always been in demand. With the surge in the number of connected devices increasing year on year, the heart of these connections is the Analog-to-Digital Converter (ADC) in the Analog Front End (AFE). The choice of ADC architecture depends on the end application with the SAR ADC consistently the most energy-efficient, compact, and popular. There are numerous SAR ADC architectures from SAR-Assisted Pipeline topologies to pure SAR. In this white paper we examine several different architectures and discuss their benefits.

Contents

Introduction

The appetite for quick-access mobile content has always been in demand. With the arrival of the Internet of Things, this demand is continuing to grow. Year on year, the number of connections are increasing, with IHS Markit data suggesting that the number of connected IoT devices will surge to 125 billion by 2030. At the heart of these connections is the analog-to-digital converter (ADC) which resides in the Analog Front End (AFE).

In a recent paper, we discussed the various architectures that are used in AFEs where the main requirement is low latency and low power. We believe that the Successive Approximation Register (SAR) ADC – one of the most energy-efficient, compact, and popular ADC architectures – is the best fit for those applications.

SAR ADC resolution can be as high as 18-bit, making it suitable for high-accuracy measurements. Sampling rates can go up to tens of MS/s (10^6 samples per second). Being a highly flexible and low-power architecture, the SAR ADC is an ideal solution for mobile radio AFEs. However, the demand for always higher bandwidths, driven by internet mobile and broadband data access by consumers, is pushing the sampling rate limits beyond those a SAR ADC can achieve.

The millimetre wave technology for 5G cellular network equipment requires converters operating at GS/s (10^9 samples per second). This can be achieved only with time-interleaved ADC architectures. Although such architectures increase the sampling rate limits significantly, they also increase the complexity and require additional calibration algorithms which are not suitable for all applications.

We will look at time-interleaved ADCs in more detail in a future paper, but here we will discuss an alternative for those applications and technologies which do not need GS/s, but need more than tens of MS/s. Some of these technologies include LTE-A, NB-IoT, 802.11ax (wireless) or G.Fast, G.hn, DSL (wireline), VSIS (analog video),

and even 5G cellular network in the sub-6GHz frequency range. For this significant number of applications and technologies, the answer lies in an evolution of the SAR ADC: the SAR-Assisted Pipeline ADC.

The SAR-Assisted Pipeline ADC architecture, which combines the architecture of a traditional Pipeline ADC with that of a SAR ADC, extends the SAR ADC max sampling rate and improves energy-efficiency, while keeping all the competitive advantages of the SAR ADC.

At Renesas, formerly Dialog, we have been investing for many years in the development of new ADC architectures to support both our customers who license our technology for use in their own systems, and also for our customers who engage with us to bring their product vision to reality through a custom ASIC. Renesas has a comprehensive portfolio of silicon proven SAR-Assisted Pipeline ADCs, available in multiple processes and geometries, and optimized for these technologies.

In this article we look in more detail at these architectures and how they are paving the way for the development of the next generation of mobile products.

Successive Approximation Register (SAR) ADC

Figure 1 shows the block diagram of a Successive Approximation Register (SAR) ADC. The analog input signal is sampled, and it is then compared to successive reference voltages by a single comparator working at a higher frequency than the sampling rate.

The successive approximation register name is related to the binary search algorithm used to find the digital output code representative of the input signal.

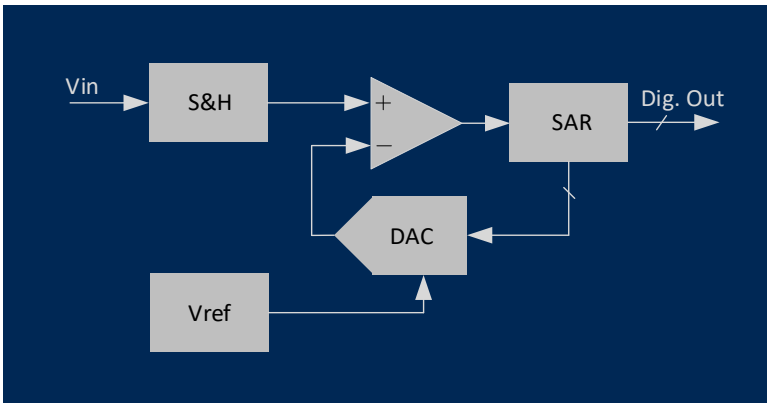

Fig.1: SAR ADC Block Diagram

Figure 2 represents the time steps of a 3-bit SAR ADC.

After the signal is held, the comparator compares that signal to the mid-scale of the input range, in this case, VREF/2. As the signal voltage level is higher than mid-scale, the comparator outputs “1”. This is the first comparator decision which corresponds to the MSB (Most Significant Bit). Based on this decision, the SAR digital block reconfigures the DAC for the next decision to be VREF/2 + VREF/4.

The next comparator decision is “0” (the input held signal is lower than VDAC), indicating that the DAC voltage must be reduced. For the next decision, the SAR digital block reconfigures the DAC to VREF/2 + VREF/4 - VREF/8.

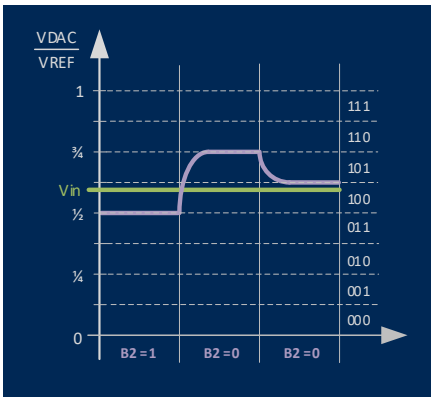

Fig.2: Successive approximation register: example for a 3-bit ADC

The last decision is still “0”, as the input signal is still lower than VDAC. This is the LSB (Least Significant Bit).

The resulting output digital word is D[2:0] = “100”.

The SAR ADC is then ready for sampling a new input signal sample to be converted.

Within one sampling period, the comparator needs to make at least as many decisions as the converter resolution, i.e. output number of bits. A higher resolution reduces the maximum sampling rate; the maximum sampling rate depends on how fast the comparator can decide and how fast the SAR logic can run.

The digital output data is available at the end of the sampling period, making the SAR ADC a converter with no latency. This is an ideal feature for multi-channel time-multiplexing conversion, being able to switch input channels as required.

By implementing the comparator with a dynamic topology, the SAR ADC can be implemented without any static bias current. Therefore, when the ADC is not converting, if the clock is stopped, there is no power dissipation. It can switch from idle mode to active mode without any start-up time, making it very power-efficient for applications not requiring full-time continuous operation.

Furthermore, the dynamic power profile allows the sampling rate to scale to any lower frequency with linear scaling of the power dissipation.

In a switched capacitor implementation, the ADC input network equivalent circuit is basically a sampling capacitor and a sampling switch. The sample and hold operation is embedded in the DAC circuitry. The sampling capacitor is sized to meet the noise requirements, and for a 65dB signal-to-noise ratio (SNR) this is around 1 to 2pF. A small switch implemented with a MOS device can have a resistance in the order of tens of ohms. This corresponds to a low-pass filter frequency higher than 1GHz. As such, the SAR ADC is suitable to convert very high frequency signals without requiring very high-power dissipation.

The maximum sampling rate is still limited by the speed of the comparator and logic. For 60+ dB SNR, the SAR ADC maximum sampling rate is limited to tens of MHz’s

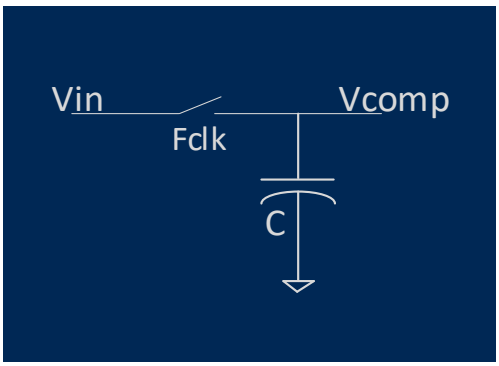

Fig.3: SAR ADC Input Network

SAR-Assisted Pipeline ADC

Figure 4 shows a 2-stage SAR-Assisted Pipeline ADC. It is comprised of two lower-resolution SAR ADC stages and a residue amplifier. The first SAR ADC stage resolves the most significant bits of the digital output word, and usually includes additional redundancy. The residue is amplified and sampled by the second SAR ADC stage. The output of this second stage corresponds to the least significant bits of the SAR-Assisted Pipeline ADC. Before having the digital output data available, it is still required for a digital correction and timing alignment due to the pipelined operation.

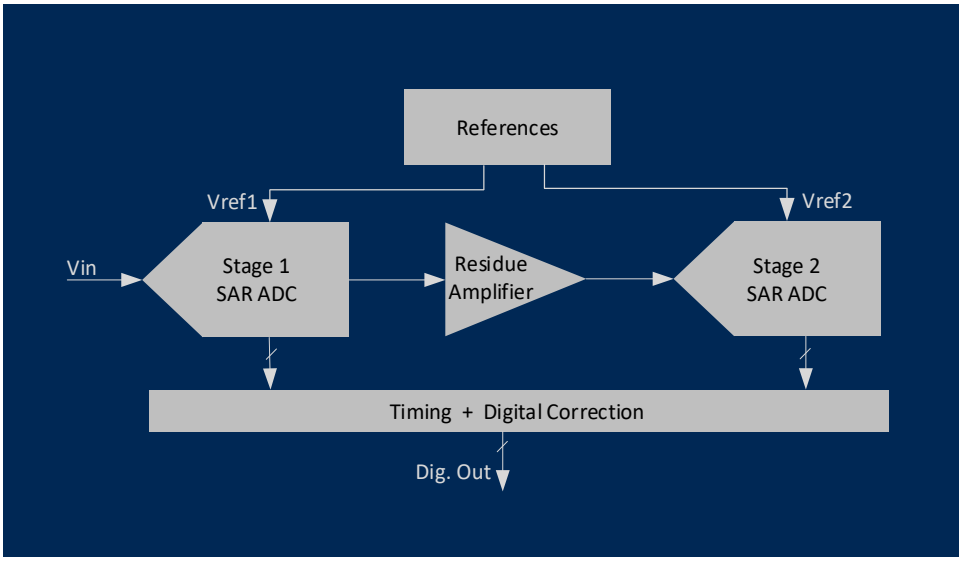

Fig.4: SAR-Assisted Pipeline ADC Block Diagram

The lower resolution of each stage of the SAR ADC allows a faster conversion time per stage. Once the first stage concludes the conversion, the residue is amplified and made available for the second stage. While stage 2 converts this signal, the first stage is already sampling and converting the next sample. This pipelining allows a significant increase in the maximum sampling rate when compared to a single SAR solution.

The residue amplifier gain relaxes the requirements for the second stage, which contributes to a significant reduction in the area and power of that stage. As such, although the residue amplifier itself dissipates power during the amplification, the overall solution remains extremely competitive and even more energy-efficient that the SAR ADC itself.

As for the SAR comparator, the residue amplifier can also be implemented with a fully dynamic topology, resulting in a converter without static current. The start-up time, duty-cycle power efficiency and power scaling, along with the frequency advantages of the SAR remain valid for the SAR-Assisted Pipeline ADC.

A critical block in any high accuracy ADC, is the reference voltage generation. In the SAR ADC, the reference voltages are used to compare against the input signal at each decision step. Although some techniques can be used to relax some of the reference voltage accuracy requirements, in general, this reference must be as accurate as the ADC accuracy specification. For high sampling rate, high-accuracy converters, having the reference voltage generated locally, close to the ADC, is extremely important. Generating this voltage outside the chip leads to performance degradation due to noise coupling and voltage ripple related to the non-negligible inductance and resistance at the bonding and package pads. Optimized and efficient reference voltage generation and buffering are critical for a robust, energy-efficient, and highly accurate converter.

Figure 5 shows our SAR-Assisted Pipeline ADC block diagram. This is a self-contained IP block, including the references generation and buffering, bias generation, timing, and calibration.

The ADC itself is supplied with the technology core supply (AVDD for the analog core and DVDD for the digital core). The I/O supply AVDDIO is used for the reference voltage generation and buffering. In order to generate a clean, noiseless reference, this block includes several filtering structures and all the supply domains include distributed internal decoupling capacitance. A deep n-well is used for all the analog section to improve immunity to substrate noise. This solution provides a very robust design with high immunity to supply and to substrate noise. This is particularly relevant when the IP is licensed to be included in the customers' SoC (System-On-Chip) where a clean, analog dedicated supply may not be available.

For IP licensing, having the full functionality included in the IP (converter, bandgap, reference buffers, biasing, filters, timing, and calibration) is very helpful for simple and successful integration. It also provides a less expensive solution, as there is no need for additional external voltage regulators or accurate references, and it does not require additional on-chip die area for decoupling capacitance.

The built-in digitally assisted calibration does not require any external signals and can be run automatically at start-up, making the IP functionality / interface very simple.

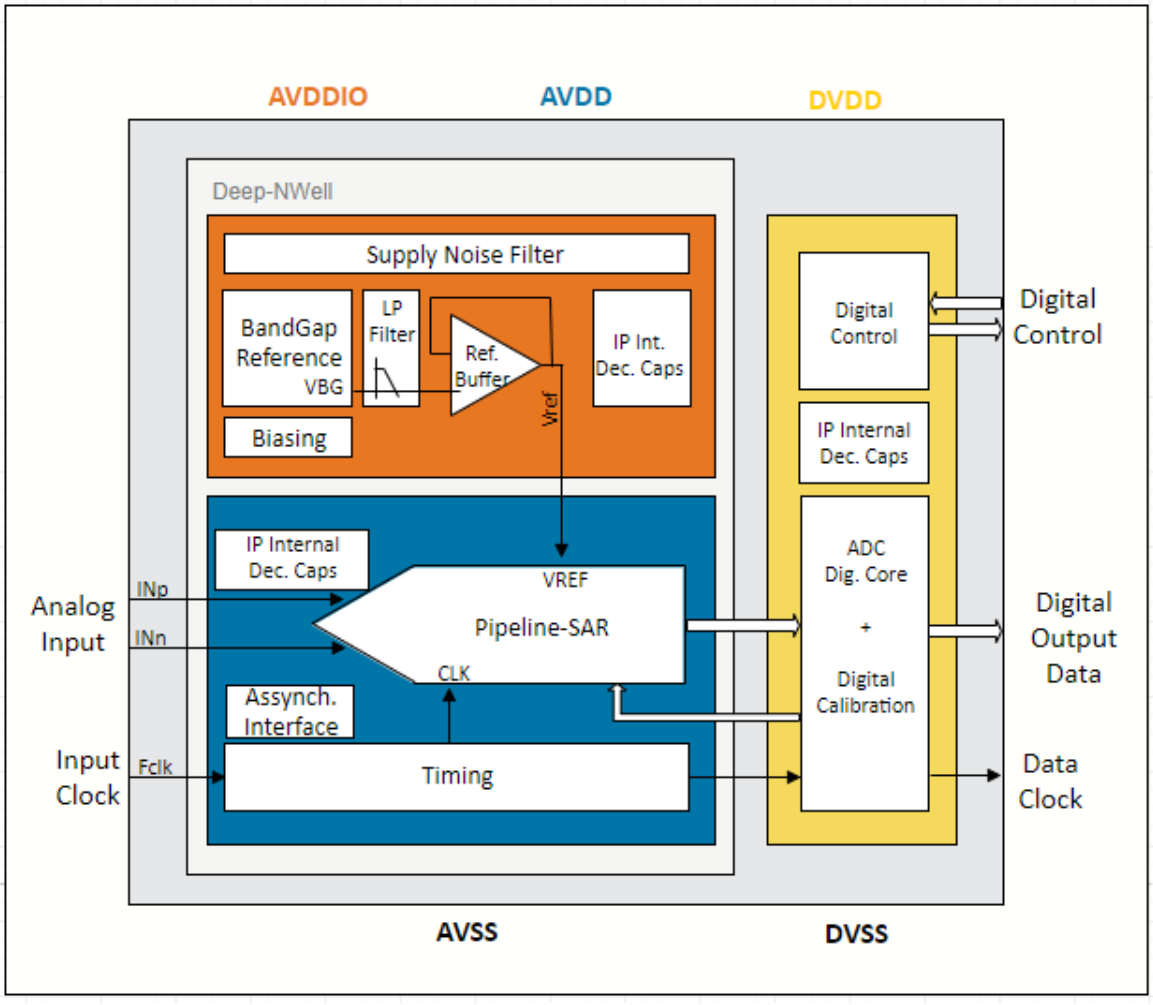

Fig.5: Renesas' SAR-Assisted Pipeline ADC

Figure 6 shows the dual-channel ADC IP version of the SAR-Assisted Pipeline ADC where some blocks are shared by both channels, resulting in power and area savings. This IP can be used for quadrature I/Q modulation architectures. Additional calibration is included for the I/Q matching.

To minimize any crosstalk between the channels, each has its own reference buffer. A dedicated internal clock-tree for each channel is also included, although there is a single input clock to the IP. The supplies are also shared by both channels without any crosstalk degradation.

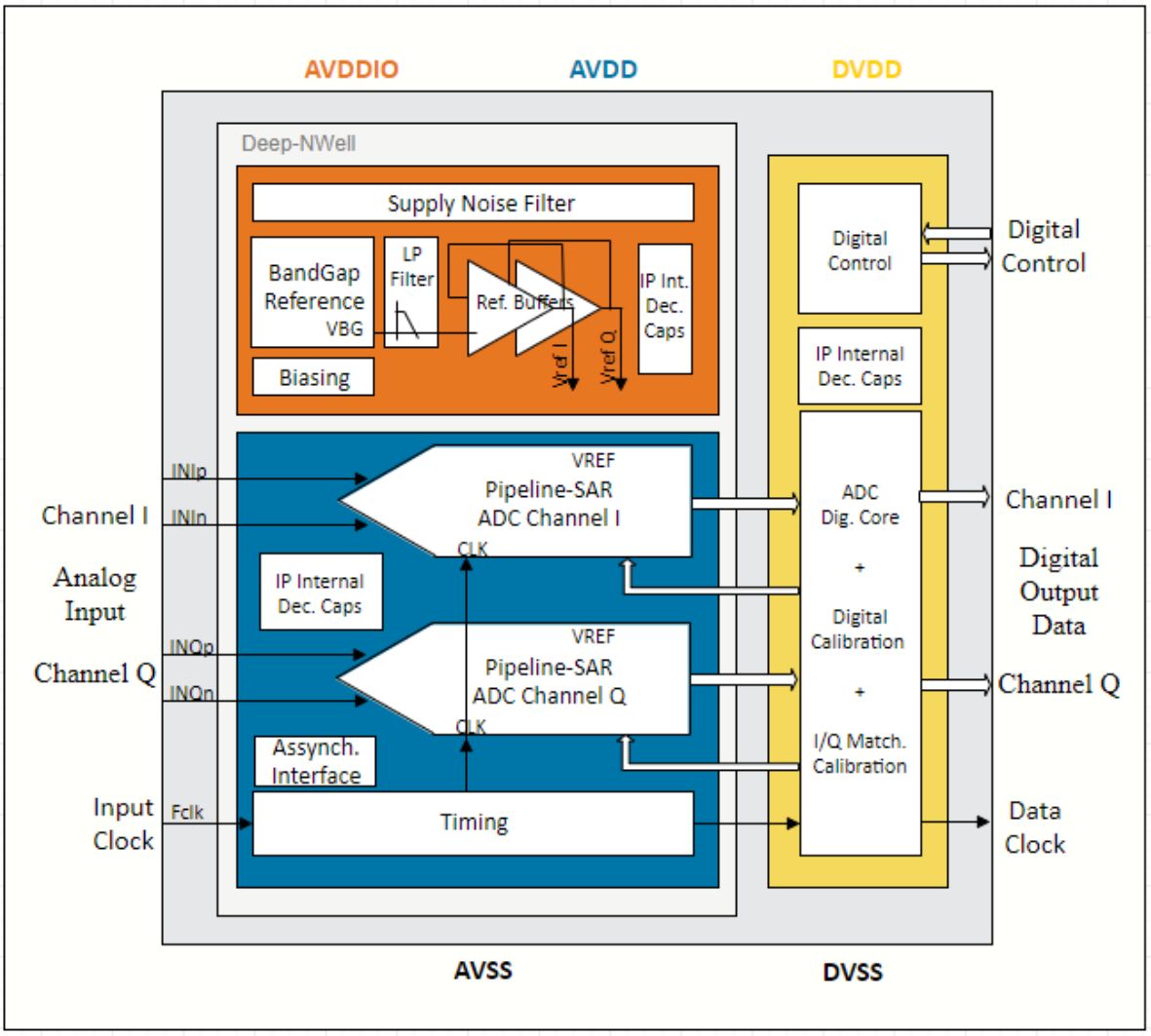

Fig.6: Renesas' SAR-Assisted Pipeline I/Q ADC

Renesas' SAR-Assisted Pipeline ADCs

We present a few examples of our SAR-Assisted Pipeline ADCs in this section.

S3ADSIQ160M12BSM28PSB is a dual-channel ADC in a 28nm process with a sampling rate per channel up to 160MS/s.

With standby mode and a power-down mode, it can be used very power efficiently. It can be configured as single channel or dual channel converter. With the 2 channels converting continuously at 160M/s, the IP block's total power dissipation is only 18mW, with about 50% current from the 1.05V supply and 50% current from the 1.8V supply. Each ADC channel has a performance of 63.1dB SNDR and, with both channels converting simultaneously, the crosstalk between channels is below -80.0dB.

This is an extremely compact IP with a total die area of 0.055mm^2.

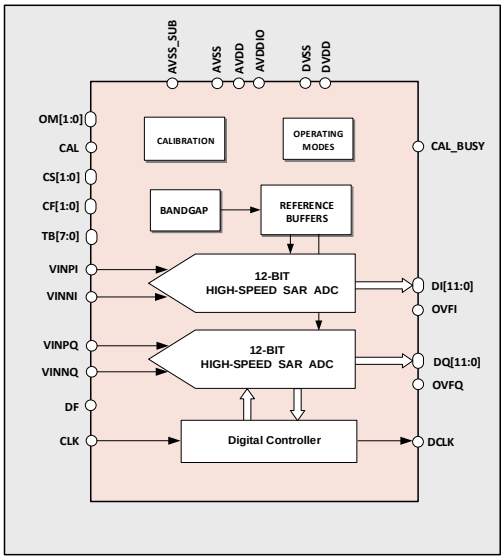

Fig.7: *S3ADSIQ160M12BSM28PSB* Block Diagram

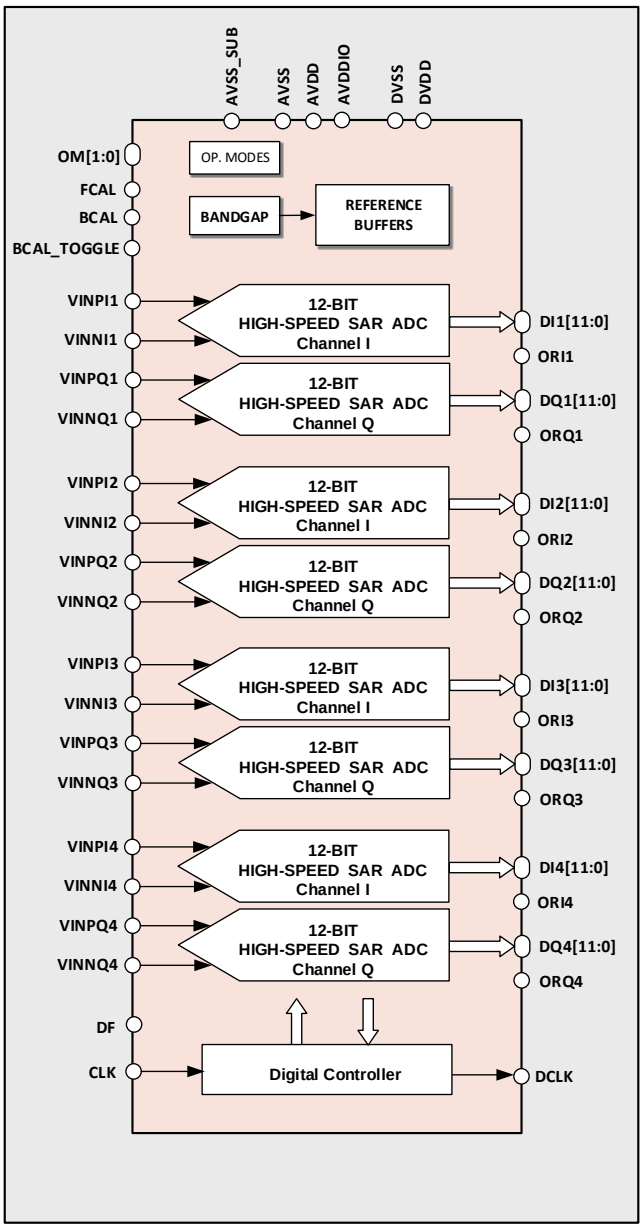

Fig.8: *S3ADS4IQ122M12BSS28LPP* Block Diagram

S3ADS4IQ122M12BSS28LPP is an octal-core ADC with 4 I/Q channels sampling simultaneously at 122.88MS/s.

All the parallel channels are supplied with a single AVDDIO=1.8V, AVDD=1.0V and DVDD=1.0V supply. A very optimized power supply rejection ratio design allows parallel conversion with shared supplies without interference between channels.

A single input clock is also shared for all the channels, but individual clock-trees were also designed for each channel for improved performance.

Likewise, there is a single bandgap, but each channel has its own reference buffer.

The complete IP, with 8 ADCs converting simultaneously, dissipates only 45mW power with a performance of 10.2-bit ENOB. It has a highly compact die area of 0.3mm^2.

S3ADS200M12BT28HPCP is a SAR-assisted Pipeline 12-bit ADC with a sampling rate of 200MS/s.

Supplied with 2.5V I/O and 0.9V core, its power dissipation is only 10mW, when converting continuously at 200MS/s.

Despite the larger 2.5V I/O devices, the total area of the IP is only 0.05mm^2.

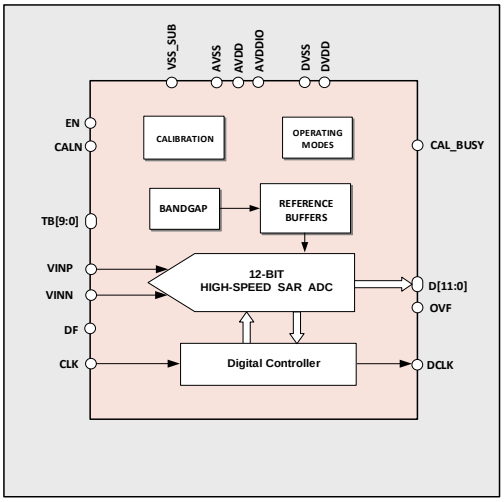

Fig.9: *S3ADS200M12BT28HPCP* Block Diagram

Conclusion

The Analog to Digital Converter (ADC) is a key component in any Analog Front End (AFE). The ADC architecture chosen depends on the end application for which the AFE is being used. There have been many developments in terms of various architectures available, and none more so than with the SAR ADC which has shown to be the most energy-efficient, compact, and popular. ADC architectures have evolved over time from the SAR to the influence of this architecture in the creation of the SAR-Assisted Pipeline ADC. In future papers we will discuss the continuation of this evolution to the Time Interleaved SAR ADC for development of products for the 5G market. Regardless of the ADC architecture that is required, and whether you are developing your own system or working with Renesas, formerly Dialog to use this ADC IP in the generation of a custom ASIC, Renesas has the experience and the ADC IP offering to suit your needs.

Revision History

Revision	Date	Description
1.0	Nov 11, 2019	Initial release
1.1	Dec 22, 2021	Re-brand