White Paper

Advantages of Using Gallium Nitride FETs in Satellite Applications

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Abstract

Silicon FETs have long since dominated the space and high reliability industry, but they are quickly approaching their theoretical limit of performance. To move forward, we need to look towards wide bandgap semiconductors. Gallium Nitride (GaN) FETs have several advantages, such as size, weight and efficiency, over traditional Silicon FETs. GaN FETs have shorter distances between the source and drain, which translates to a much smaller die and lower resistance (reduced conduction losses). The smaller die, thereby, leads to fewer parasitics such as output capacitance and layout inductances, which results in lower switching losses. The combination of lower switching and conduction losses enables much higher efficiencies. The more efficient a converter is, the less the power gets dissipated into heat, resulting in fewer heat sinking requirements that, thus, reduce the weight of the overall power supply. The one key trait of GaN FETs that is different from Silicon FETs is the fact that the GaN's gate-source voltage can never exceed 6V. Most radiation hardened FET drivers on the market provide drive voltages in excess of 10V (to support Silicon FETs), which are damaging for GaN. A gate driver that can level shift the 10V+ signal down to acceptable levels for GaN would help increase the adoption rate of GaN in the space and high-reliability industry.

Introduction

Despite the fact that the satellite industry tends to lag on new technology adoption, in general, this industry has been very interested in, and has already deployed, next-generation Gallium Nitride (GaN) technology for RF and switching applications. An application where GaN often hasn't been deployed is power management, in which the advantages of GaN performance can be realized even more so. What was needed to enable this adoption has been missing up until now. With enhancement mode GaN FET availability, and now radiation-hardened ground-up designed GaN FET driver availability, GaN deployment in power management applications can be realized. Substantial improvements in board space savings and power efficiency are now possible with these products due to GaN FET best-in-class gate-charge performance and higher switching frequency capability. GaN FET performance and GaN FET driver solution details will be discussed in more detail in this paper.

Characteristics of GaN FETs

There are several characteristics of GaN FETs that make them attractive for use in power supplies in satellites; i.e., the physical attributes (inherent radiation tolerance[1] and small die size), electrical characteristics (no parasitic p-n diode and fast switching), and power system advantages (increased efficiency and smaller total size) of GaN FETs.

In contrast to silicon MOSFETs, GaN FETs do not have a gate oxide layer and, thus, gamma radiation does not form traps (holes) that might typically form in a gate oxide layer when using silicon MOSFETs. GaN FETs also perform well in single-event effects (SEE) testing[2].

Figure 1 shows the structure of a GaN FET. The starting point is a standard silicon wafer. GaN and other materials are added on top, as shown. Notice that this GaN FET is a lateral device; current flow is horizontal through the GaN 2-dimensional electron gas (as shown by "–" in the diagram).

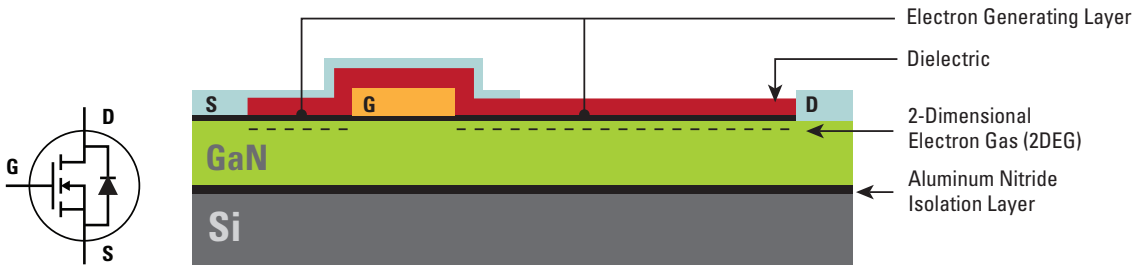

Figure 1. *EPC's GaN Power Transistor Structure*

GaN is a wide bandgap material. Compared with silicon, the separation between the drain and source can, in theory, be a factor of 10 smaller. For the same RDSON, the width of the channel can be much narrower, in part due to the much shorter length. While silicon MOSFETs are very close to their theoretical limit, GaN FETs have room for further improvement, as shown in Figure 2. In addition, for satellite applications, converting standard-production MOSFETs to space-grade MOSFETs causes a performance degradation versus the inherent ability of GaN FETs to meet space applications requirements.

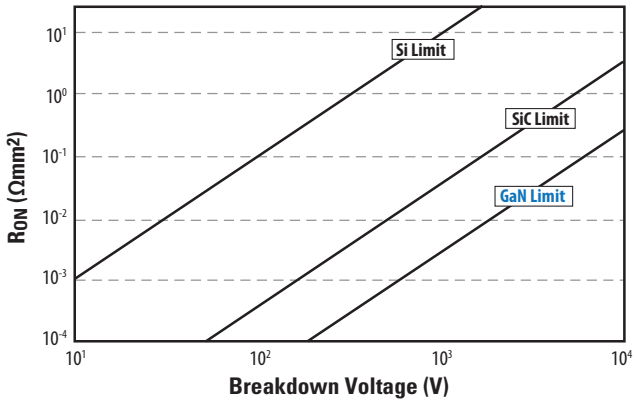

Figure 2. *Resistance vs. Breakdown Voltage*

The smaller die size of a GaN FET, compared to a silicon MOSFET, enables performance improvements in switching power applications. Parasitics such as output capacitance and layout inductance are reduced, leading to reduced switching losses and/or higher frequency operation with the same loss.

GaN FETs do not have a parasitic p-n diode. This is convenient in that there is no reverse recovery. Reverse recovery not only causes a longer dead time to recover the diode charge, it's also a function of several factors such as temperature, current, and length of time the diode conducts. The question comes up: if GaN FETs do not have this element, do they conduct in the reverse direction (from source to drain) when the gate is "off" (Vgs = 0V)? The answer is yes, GaN FETs do conduct in the reverse direction using the same channel they use in the forward direction (not a parasitic element).
The voltage drop of this conduction is greater than the drop of a diode; however, total loss can be minimized by using a very short dead time. Due to no reverse recovery, a dead time in the order of 5-15 nS can be used. In addition, if desired, an optional parallel Schottky diode can be used around a GaN FET (typically a small diode).

Switching Power Supply Applications

GaN FETs allow power supply designers to further optimize their designs. Advantages for the total power supply include size and weight, efficiency, EMI, and, potentially, fewer voltages and higher loop bandwidth.

Size and Weight: The fast switching and reduced parasitics lead to fewer losses for each switching cycle. The power supply designer can choose how to use this advantage – either raise the frequency, increase the efficiency, or a balance of both (higher frequency and simultaneous higher efficiency). While GaN FETs themselves are smaller than equivalent MOSFETs, especially for satellite applications, the smaller size and weight of the overall power supply is highly beneficial. Increased efficiency can result in reduced size/weight of heat sinking, as well as a reduced draw from the power source. Increased frequency can result in smaller inductors and capacitors, and with inductors, a reduced value of inductance may result in lower copper losses.

Efficiency: Due to the ability to efficiently raise the switching frequency, the speed of the feedback loop can also be made faster if desired. The advantages of faster transient response include the possibility of reducing the size of the output capacitance because the power supply would have the ability to respond quicker to a load change, and thus, not need as much energy from the output capacitors to "ride out" the effect of the transient.

EMI: Increasing frequency and switching speed may seem to increase the issue of EMI, but GaN can have advantages even here. Reduced parasitics mean less energy stored and released in these parasitic elements during each switching cycle. In addition, due to the smaller size, the board layout can be improved to reduce the loop inductance. Below is an example switching waveform taken from a power supply half-bridge evaluation board[3]. Note that even though this buck converter has fast rise and fall times, the voltage overshoot is low due to an optimized layout.

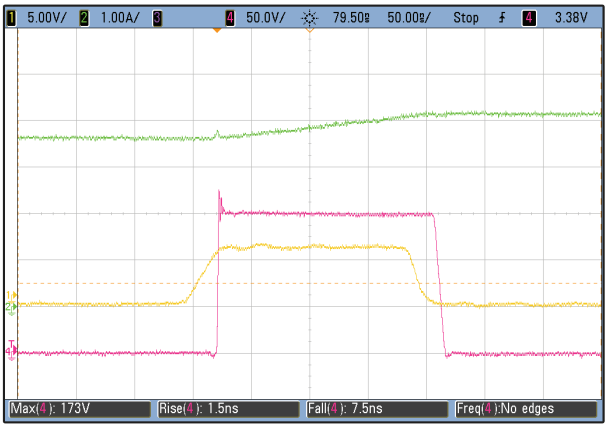

***Figure 3**. Waveforms for 150 VIN to 5 VOUT @ 4A (200 kHz) Buck Convertor.*
CH1: VPWM Input Voltage, CH2: Inductor Current, CH4: VOUT Switch Node Voltage

Gate Driver

To use GaN FETs to their full advantage, a specialized gate driver that is fast and regulated to the ideal drive voltage is needed. The maximum gate voltage allowed is 6V, and most commercial-grade application GaN FET drivers use 5V as the drive voltage. However, for satellite and high-reliability applications, an increased voltage margin is often required. The ideal gate drive voltage for these applications is 4.5V. This voltage has minimal impact on RDSON versus a 5V gate drive. In a worst case situation, using a drive voltage less than 4.5V nominal could cause the RDSON to increase too much. The curves in GaN datasheets are for typical devices and should not be interpreted as "a nominal gate drive voltage of 4V or less is a good choice".

Most FET controllers and drivers on the market today provide drive voltages in excess of 10V, which would damage the gates of GaN FETs. Having a driver that can accept MOSFET voltage levels and level shift them down to a 4.5V gate drive would be ideal so as to take advantage of the readily available controllers on the market and allow one to merely swap out the FET. There are two important factors to examine when considering a driver: does it have a well-regulated gate drive when switching, and how does it ensure the GaN FET will stay off when it should.

A well-regulated gate drive will maintain the gate voltage regardless of its supply line and output load variations. The nature of a driver is such that it needs to be able to provide amps of current within a short time repeatedly. This is usually achieved by tuning the compensation of the internal regulator for a given output capacitance. As this is usually taken care of by the IC manufacturer, the real challenge here is dealing with any stray inductance in the line between this output capacitance and the gate of the GaN FET. Amps of current in short periods of time result in large voltage transients that can be damaging to its gate. To get around this, we first ensure that the copper trace between the driver's output and the gate of the FET is as short as it can possibly be. Here's an example of an optimized layout for a low side application:

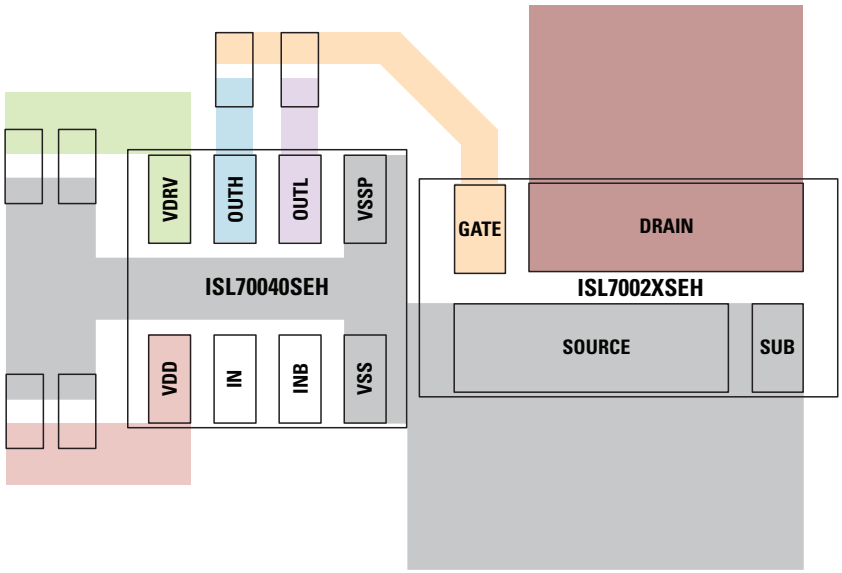

Figure 4. *Optimized layout for minimizing inductance in the gate drive loop; the gate loop is as thick and short as it can be. The path to minimize is from VDRV (green) through OUTH (blue) to the Gate (orange) and back down to VSSP (grey) via OUTL (purple).*

The next task is to ensure that the gate return loop's inductance is also minimized. In the example above, the gate return (Substrate) is merged with the source plane to achieve this. If there are still undesirable voltage spikes on the gate waveform once the layout is taken into account, the gate resistors can be increased to compensate.

It is important to make sure that the driver has a fail-safe built in that will turn off the FET if something goes wrong. If the inputs somehow are no longer driven, they should settle in a state that shuts off the FET. Another situation in which to keep the switch off is when the gate drive voltage is not high enough to drive the GaN with its optimal RDSON. Here's a block diagram of a GaN FET driver that could achieve that:

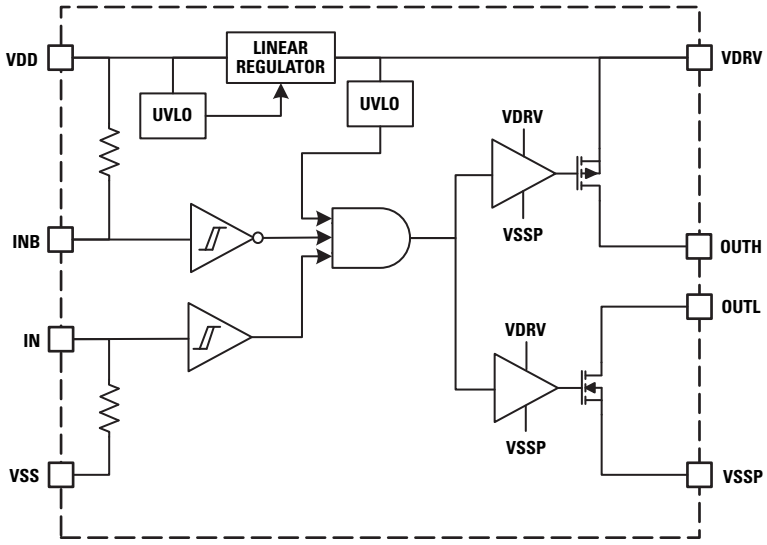

Figure 5. *Block Diagram for the ISL70040SEH*

Apart from the technicalities that encompass designing a robust low-side gate driver, designing for satellite systems poses some unique hurdles to overcome. For satellites to function as intended in orbit, their components need to maintain proper operation with prolonged exposure to Low Dose Rate (LDR) and Total Ionizing Dose (TID), as well as handle interactions with ionized particles (such as heavy ions) in space. Having a GaN FET driver that doesn't flip states when a heavy ion deposits a charge on a junction or have its device threshold shift with HDR and LDR TID is something that must be mitigated in the IC design and process design phases. Here are some graphs that show what a driver can do when it's designed from the ground up for space (as opposed to a commercial up-screened IC).

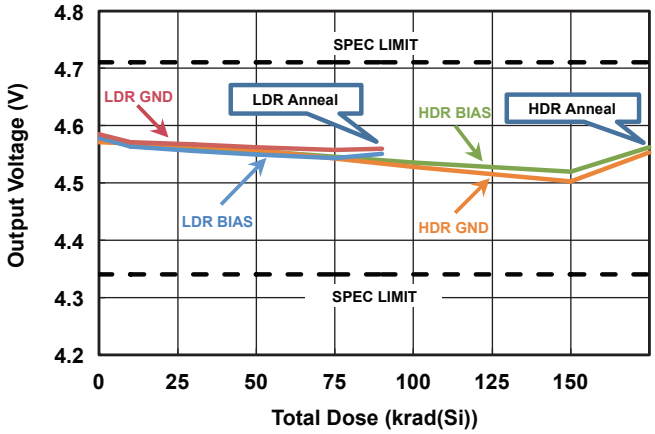

Figure 6. *ISL70040SEH Gate Drive Voltage vs. High Dose Rate (50-300 rad(Si)/s) and Low Dose Rate (<10 mrad(Si)/s)*

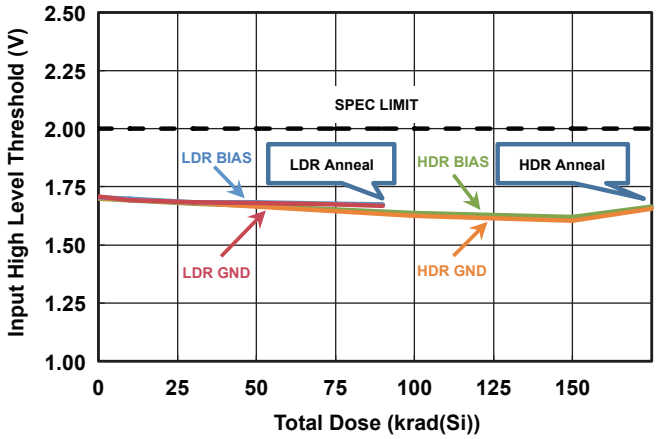

Figure 7. *ISL70040SEH Input Logic High Thresholds vs. High Dose Rate (50-300 rad(Si)/s) and Low Dose Rate (<10 mrad(Si)/s)*

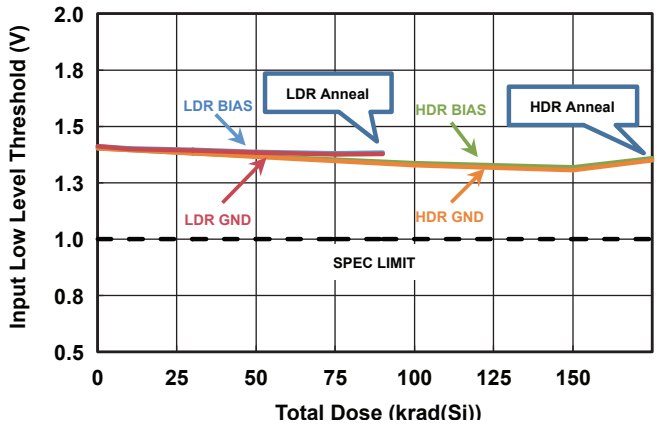

Figure 8. *ISL70040SEH Input Logic Low Thresholds vs. High Dose Rate (50-300 rad(Si)/s) and Low Dose Rate (<10 mrad(Si)/s)*

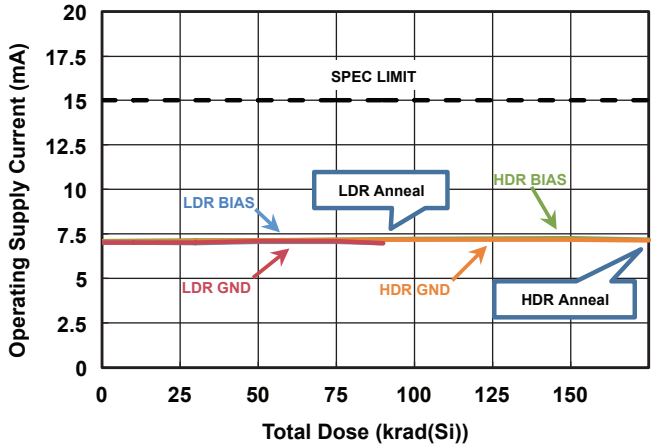

Figure 9. *ISL70040SEH Operating Supply Current vs. High Dose Rate (50-300 rad(Si)/s) and Low Dose Rate (<10 mrad(Si)/s)*

For the device shown above, at an LET of 86 MeV•cm2/mg, there were no Single Event Transients recorded with a static input, and for a dynamic input at 500kHz where SETs were defined as a ±20 ns perturbation in pulse width, it had a very small cross section of $\leq 1.7 \times 10^{-6} cm^2$.

Conclusion

GaN FETs are a very good fit for satellite applications, but require a good gate driver to realize their full potential. Together, they allow more efficient switching, higher frequency operation, reduced gate drive voltage, and smaller solution sizes compared to the traditional silicon counter parts.

Footnotes:

[1] HEMTs In Space – A New Take On Rad Hardness, Compound Semiconductor, https://compoundsemiconductor.net/article/99757-HEMTs-in-space-a-new-take-on-rad-hardness.html

[2] Alex Lidow et al, GaN Transistors for Efficient Power Conversion, Wiley, 2015, p. 172-178.

[3] EPC9014 Quick Start Guide, EPC, page 2 Figure 4.

Document No.: R18WP001-EU0000-FET-GATE-DRIVER