

致尊敬的顾客

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瑞萨电子公司网址：<http://www.renesas.com>

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瑞萨电子公司

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CMOS 逻辑 HD74AC 系列 (FACT)

规格的定义

* FACT 是美国国家半导体公司的注册商标。

1. AC 负载项目和测量波形

1.1 绝对最大额定值

项目	符号	额定值	单位	条件
电源电压	V_{CC}	-0.5 to 7.0	V	
DC 输入二极管电流	I_{IK}	-20	mA	$V_I = -0.5V$
		20	mA	
DC 输入电压	V_I	-0.5 to $V_{CC}+0.5$	V	$V_I = V_{CC}+0.5$
DC 输出二极管电流	I_{OK}	-50	mA	$V_O = -0.5$
		50	mA	$V_O = V_{CC}+0.5$
DC 输出电压	V_O	-0.5 to $V_{CC}+0.5$	V	
DC 输出电流	I_O	± 50	mA	
输出引脚的 DC V_{CC} 或 GND 电流	I_{CC} or I_{GND}	± 50	mA	每个输出引脚
保存温度	T_{STG}	-65 to 150	$^{\circ}C$	

【注】绝对最大额定值是指瞬间也不能超过的极限值，是任意 2 个或者 2 个以上的项目都不能同时达到的值。

1.2 推荐工作条件

项目	符号	额定值	单位	条件
电源电压 (没有特别记载其他用途时)	V_{CC}	2.0 to 6.0	V	
输入电压	V_I	0 to V_{CC}	V	
输出电压	V_O	0 to V_{CC}	V	
工作温度	T_a	-40 to +85	$^{\circ}C$	
输入的上升和下降时间'AC 型 (施密特触发器的输入除外) V_{IN} 30% ~ 70% V_{CC}	t_r , t_f	8	ns/V	V_{CC} @ 3.0V
				V_{CC} @ 4.5V
				V_{CC} @ 5.5V
输入的上升和下降时间'ACT 型 (施密特触发器输入除外) V_{IN} 0.8 ~ 2.0V	t_r , t_f	8	ns/V	V_{CC} @ 4.5V
				V_{CC} @ 5.5V

1.3 DC特性 (AC系列)

项目	符号	V _{CC} (V)	Ta=25°C			Ta=-40~+85°C		单位	条件	
			min.	typ.	max.	min.	max.			
输入电压	V _{IH}	4.5	2.0	1.5	—	2.0	—	V	V _{out} =0.1V or V _{CC} -0.1V	
		5.5	2.0	1.5	—	2.0	—			
	V _{IL}	4.5	—	1.5	0.8	—	0.8	V	V _{out} =0.1V or V _{CC} -0.1V	
		5.5	—	1.5	0.8	—	0.8			
输出电压	V _{OH}	4.5	4.4	4.49	—	4.4	—	V	V _{IN} =V _{IL} or V _{IH} I _{out} =-50μA	
		5.5	5.4	5.49	—	5.4	—			
		4.5	3.94	0.0001	—	3.80	—	V	V _{IN} =V _{IL} or V _{IH}	I _{OH} =-24mA
		5.5	4.94	—	—	4.80	—			I _{OH} =-24mA
	V _{OL}	4.5	—	0.001	0.1	—	0.1	V	V _{IN} =V _{IL} or V _{IH} I _{out} =50μA	
		5.5	—	0.001	0.1	—	0.1			
		4.5	—	—	0.32	—	0.37	V	V _{IN} =V _{IL} or V _{IH}	I _{OL} =24mA
		5.5	—	—	0.32	—	0.37			I _{OL} =24mA
输入电流	I _{IN}	5.5	—	—	±0.1	—	±1.0	μA	V _{IN} =V _{CC} or GND	
OFF 状态下的 输出电流	I _{OZ}	5.5	—	—	±0.5	—	±5.0	μA	V _{IN} =V _{IL} or V _{IH} V _{out} =V _{CC} or GND	
静态消耗电流	I _{CC}	5.5	—	—	8.0	—	—	μA	V _{IN} =V _{CC} or GND	
消耗电流/输入	I _{CCT}	5.5	—	0.6	—	—	1.5	mA	V _{IN} =V _{CC} -2.1V	
动态输出电流注	I _{OLD}	5.5	—	—	—	86	—	mA	V _{OLD} =1.1V	
	I _{OHD}	5.5	—	—	—	-75	—	mA	V _{OHD} = 3.85V	

【注】 最大试验时间不超过20ms, 并且不能同时对2个或2个以上的输出引脚进行试验。

1.4 DC 特性 (ACT 系列)

项目	符号	V _{CC} (V)	Ta=25°C			Ta=-40~+85°C		单位	条件
			min.	typ.	max.	min.	max.		
输入电压	V _{IH}	4.5	2.0	1.5	—	2.0	—	V	V _{out} =0.1V or V _{CC} -0.1V
		5.5	2.0	1.5	—	2.0	—		
	V _{IL}	4.5	—	1.5	0.8	—	0.8	V	V _{out} =0.1V or V _{CC} -0.1V
		5.5	—	1.5	0.8	—	0.8		
输出电压	V _{OH}	4.5	4.4	4.49	—	4.4	—	V	V _{IN} =V _{IL} or V _{IH} I _{out} =-50μA
		5.5	5.4	5.49	—	5.4	—		
		4.5	3.94	0.0001	—	3.80	—	V	
		5.5	4.94	—	—	4.80	—		
	V _{OL}	4.5	—	0.001	0.1	—	0.1	V	V _{IN} =V _{IL} or V _{IH} I _{out} =50μA
		5.5	—	0.001	0.1	—	0.1		
		4.5	—	—	0.32	—	0.37	V	
		5.5	—	—	0.32	—	0.37		
输入电流	I _{IN}	5.5	—	—	±0.1	—	±1.0	μA	V _{IN} =V _{CC} or GND
OFF 状态下的 输出电流	I _{OZ}	5.5	—	—	±0.5	—	±5.0	μA	V _{IN} =V _{IL} or V _{IH} V _{out} =V _{CC} or GND
静态消耗电流	I _{CC}	5.5	—	—	8.0	—	—	μA	V _{IN} =V _{CC} or GND
消耗电流/输入	I _{CCT}	5.5	—	0.6	—	—	1.5	mA	V _{IN} =V _{CC} -2.1V
动态输出电流注	I _{OLD}	5.5	—	—	—	86	—	mA	V _{OLD} =1.1V
	I _{OHD}	5.5	—	—	—	-75	—	mA	V _{OHD} =3.85V

【注】 最大试验时间不超过2.0ms，并且不能同时对2个或2个以上的输出引脚进行试验。

2. 负载电路

用于规定 FACT 特性和传播延迟时间的 AC 负载电路如图 1 所示。只要没有特别指定其他用途，就使用此负载电路。

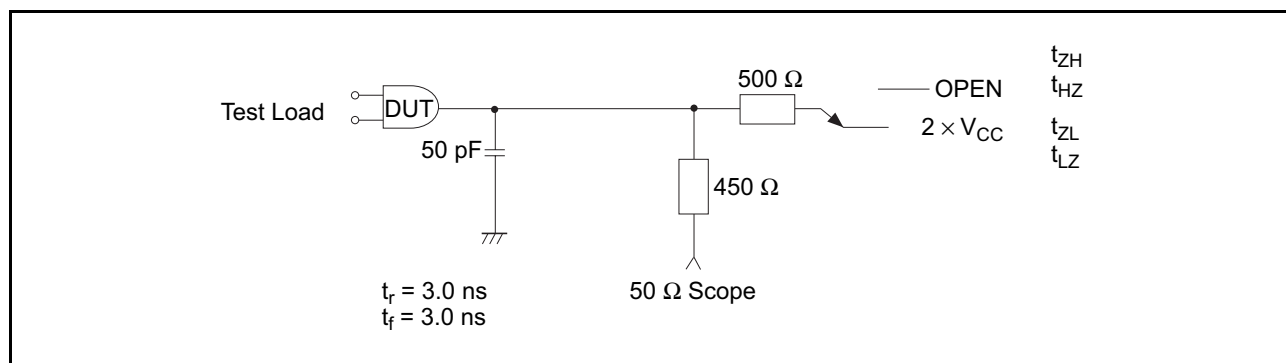


图 1 AC 负载电路

通过使用此负载电路，能减少与用户测量系统相关的问题，同时能为用户提供在实际使用时的更有意义的

对于将传统TTL等的 $C_L=15\text{pF}$ 连接GND的负载电路，为了减小寄生电容，所以在制作测试夹具时需要特别小心，而且还需要使用高输入阻抗和高频探针。

FACT的负载电路为 $C_L=50\text{pF}$ ，在增加寄生电容的容限的同时，起输出信号上升或者下降时的负载作用。此负载电路能为系统设计提供接近于一般应用系统假设的负载并且便于使用的传播延迟时间的数值。

如果负载容量从 15pF 变为 50pF ，传播延迟时间就变为 1ns 左右的大数值，连接到GND的 500Ω 电阻就能被视为示波器的无源探针。换言之，连接GND的 500Ω 电阻能被视为通过 450Ω 的电阻和 50Ω 的同轴电缆，串联到内部连接了 50Ω 终端电阻的采样示波器。器件的输入引脚应该通过相同阻抗的电缆连接到采样示波器的另一个输入端。相当于脉冲发生器的信号输出端连接了一个 50Ω 的终端电阻。

在图1的电路中，在测量器件的输出引脚和开关之间连接了另一个 500Ω 的电阻。在大部分测量时，此开关为断开状态；在测量三态输出的允许时间和禁止时间（Low→OFF或者OFF→Low）时，此开关为闭合状态。在开关闭合后， $2\times V_{CC}$ 电压被2个 500Ω 的电阻分压，输出引脚的电压变为静态High电平。

3. 试验条件

FACT试验时所使用的输入信号的电压电平如图2和图3所示。AC试验的条件和其他族一样，AC和ACQ系列的“Low”电平为 0V ，“High”电平为 V_{CC} ；ACT系列的“Low”电平为 0V ，“High”电平为 3V 。

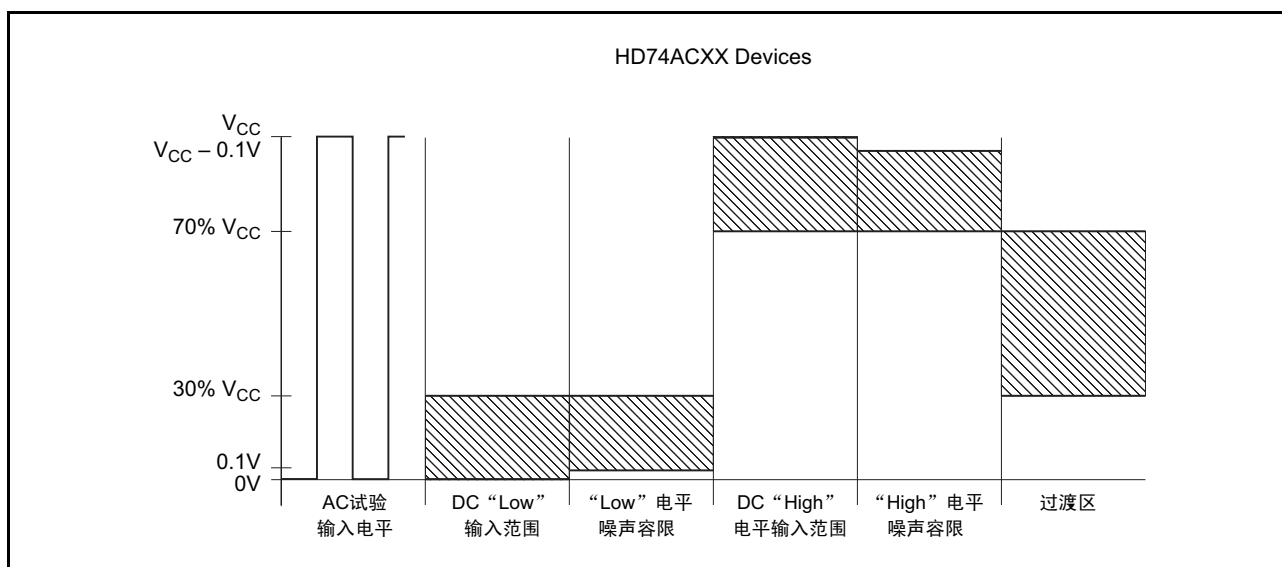


图2 输入信号的电压电平

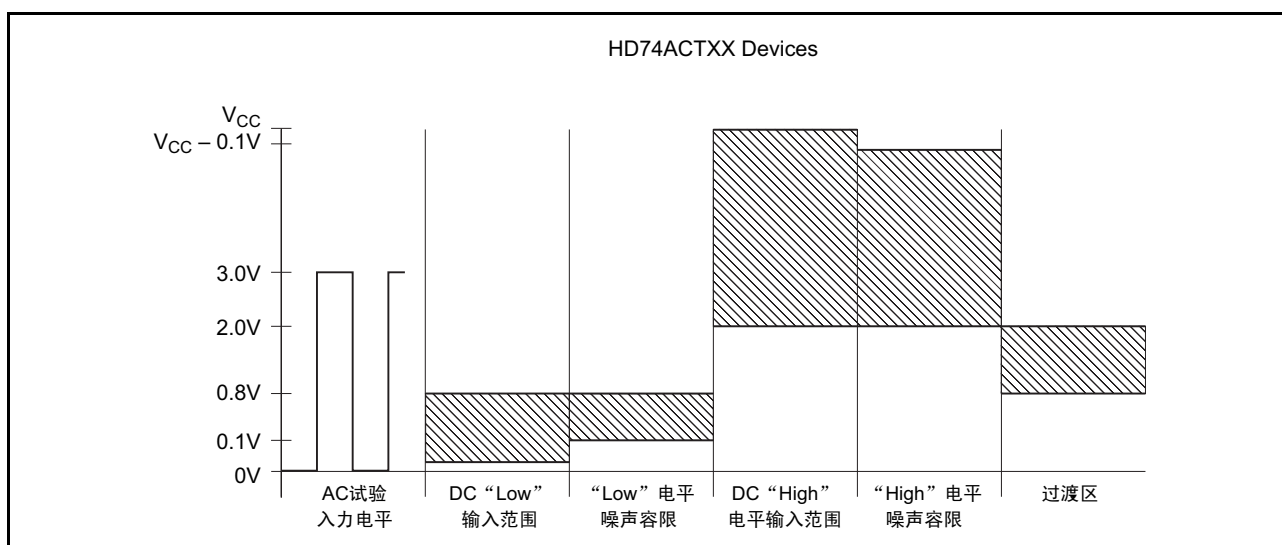


图3 输入信号的电压电平

DC特性项目试验的输入电压通常为规格中的 V_{IL} 和 V_{IH} 的值。

在进行试验时，尤其在使用IC测试设备和处理设备时，必须注意：需要适当地对电源实施去耦，试验信号不能受到噪声的影响。为了提高对测试仪固有噪声（在实际系统中不会发生）的噪声容限，有时需要调整输入电压电平。

在试验噪声容限时，必须将输入电压先升高到和电源电压 V_{CC} 相同的值，然后降低到相当于 V_{IH} 的电平，并且再升高到 V_{CC} 电平。对于 V_{IL} ，也需要将 V_{IN} 从0V升高到 V_{IL} 电平，再返回到0V。必须确认在输入电压为 V_{IH} 或者 V_{IL} 时输出不发生变化。

在制作测试夹具时，必须充分考虑高频特性的布线。为了将输出波形的波纹和负尖峰降到最小，必须尽量缩短负载电容的连线并且加宽GND布线（最好是地线面），还必须尽量缩短 V_{CC} 的旁路电容器连接到试验插座的连线。

4. 输入脉冲的上升时间和下降时间

在AC试验中，输入信号的上升时间和下降时间为3ns，AC系列的振幅为0V~ V_{CC} ，ACT系列的振幅为0V~3V。在测量最大时钟频率和脉宽时，输入信号的上升时间和下降时间不超过1ns。

如果延长输入信号的上升时间和下降时间，传统的HD14000B系列、HC系列、FACT等的CMOS就容易振荡。对于FACT，由于提高了速度等特性，所以和其他速度较慢的族相比，对于缓慢的输入信号的上升和下降就变得非常敏感。

振荡的原因有以下几种：

首先考虑输出部分。通常，CMOS的输出通过非常小的DC漏泄电流来驱动电容性负载。当输出从High电平变为Low电平或者从Low电平变为High电平时，此电容进行放电或者充电。对于现在的高性能器件，通常在2~3ns非常短的时间内进行充电或者放电。电容性负载的急速充放电会在输出部分引发瞬间的电流突变，因而封装内部的GND和 V_{CC} 引线因引线的寄生电感而产生电位差，导致芯片内的GND电位使封装外部发生变动。

其次考虑输入部分。如果芯片内的GND电位发生变动，对于DUT（被测量器件），输入的电压电平似乎发生了变动。如果输入电压的上升时间很长，就在输出发生变化时输入电压仍在器件的阈值区内或者非常接近阈值区。

如果因封装内的寄生电感而引起很大的电压变化，阈值区也会发生大的波变，并且输入电压会再次在阈值区上下变动。此时，如果器件的增益足够高并且输入电压的上升时间和下降时间很长，器件就会开始振荡。器件的传播延迟时间越短，输入电压停留在阈值区的时间也就越短。

器件的增益越高，输出的变化越急剧，电感产生的电压也就越高。输出越快，瞬间电流变化就越大，电感产生的电压也就越大。

在测量输入电压的上升时间和下降时间时出现的问题并不都是由封装相关的输出振荡引起的。

无论使用何种测试设备，其 V_{CC} 和GND引脚都带有某种有限电感。在决定输出发生变化时所感应的电压值时，还需要将封装的电感加上该测试设备引脚的电感。被测输入引脚的输入电压源离输入引脚越远，就越容易受到引脚的电感或者寄生电容的影响，也会受到重叠在输入信号上的各种噪声的影响。当FACT的增益约为100时，输出为5V最大摆动时所需的输入信号的振幅仅为50mV。

5. 传播延迟时间、最大时钟频率、准备时间和保持时间

在测量大部分的传播延迟时间时，使用 $f=1\text{MHz}$ 的方波；在测量最大时钟频率时，需要提高频率，但是占空比总保持在50%；在测量准备时间、保持时间和恢复时间等时，通常需要2台脉冲发生器。

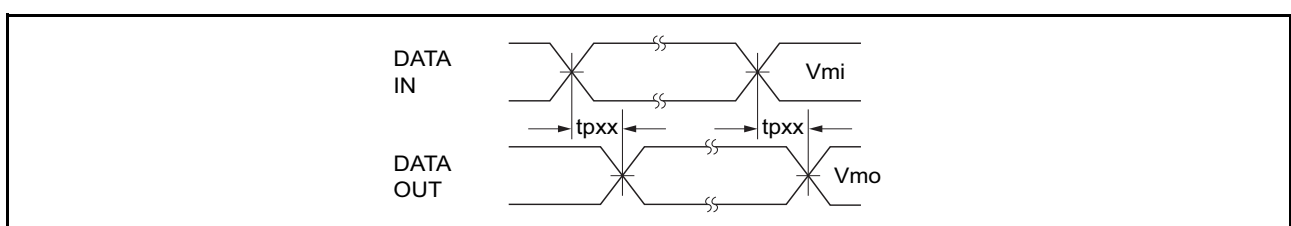


图4 传播延迟时间

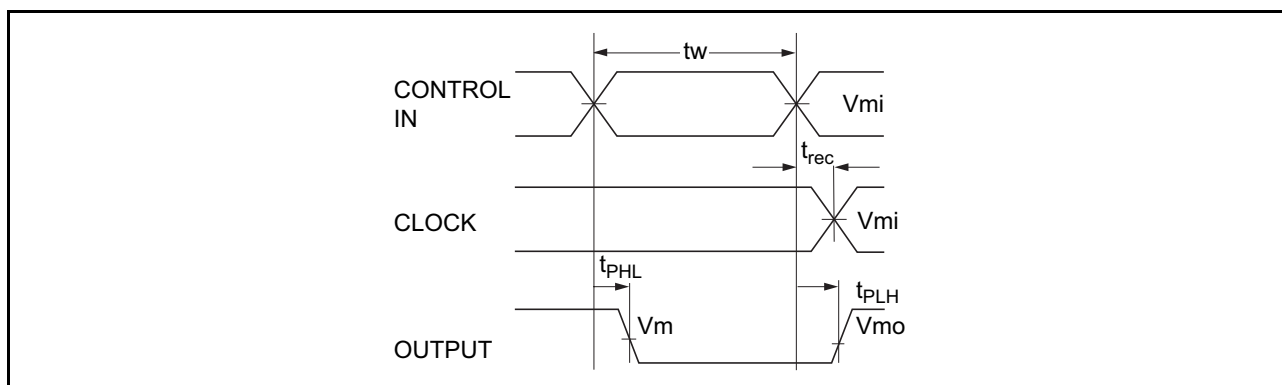


图5 传播延迟时间、脉冲时间和trec波形

6. 允许时间和禁止时间

如图6和图7所示，在输出从 V_{CC} 或者GND变化10%的点测量禁止时间。此方法能提高测量的再现性和缩短试验时间，同时能为系统设计者在计算最小周期时提供更现实的延迟时间。

高阻抗状态下的上升时间和下降时间取决于RC。最初的10%比较接近于直线，是不易受外部影响的部分。

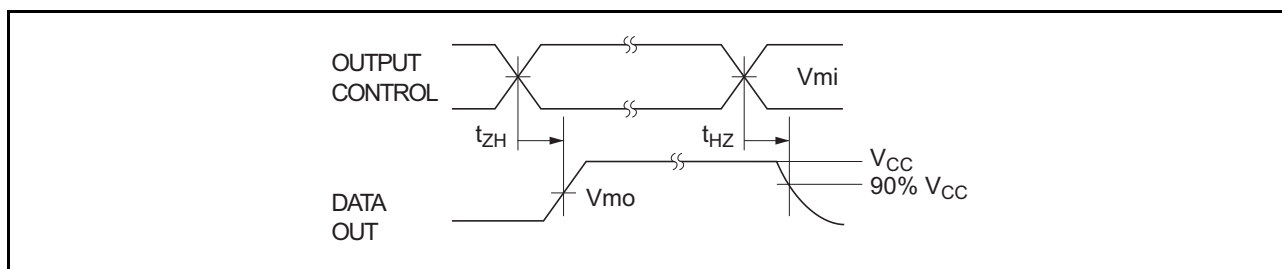


图6 三态输出的允许时间和禁止时间

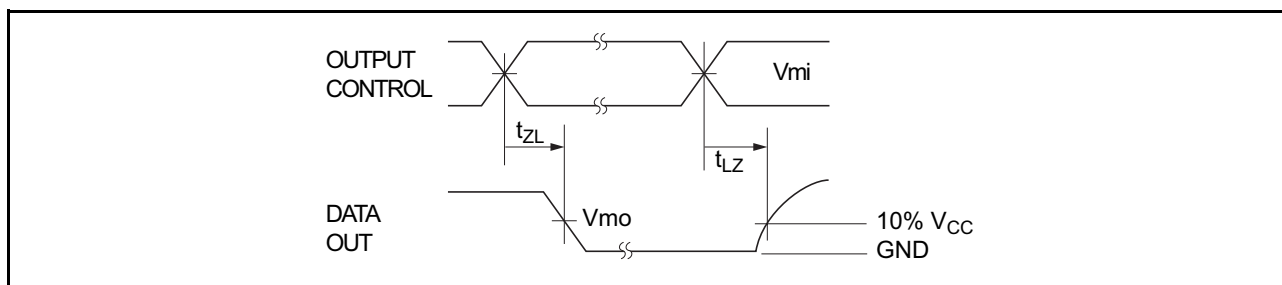


图7 三态输出的允许时间和禁止时间

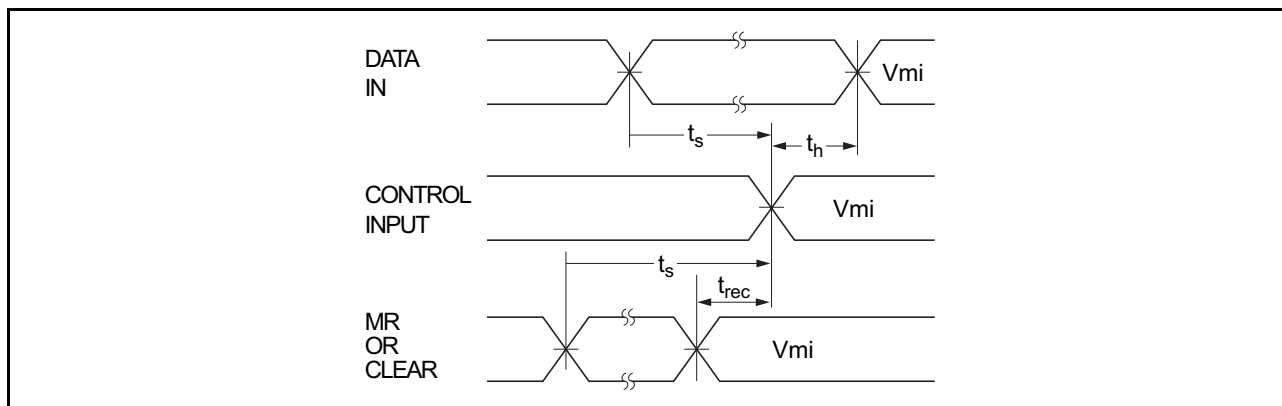


图8 准备时间、保持时间和恢复时间

对于一般的设计, 输出电压 10% 的变化是器件的输出为 OFF 时的适当值, 而在超过 10% 的变化点进行测量时, 只是延长了不必要的禁止时间。

在系统设计时, 即使在最坏的条件下, 也必须使用允许时间和禁止时间来设定时序信号, 以便在 1 个输出为 ON 状态前使其他所有的输出为 OFF 状态, 所以如果延长不必要的禁止时间, 就不利于系统的性能。

7. 功耗试验

为了避免测量 C_{PD} 时的混乱, JEDEC 规定了各种器件类型的试验条件。因此各种器件都按照此规定的方法进行试验, 而且容易进行规格的比较。规定了全部器件必须在 $V_{CC}=5.0V$ 、 $T_a=25^{\circ}C$ 的条件下进行试验; 在三态输出的情况下, 必须分别进行允许状态和禁止状态下的测量。

表 1 功耗试验

门电路	改变 1 个输入, 对其他输入施加偏压, 使对应的输出发生变化。
锁存器	使允许输入和 D 输入发生变化, 以便锁存器进行交替触发。
触发器	改变 D 输入 (或者对 J、K 输入施加偏压) 和时钟输入, 使输出在每个时钟周期发生变化。对于有共同时钟输入引脚的器件, 只能使 1 个触发器工作。
解码器	改变 1 个地址输入, 使 2 个输出发生变化。
多路复用器	改变 1 个地址输入, 给对应的数据输入施加反相逻辑电平的偏压, 使输出发生变化。
计数器	对输入施加偏压并改变时钟输入, 使计数器工作。
移位寄存器	对输入施加偏压并改变时钟输入, 使计数器工作。
收发器	改变 1 个数据输入, 对于双向器件, 只能将一个方向设定为允许状态。
奇偶发生器	改变 1 个输入。
优先编码器	改变优先级最低的输入。

分别给发生变化的输出外加 50pF 的负载电容。如果器件能在足够高的频率下工作, 就能忽视静态消耗电流, 可用下式表示 $f=1MHz$ 时的 C_{PD} 值:

$$C_{PD}=I_{CC}/(V_{CC})(1 \times 10^6) - \text{负载电容}$$

8. 静电击穿

必须注意防止静电对器件的损伤。合成纤维、地毯、塑料垫、托盘、软管、袋子等绝缘体、或者未接地的电子工具或者设备等很容易带电, 如果置于干燥的空气中, 问题将会变得更严重。通常, 作业人员在接触器件前, 需要触摸接地的物体, 最好通过 $100k\Omega \sim 1M\Omega$ 高电阻将人体接地。

而且, 许多接地不合适的处理设备有可能给器件带来损伤。因此, 必须确认在测试设备的塑料部件中, 靠近器件的部件全部需要具有导电性并且已经被接地。

修订记录

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